Program : **B.Tech**

Subject Name: **Analog and Digital Communication**

Subject Code: **IT-404**

Semester: **4th**

Unit-5

Digital modulations techniques, Generation, detection, equation and Bandwidth of amplitude shift keying (ASK) Binary Phase Shift keying (BPSK), Differential phase shift keying (DPSK), offset and non offset quadrature phase shift keying (QPSK), M-Ary PSK, Binary frequency Shift Keying (BFSK), M-Ary FSK Quadrature Amplitude modulation (QAM)

5.1. Digital Modulation

Digital Modulation provides more information capacity, high data security, quicker system availability with great quality communication. Hence, digital modulation techniques have a greater demand, for their capacity to convey larger amounts of data than analog modulation techniques.

There are many types of digital modulation techniques and also their combinations, as listed below.

ASK – Amplitude Shift Keying

The amplitude of the resultant output depends upon the input data whether it should be a zero level or a variation of positive and negative, depending upon the carrier frequency.

FSK – Frequency Shift Keying

The frequency of the output signal will be either high or low, depending upon the input data applied.

PSK – Phase Shift Keying

The phase of the output signal gets shifted depending upon the input. These are mainly of two types, namely Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK), according to the number of phase shifts. The other one is Differential Phase Shift Keying (DPSK) which changes the phase according to the previous value.

M-ary Encoding

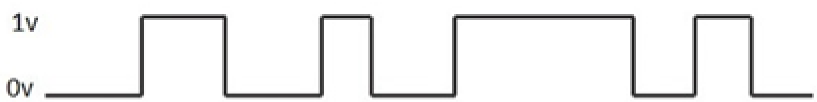
M-ary Encoding techniques are the methods where more than two bits are made to transmit simultaneously on a single signal. This helps in the reduction of bandwidth.

The types of M-ary techniques are M-ary ASK, M-ary FSK & M-ary PSK.

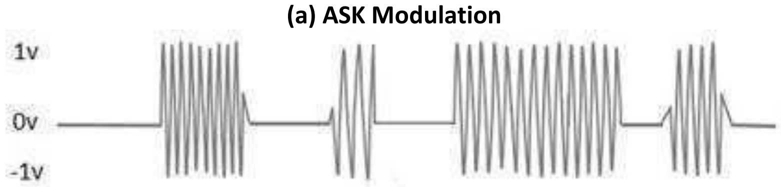
5.2. Amplitude Shift Keying (ASK) is a type of Amplitude Modulation which represents the binary data in the form of variations in the amplitude of a signal.

Any modulated signal has a high frequency carrier. The binary signal when ASK modulated, gives a zero value for Low input while it gives the carrier output for High input.

The figure 3.1.1 represents ASK modulated waveform along with its input.



(a) ASK Modulation



(b) ASK Modulated Wave

Figure 5.1. ASK Modulation

To find the process of obtaining this ASK modulated wave, let us learn about the working of the ASK modulator.

5.2.1. ASK Modulator

The ASK modulator block diagram comprises of the carrier signal generator, the binary sequence from the message signal and the band-limited filter. Following is the block diagram of the ASK Modulator.

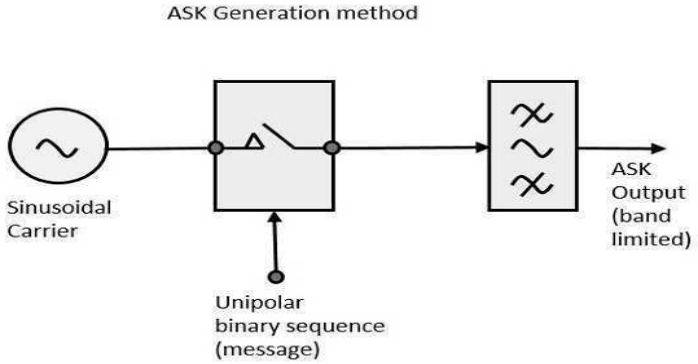


Figure 5.2. ASK Modulator

The carrier generator sends a continuous high-frequency carrier. The binary sequence from the message signal makes the unipolar input to be either High or Low. The high signal closes the switch, allowing a carrier wave. Hence, the output will be the carrier signal at high input. When there is low input, the switch opens, allowing no voltage to appear. Hence, the output will be low.

The band-limiting filter, shapes the pulse depending upon the amplitude and phase characteristics of the band-limiting filter or the pulse-shaping filter.

5.2.2. ASK Demodulator

There are two types of ASK Demodulation techniques. They are –

- Asynchronous ASK Demodulation/detection
- Synchronous ASK Demodulation/detection

The clock frequency at the transmitter when matches with the clock frequency at the receiver, it is known as a Synchronous method, as the frequency gets synchronized. Otherwise, it is known as Asynchronous.

5.2.3. Asynchronous ASK Demodulator

The Asynchronous ASK detector consists of a half-wave rectifier, a low pass filter, and a comparator. Following is the block diagram for the same.

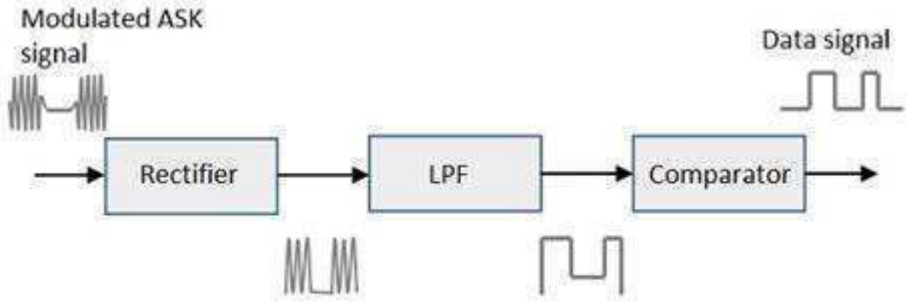


Figure 5.3. ASK Demodulator

The modulated ASK signal is given to the half-wave rectifier, which delivers a positive half output. The low pass filter suppresses the higher frequencies and gives an envelope detected output from which the comparator delivers a digital output.

5.2.4. Synchronous ASK Demodulator

Synchronous ASK detector consists of a Square law detector, low pass filter, a comparator, and a voltage limiter. Following is the block diagram for the same.

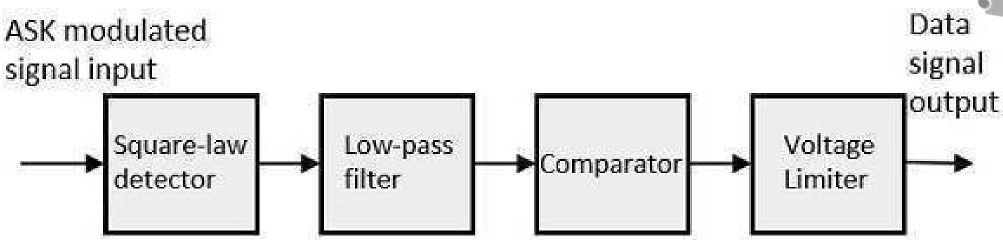


Figure 5.4. Synchronous ASK Demodulator

The ASK modulated input signal is given to the Square law detector. A square law detector is one whose output voltage is proportional to the square of the amplitude modulated input voltage. The low pass filter minimizes the higher frequencies. The comparator and the voltage limiter help to get a clean digital output.

5.3. Frequency Shift Keying

Frequency Shift Keying (FSK) is the digital modulation technique in which the frequency of the carrier signal varies according to the digital signal changes. FSK is a scheme of frequency modulation. The output of a FSK modulated wave is high in frequency for a binary High input and is low in frequency for a binary Low input. The binary 1s and 0s are called Mark and Space frequencies. The following image is the diagrammatic representation of FSK modulated waveform along with its input.

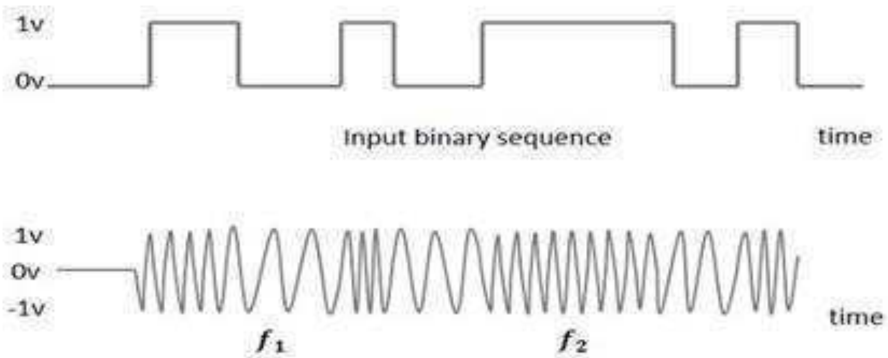


Figure 5.5. Frequency Shift Keying (FSK)

To find the process of obtaining this FSK modulated wave, let us know about the working of a FSK modulator.

5.3.1. FSK Modulator

Binary Frequency Shift Keying (BFSK)
In binary frequency-shift keying (BFSK) the binary data waveform d(t) generates a binary signal

$$v_{BFSK}(t) = \sqrt{2P_s}\cos[\omega_o t + d(t)\Omega t] \qquad \text{...3.7.1}$$

Here d(t) = + 1 or -1 corresponding to the logic levels 1and 0 of the data waveform. The transmitted signal is of amplitude $\sqrt{2P_s}$ and is either

$$v_{BFSK}(t) = S_H(t) = \sqrt{2P_s}\cos(\omega_o + \Omega)\, t \qquad \text{...3.7.2}$$

$$v_{BFSK}(t) = S_L(t) = \sqrt{2P_s}\cos(\omega_o - \Omega)\, t \qquad \text{...3.7.3}$$

and thus has an angular frequency $\omega_o + \Omega$ or $\omega_o - \Omega$ with Ω a constant offset from the nominal carrier frequency ω_o. We shall call the higher frequency ω_H(= $\omega_o + \Omega$) and the lower frequency ω_L.(= $\omega_o - \Omega$). We may conceive that the BFSK signal is generated in the manner indicated in Fig. 3.7.1. Two balanced modulators are used, one with carrier ω_H and one with carrier ω_L. The voltage values of $P_H(t)$ and of $P_L(t)$ are related to the voltage values of d(t) in the following manner

d(t)	$P_H(t)$	$P_L(t)$
+1V	+1V	0V
-1V	0V	+1V

Thus when d(t) changes from +1 to -1 P_H changes from 1 to 0 and P_L from 0 to 1. At any time either P_H or P_L is 1 but not both so that the generated signal is either at angular frequency ω_H or at ω_L.

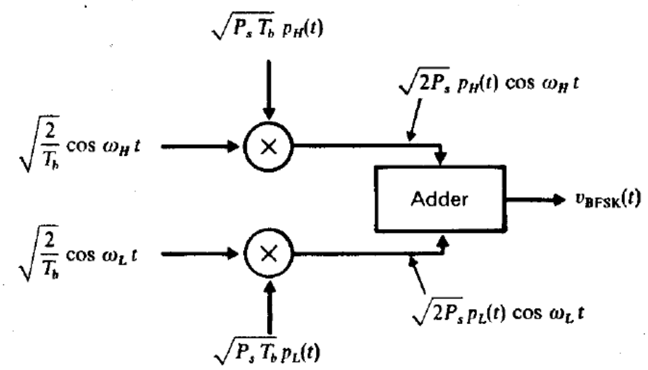


Figure 5.6. A representation of a manner in which a BFSK signal can be generated.

The two oscillators, producing a higher and a lower frequency signals, are connected to a switch along with an internal clock. To avoid the abrupt phase discontinuities of the output waveform during the transmission of the message, a clock is applied to both the oscillators, internally. The binary input sequence is applied to the transmitter so as to choose the frequencies according to the binary input.

5.3.2. FSK Demodulator

There are different methods for demodulating a FSK wave. The main methods of FSK detection are asynchronous detector and synchronous detector. The synchronous detector is a coherent one, while asynchronous detector is a non-coherent one.

5.3.3. Asynchronous FSK Detector

The block diagram of Asynchronous FSK detector consists of two band pass filters, two envelope detectors, and a decision circuit. Following is the diagrammatic representation.

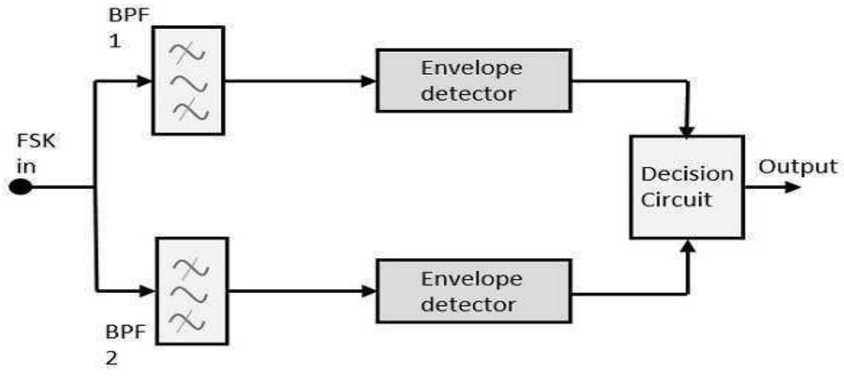


Figure 5.7. Asynchronous FSK Detector

The FSK signal is passed through the two Band Pass Filters (BPFs), tuned to Space and Mark frequencies. The output from these two Band Pass Filters looks like ASK signal; which is then applied to the envelope detector. The signal in each envelope detector is modulated asynchronously.

The decision circuit chooses which output is more likely and selects it from any one of the envelope detectors. It also re-shapes the waveform to a rectangular one.

5.3.4. Synchronous FSK Detector

The block diagram of Synchronous FSK detector consists of two mixers with local oscillator circuits, two band pass filters and a decision circuit. Following is the diagrammatic representation.

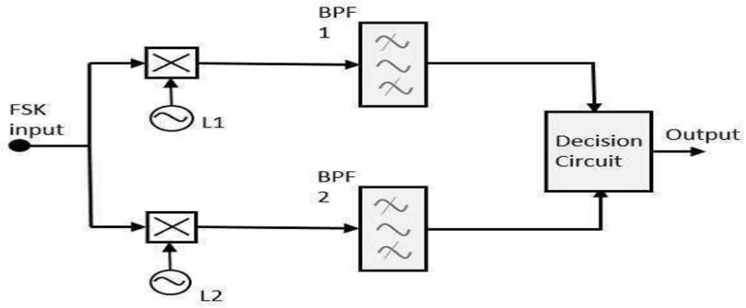


Figure 5.8. Synchronous FSK Detector

The FSK signal input is given to the two mixers with local oscillator circuits. These two are connected to two band pass filters. These combinations act as demodulators and the decision circuit chooses which output is more likely and selects it from any one of the detectors. The two signals have a minimum frequency separation.

For both of the demodulators, the bandwidth of each of them depends on their bit rate. This synchronous demodulator is a bit complex than asynchronous type demodulators.

5.3.5. Geometrical Representation of Orthogonal BFSK

In M-ary phase-shift keying and in quadrature-amplitude shift keying, any signal could be represented as $C_1u_1(t) + C_2u_2(t)$. There $u_1(t)$ and $u_2(t)$ are the orthonormal vectors in signal space, that is, $u1(t) = \sqrt{\frac{2}{T_s}}.\cos(\omega_o t)$and $u2(t) = \sqrt{\frac{2}{T_s}}.\sin(\omega_o t)$.

The functions u1 and u2 are orthonormal over the symbol interval T_S. And, if the symbol is a single bit, $T_S = T_b$. The coefficients C1 and C2 are constants. The normalized energies associated with $C_1u_1(t)$ and with $C_2u_2(t)$are respectively C_1^2 and C_2^2 and the total signal energy is $C_1^2 + C_2^2$.

In the present case of BFSK it is appropriate that the orthogonality should result from a special selection of the frequencies of the unit vectors. Accordingly, with m and n integers, let us establish unit vectors

$$u_1(t) = \sqrt{\frac{2}{T_b}}\cos 2\pi m f_b t \quad \text{...1}$$

and

$$u_2(t) = \sqrt{\frac{2}{T_b}}\cos 2\pi n f_b t \quad \text{...2}$$

Where $f_b=1/T_b$. The vectors U1 and U2 are the m^{th} and n^{th} harmonics of the (fundamental) frequency f_b. As we are aware, from the principles of Fourier analysis, different harmonics (m ± n) are orthogonal over the interval of the fundamental period $T_b = 1/f_b$.

If now the frequencies f_H and f_L in a BFSK system are selected to be (assuming m > n)

$$f_H = mf_b \quad \text{...3}$$

and

$$f_L = nf_b \quad \text{...4}$$

Then corresponding signal vectors are

$$S_H(t) = \sqrt{E_b}u_1(t) \quad \text{...5}$$

and

$$S_L(t) = \sqrt{E_b}u_2(t) \quad \text{...6}$$

The signal space representation of these signals is shown in Fig. 3.7.4. The signals, like the unit vectors are orthogonal. The distance between signal end points is therefore

$$d = \sqrt{2E_b}$$

Note that this distance is considerably smaller than the distance separating end points of BPSK signals, which are antipodal.

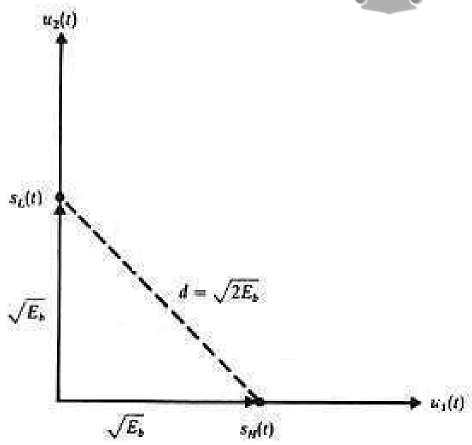


Figure 5.9. Signal Space representation of BFSK

5.4. Phase Shift Keying (PSK)

Phase Shift Keying (PSK) is the digital modulation technique in which the phase of the carrier signal is changed by varying the sine and cosine inputs at a particular time. PSK technique is widely used for wireless LANs, bio-metric, contactless operations, along with RFID and Bluetooth communications.
PSK is of two types, depending upon the phases the signal gets shifted. They are −

1. **Binary Phase Shift Keying (BPSK):** This is also called as 2-phase PSK or Phase Reversal Keying. In this technique, the sine wave carrier takes two phase reversals such as 0° and 180°.
2. **Quadrature Phase Shift Keying (QPSK):** This is the phase shift keying technique, in which the sine wave carrier takes four phase reversals such as 0°, 90°, 180°, and 270°.

5.4.1. BPSK Modulator:

The block diagram of Binary Phase Shift Keying consists of the balance modulator which has the carrier sine wave as one input and the binary sequence as the other input. Following is the diagrammatic representation.

BPSK Modulator

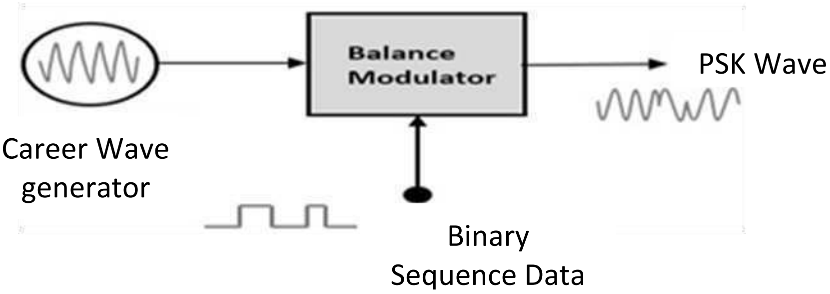


Figure 5.10 BPSK Modulator

The modulation of BPSK is done using a balance modulator, which multiplies the two signals applied at the input. For a zero binary input, the phase will be 0° and for a high input, the phase reversal is of 180°.
Following is the diagrammatic representation of BPSK Modulated output wave along with its given input.

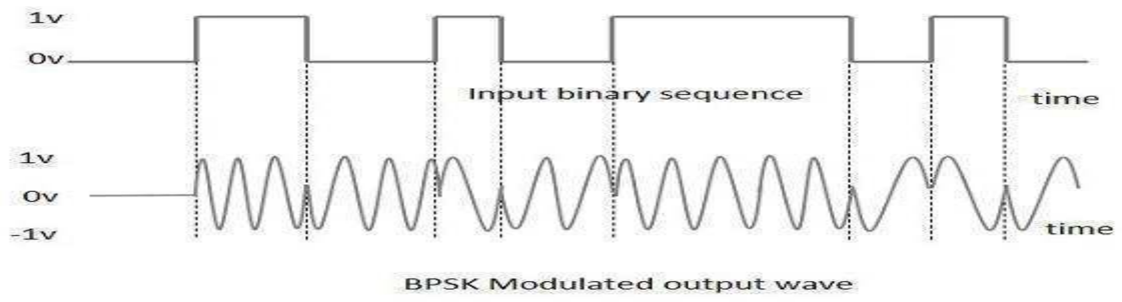


Figure 5.11. BPSK Modulated Waveform

The output sine wave of the modulator will be the direct input carrier or the inverted (180° phase shifted) input carrier, which is a function of the data signal.

5.4.2. BPSK Demodulator

The block diagram of BPSK demodulator consists of a mixer with local oscillator circuit, a band pass filter, a two-input detector circuit. The diagram is as follows.

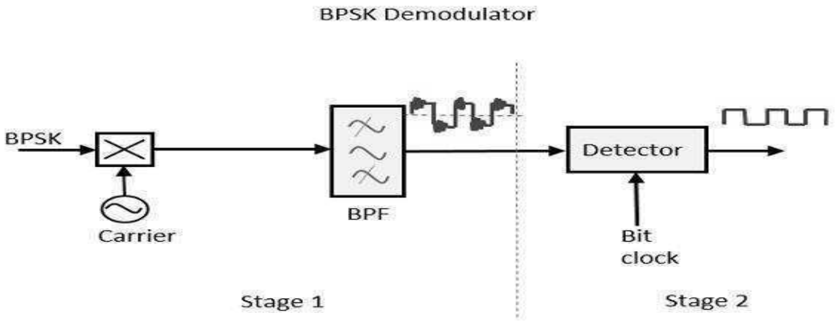


Figure 5.12 BPSK Demodulator

By recovering the band-limited message signal, with the help of the mixer circuit and the band pass filter, the first stage of demodulation gets completed. The base band signal which is band limited is obtained and this signal is used to regenerate the binary message bit stream.

In the next stage of demodulation, the bit clock rate is needed at the detector circuit to produce the original binary message signal. If the bit rate is a sub-multiple of the carrier frequency, then the bit clock regeneration is simplified. To make the circuit easily understandable, a decision-making circuit may also be inserted at the 2nd stage of detection.

5.5. Quadrature Phase Shift Keying (QPSK):

The Quadrature Phase Shift Keying (QPSK) is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier (DSBSC) modulation scheme, which sends two bits of digital information at a time, called as digits.

Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows space for the other users.

5.5.1. QPSK Modulator

The QPSK Modulator uses a bit-splitter, two multipliers with local oscillator, a 2-bit serial to parallel converter, and a summer circuit. Following is the block diagram for the same.

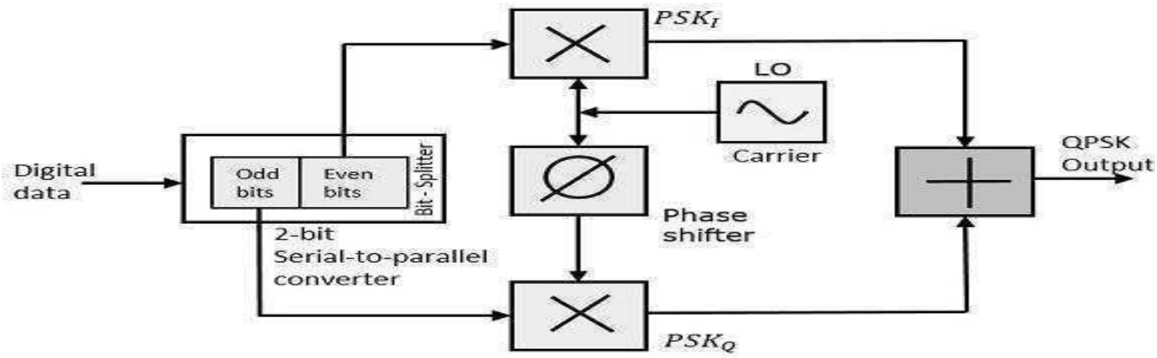


Figure 5.13 QPSK Modulator

At the modulator's input, the message signal's even bits (i.e., 2nd bit, 4th bit, 6th bit, etc.) and odd bits (i.e., 1st bit, 3rd bit, 5th bit, etc.) are separated by the bits splitter and are multiplied with the same carrier to generate odd BPSK (called as PSK_I) and even BPSK (called as PSK_Q). The PSK_Q signal is anyhow phase shifted by 90° before being modulated.

The QPSK waveform for two-bits input is as follows, which shows the modulated result for different instances of binary inputs.

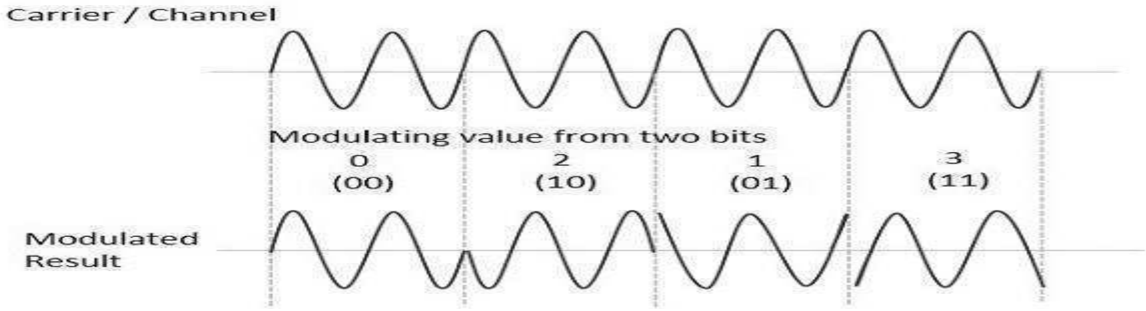


Figure 5.14 QPSK Waveforms

5.5.2. QPSK Demodulator

The QPSK Demodulator uses two product demodulator circuits with local oscillator, two band pass filters, two integrator circuits, and a 2-bit parallel to serial converter. Following is the diagram for the same.

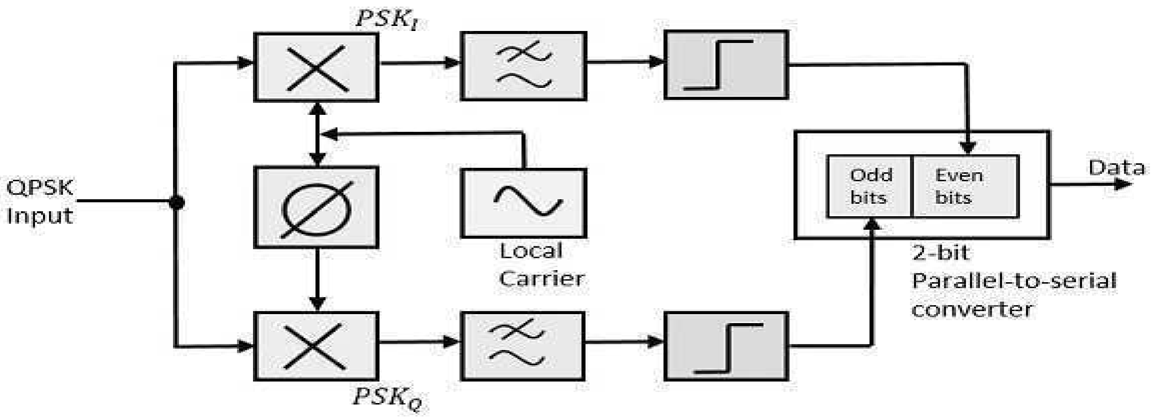


Figure 5.15 QPSK Demodulator

The two product detectors at the input of demodulator simultaneously demodulate the two BPSK signals. The pair of bits is recovered here from the original data. These signals after processing, are passed to the parallel to serial converter.

5.5.3. Phasor Diagram:

When b_0 = 1 the signal $s_o(t)$ = $\sqrt{P_s}.\sin(\omega_o t)$, and $s_o(t)$ = $-\sqrt{P_s}.\sin(\omega_o t)$ when b_o = -1. Correspondingly, for $b_e(t)$ = ± 1, $s_e(t)$ = $\pm.\sqrt{P_s}.(t)\cos(\omega_o t)$ These four signals have been represented as phasors in Fig. 3.4.4.4. They are in mutual phase quadrature. Also drawn are the phasors representing the four possible output signals $v_m(t) = so(t) + Se(t)$. These four possible output signals have equal amplitude $\sqrt{2P_s}$ and are in phase quadrature; they have been identified by their corresponding values of b_o and b_e. At the end of each bit interval (i.e., after each time T_b) either b_o, or b_e can change, but both cannot change at the same time. Consequently, the QPSK system shown in Fig. 3.4.4.3 is called offset or staggered QPSK and abbreviated OQPSK. After each time T_b, the transmitted signal, if it changes, changes phase by 90° rather than by 180° as in BPSK.

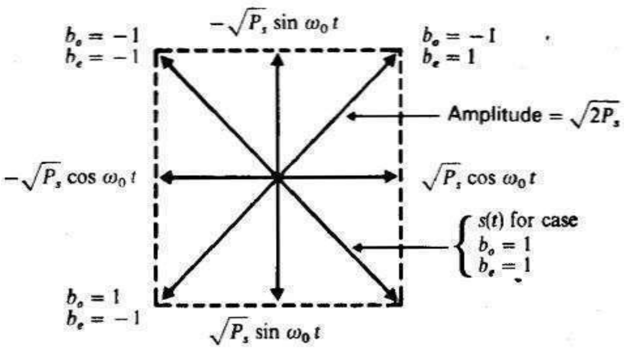


Figure 5.16. Phasor diagrams for the sinusoids

5.5.4. Non-offset QPSK

Suppose that in Fig. 3.4.4.3 we introduce an additional flip-flop before either the odd or even flip-flop. Let this added flip-flop be driven by the clock which runs at the rate f_b. Then one or the other bit streams, odd or even, will be delayed by one bit interval. As a result, we shall find that two bits which occur in time sequence (i.e., serially) in the input bit stream b(t) will appear at the same time (i.e., in parallel) at the outputs of the odd and even flip-flops. In this case $b_e(t)$ and $b_o(t)$ can change at the same time, after each time $2T_b$, and there can be a phase change of 180° in the output signal. There is no difference, in principle, between a staggered and non-staggered system.

In practice, there is often a significant difference between QPSK and OQPSK. At each transition time, T" for OQPSK and $2T_b$ for QPSK, one bit for OQPSK and perhaps two bits for QPSK change from 1V to -1V or -1V to 1V. Now the bits be(t) and bo(t) can, not change instantaneously and, in changing, must pass through zero and dwell in that neighborhood at least briefly. Hence there will be brief variations in the amplitude of the transmitted waveform. These variations will be more pronounced in QPSK than in OQPSK since in the first case both be(t) and bo(t) may be zero simultaneously so that the signal amplitude may actually be reduced to zero temporarily.

5.6. Differential Phase Shift Keying (DPSK)

In Differential Phase Shift Keying (DPSK) the phase of the modulated signal is shifted relative to the previous signal element. No reference signal is considered here. The signal phase follows the high or low state of the previous element. This DPSK technique doesn't need a reference oscillator.

The following figure represents the model waveform of DPSK.

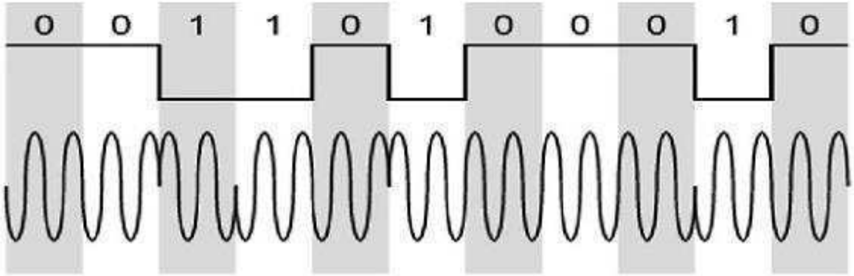


Figure 5.17 Differential Phase Shift Keying (DPSK)

It is seen from the above figure that, if the data bit is Low i.e., 0, then the phase of the signal is not reversed, but continued as it was. If the data is a High i.e., 1, then the phase of the signal is reversed, as with NRZI, invert on 1 (a form of differential encoding).
If we observe the above waveform, we can say that the High state represents an M in the modulating signal and the Low state represents a W in the modulating signal.

5.6.1. DPSK Modulator

DPSK is a technique of BPSK, in which there is no reference phase signal. Here, the transmitted signal itself can be used as a reference signal. Following is the diagram of DPSK Modulator.

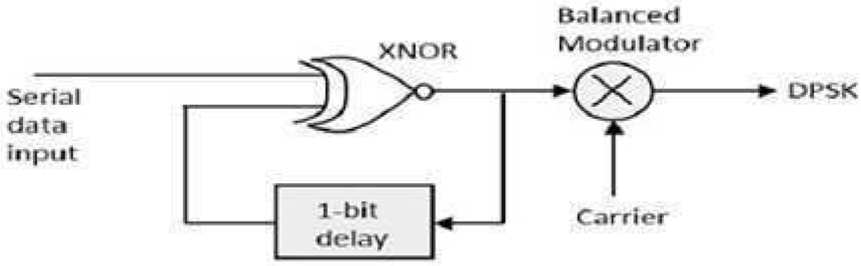


Figure 5.18 DPSK Modulator

DPSK encodes two distinct signals, i.e., the carrier and the modulating signal with 180° phase shift each. The serial data input is given to the XNOR gate and the output is again fed back to the other input through 1-bit delay. The output of the XNOR gate along with the carrier signal is given to the balance modulator, to produce the DPSK modulated signal.

5.6.2. DPSK Demodulator

In DPSK demodulator, the phase of the reversed bit is compared with the phase of the previous bit. Following is the block diagram of DPSK demodulator.

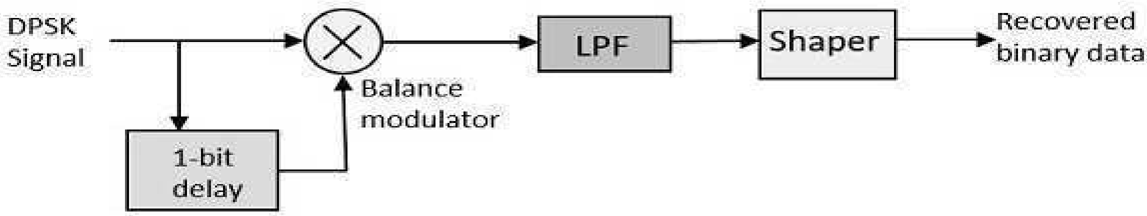


Figure 5.19 DPSK Demodulator

From the above figure, it is evident that the balance modulator is given the DPSK signal along with 1-bit delay input. That signal is made to confine to lower frequencies with the help of LPF. Then it is passed to a shaper circuit, which is a comparator or a Schmitt trigger circuit, to recover the original binary data as the output.

5.7. M-ary Equation

The word binary represents two bits. M represents a digit that corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables.
This is the type of digital modulation technique used for data transmission in which instead of one bit, two or more bits are transmitted at a time. As a single signal is used for multiple bit transmission, the channel bandwidth is reduced.
If a digital signal is given under four conditions, such as voltage levels, frequencies, phases, and amplitude, then M = 4. The number of bits necessary to produce a given number of conditions is expressed mathematically as $N=\log 2M$. Where N is the number of bits necessary M is the number of conditions, levels, or combinations possible with N bits.
The above equation can be re-arranged as

$$2N=M$$

For example, with two bits, $2^2 = 4$ conditions are possible.

5.7.1. Types of M-ary Techniques

In general, Multi-level (M-ary) modulation techniques are used in digital communications as the digital inputs with more than two modulation levels are allowed on the transmitter's input. Hence, these techniques are bandwidth efficient. There are many M-ary modulation techniques. Some of these techniques, modulate one parameter of the carrier signal, such as amplitude, phase, and frequency.

5.7.2. M-ary ASK

This is called M-ary Amplitude Shift Keying (M-ASK) or M-ary Pulse Amplitude Modulation (PAM).
The amplitude of the carrier signal, takes on M different levels.

Representation of M-ary ASK

$S_m(t) = A_m \cos(2\pi f_c t) \qquad A_m \in (2m - 1 - M)\Delta, m = 1,2, \dots \dots M$ and $0 \leq t \leq T_s$

Some prominent features of M-ary ASK are −

- This method is also used in PAM.
- Its implementation is simple.
- M-ary ASK is susceptible to noise and distortion.

5.4. M-ARY FSK

An M-ary FSK communications system is shown in Fig. 5.19. It is an obvious extension of a binary FSK system. At the transmitter an N-bit symbol is presented each T_S, to an N-bit D/A converter. The converter output is applied to a frequency modulator, i.e., a piece of hardware which generates a carrier waveform whose frequency is determined by the modulating waveform. The transmitted signal, for the duration of the symbol interval, is of frequency f_0 or f_1 ...or f_{M-1} with M = 2^N. At the receiver, the incoming signal is applied to M paralleled band pass filters each followed by an envelope detector. The band pass filters have center frequencies $f_0, f_1, \dots, f_{M-1}$. The envelope detectors apply their outputs to a device which determines which of the detector indications is the largest and transmits that envelope output to an N-bit AID converter.
The probability of error is minimized by selecting frequencies $f_0, f_1, \dots, f_{M-1}$ so that the M signals are mutually orthogonal. One commonly employed arrangement simply provides that the carrier frequency be successive even harmonics of the symbol frequency $f_S=1/T_S$. Thus the lowest frequency, say f_0, is f_0 = k f_S, while $f_1 = (k + 1) f_S$, $f_2 = (k + 2) f_S$ etc. In this case, the spectral density patterns of the individual possible transmitted signals overlap in the manner shown in Fig. 5.20. We observe that to pass M-ary FSK the required spectral range is

$$B = 2Mf_S \qquad \dots 1$$

Since $f_S= f_b/N$ and M=2^N, we have

$$B = 2^{N+1}f_b/N \qquad \dots 2$$

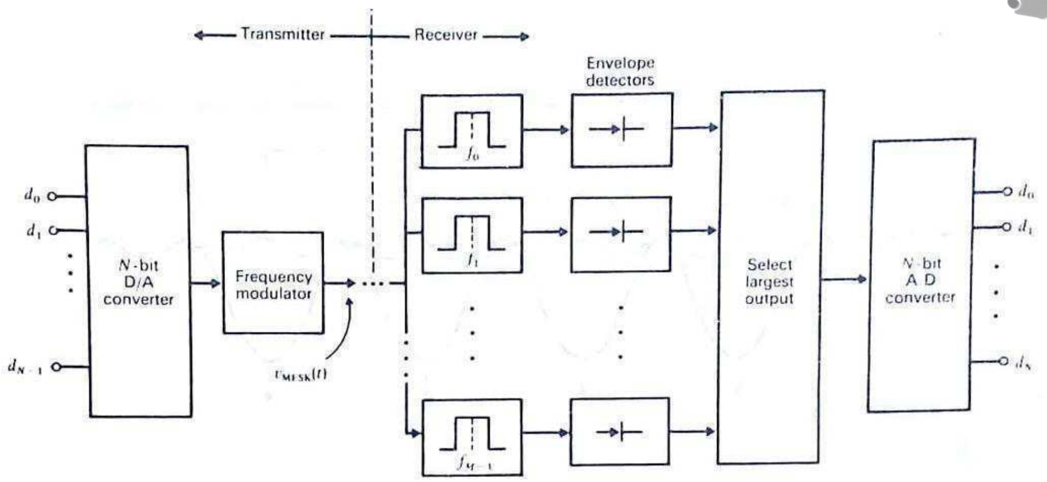


Figure 5.20 An M-ARY Communication System

Note that M-ary FSK requires a considerably increased bandwidth in comparison with M-ary PSK. However, as we shall see, the probability of error for M-ary FSK decreases as M increases, while for M-ary PSK, the probability of error increases with M.

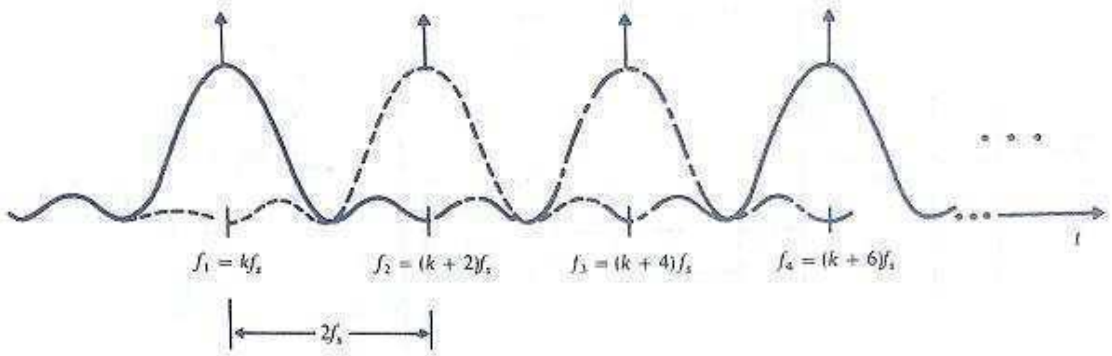


Figure 5.21. Power Spectral Density of an M-ARY FSK (Four Frequencies are shown)

Geometrical Representation of an M-ARY FSK

The case of M-ary orthogonal FSK signals is shown in figure 5.21. We simply conceive of a coordinate system with M mutually orthogonal coordinate axes. The square of the length of the signal vector is the normalized signal energy. When the frequencies are selected to generate orthogonal signals.

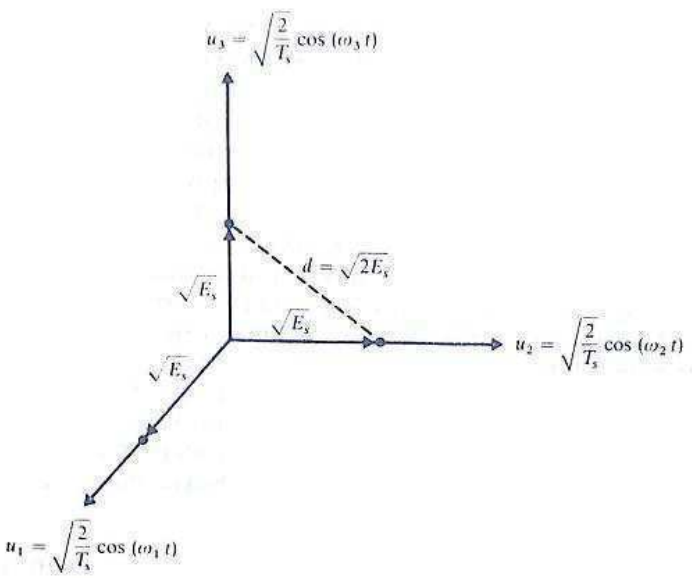


Figure 5.22 Geometrical representation of orthogonal M-ary FSK (M = 3)

Note that this value of d is greater than the values of d calculated for M-ary PSK with the exception of the cases M = 2 and M = 4. It is also greater than d in the case of 16-QASK.

$$d = \sqrt{2E_s} = \sqrt{2NE_b}$$

5.7.3. M-ary FSK
This is called as M-ary Frequency Shift Keying (M-ary FSK).
The frequency of the carrier signal, takes on M different levels.

Representation of M-ary FSK

$$S_i(t) = \sqrt{\frac{2E_s}{T_s}} \cos\left(\frac{\pi}{T_s}(n_c + i)t\right) \qquad 0 \le t \le T_s \quad i = 1,2,\dots\dots M$$

Where $fc = nc/\,2Ts$

for some fixed integer n.
Some prominent features of M-ary FSK are –

- Not susceptible to noise as much as ASK.
- The transmitted M number of signals are equal in energy and duration.
- The signals are separated by 12Ts
- Hz making the signals orthogonal to each other.
- Since M signals are orthogonal, there is no crowding in the signal space.
- The bandwidth efficiency of M-ary FSK decreases and the power efficiency increases with the increase in M.

5.7.3. M-ary PSK
This is called as M-ary Phase Shift Keying (M-ary PSK).
The phase of the carrier signal, takes on M different levels.
Representation of M-ary PSK

$$S_i(t) = \sqrt{\frac{2E}{T}} \cos(\omega_{0t} + \phi_i t) \qquad 0 \le t \le T \ and \quad i = 1,2,\dots\dots M$$

$\phi_i(t) = \frac{2\pi i}{M}$ where $i = 1,2,\dots\dots M$

Some prominent features of M-ary PSK are –

- The envelope is constant with more phase possibilities.
- This method was used during the early days of space communication.
- Better performance than ASK and FSK.
- Minimal phase estimation error at the receiver.
- The bandwidth efficiency of M-ary PSK decreases and the power efficiency increases with the increase in M.

In BPSK we transmit each bit individually. Depending on whether b(t) is logic 0 or logic 1, we transmit one or another of a sinusoid for the bit time T_b, the sinusoids differing in phase by 2π/2 = 180^0. In QPSK we lump together two bits. Depending on which of the four two-bit words develops, we transmit one or another of four sinusoids of duration $2T_b$ the sinusoids differing in phase by amount 2π/4 = 90°. The scheme can be extended. Let us lump together N bits so that in this N-bit symbol, extending over the time NT_b, there are 2N = M possible symbols. Now let us represent the symbols by sinusoids of duration $NT_b= T_s$ which differ from one another by the phase 2 π / M. Hardware to accomplish such M-ary communication is available.

Thus in M-ary PSK the waveforms used to identify the symbols are

$$v_m(t) = \sqrt{2P_s} \cos(\omega_o t + \emptyset_m) \text{ (m=0, 1, ..., M-1)} \qquad \dots 1$$

Where phase angle is given by

$$\emptyset_m = (2m+1)\frac{\pi}{M} \qquad \dots 2$$

The waveforms of Eq. are represented by the dots in Fig. 5.1 in a signal space in which the coordinate axes are the orthonormal waveforms $u1(t) = \sqrt{2/T_s}\cos(\omega_o t)$ and $u2(t) = \sqrt{2/T_s}\sin(\omega_o t)$. The distance of each dot from the origin is $\sqrt{E_s} = \sqrt{P_s T_s}$

From Eq. (1) we have

$$v_m(t) = (\sqrt{2P_s}\cos\emptyset_m)\cos(\omega_o t) - (\sqrt{2P_s}\sin\emptyset_m)\sin(\omega_o t) \qquad ...3$$

Defining p_e and p_o by

$$p_e = \sqrt{2P_s}\cos\emptyset_m \qquad ...4$$

$$p_o = \sqrt{2P_s}\sin\emptyset_m \qquad ...5$$

Equation 3 becomes

$$v_m(t) = p_e\cos(\omega_o t) - p_o\sin(\omega_o t) \qquad ...6$$

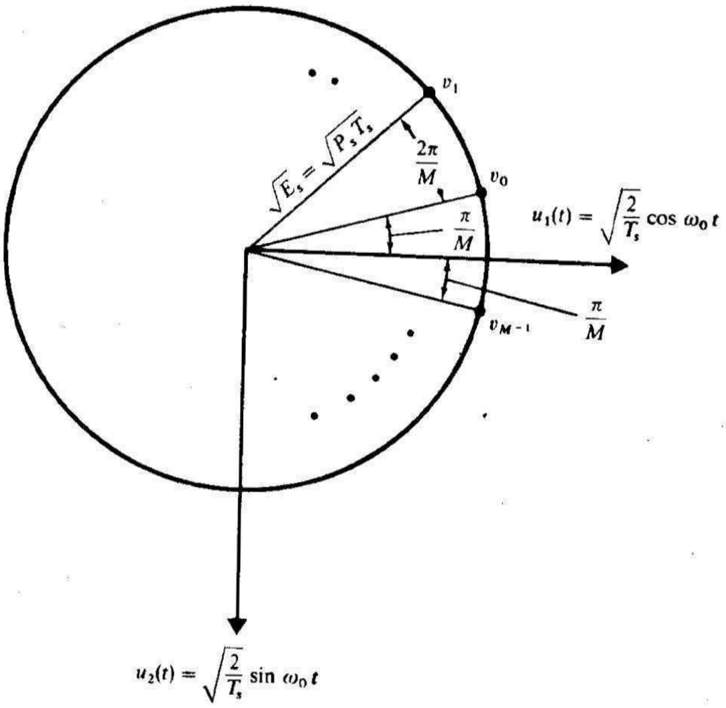


Figure 5.23 Graphical representation of M-ary PSK Signals

M-ary Transmitter and Receiver

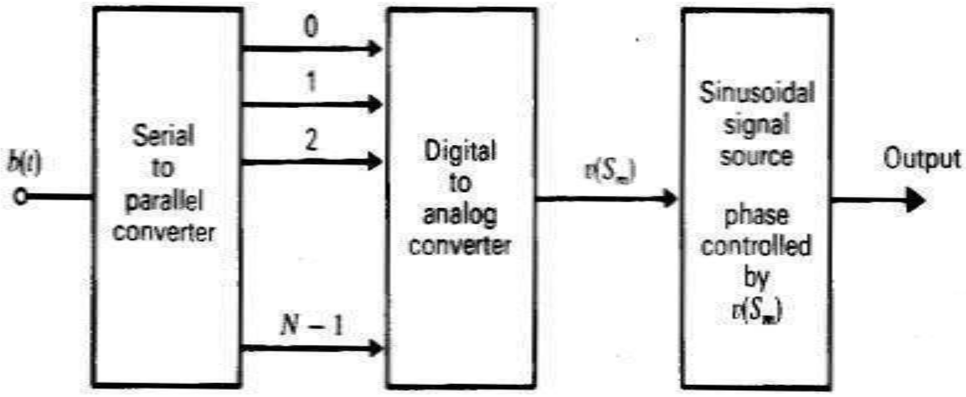


Figure.5.24. M Ary Transmitter

The transmitter, the bit stream b(t) is applied to a serial-to-parallel converter. This converter has facility for storing the N bits of a symbol. The N bits have been presented serially, that is, in time sequence, one after another. These N bits, having been assembled, are then presented all at once on N output lines of the converter, that is they are presented in parallel. The converter output remains unchanging for the duration NTb of a symbol during which time the converter is assembling a new group of N bits. Each symbol time the converter output is updated.

The converter output is applied to a D/A converter. This D/A converter generates an output voltage which assumes one of 2N = M different values in a one to-one correspondence to the M possible symbols applied to its input. That is, the D/A output is a voltage v(Sm) which depends on the symbol Sm (m = 0, 1,... ,M - 1).

Finally v(Sm) is applied as a control input to a special type of constant amplitude sinusoidal signal source whose phase 4>m is determined by v(Sm). Altogether, then, the output is a fixed amplitude, sinusoidal waveform, whose phase has a one-to-one correspondence to the assembled N-bit symbol. The phase can change once per symbol time.

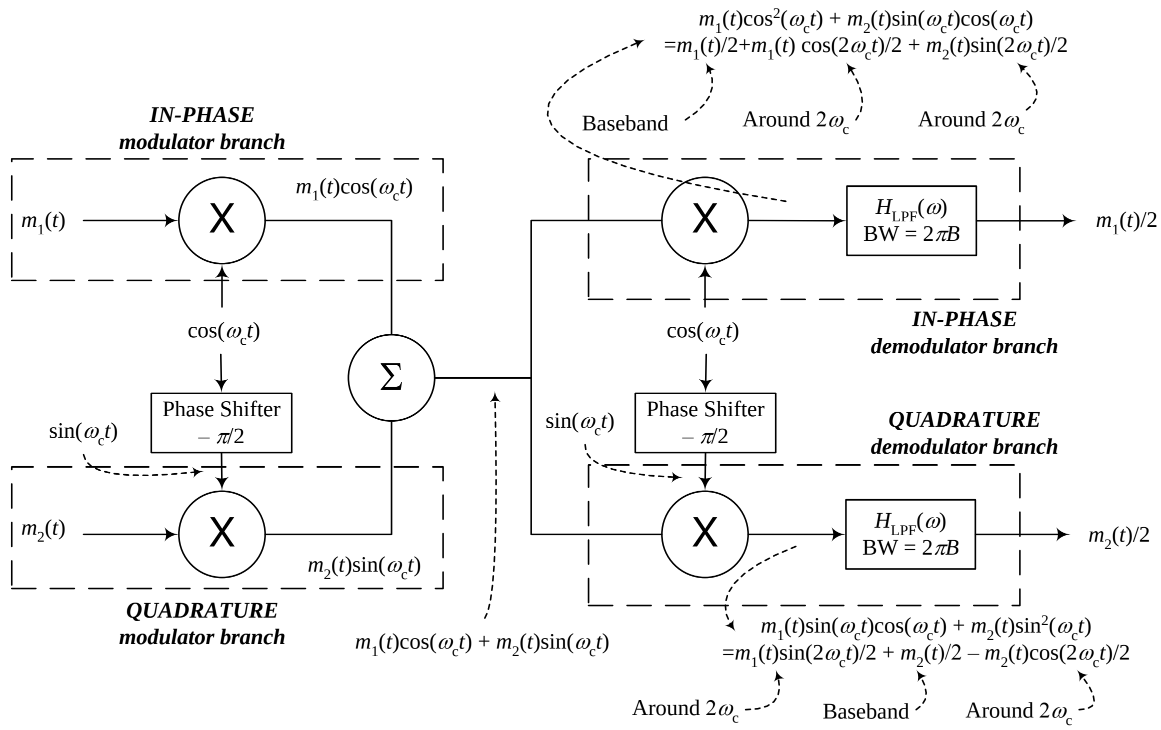
5.9. Quadrature Amplitude Modulation (QAM):

Quadrature Amplitude Modulation, QAM utilises both amplitude and phase components to provide a form of modulation that is able to provide high levels of spectrum usage efficiency. QAM, quadrature amplitude modulation has been used for some analogue transmissions. QAM is a signal in which two carriers shifted in phase by 90 degrees (i.e. sine and cosine) are modulated and combined. As a result of their 90° phase difference they are in quadrature and this gives rise to the name. Often one signal is called the In-phase or "I" signal, and the other is the quadrature or "Q" signal.

The resultant overall signal consisting of the combination of both I and Q carriers contains of both amplitude and phase variations. In view of the fact that both amplitude and phase variations are present it may also be considered as a mixture of amplitude and phase modulation.

The basic way in which a QAM signal can be generated is to generate two signals that are 90° out of phase with each other and then sum them. This will generate a signal that is the sum of both waves, which has certain amplitude resulting from the sum of both signals and a phase which again is dependent upon the sum of the signals.

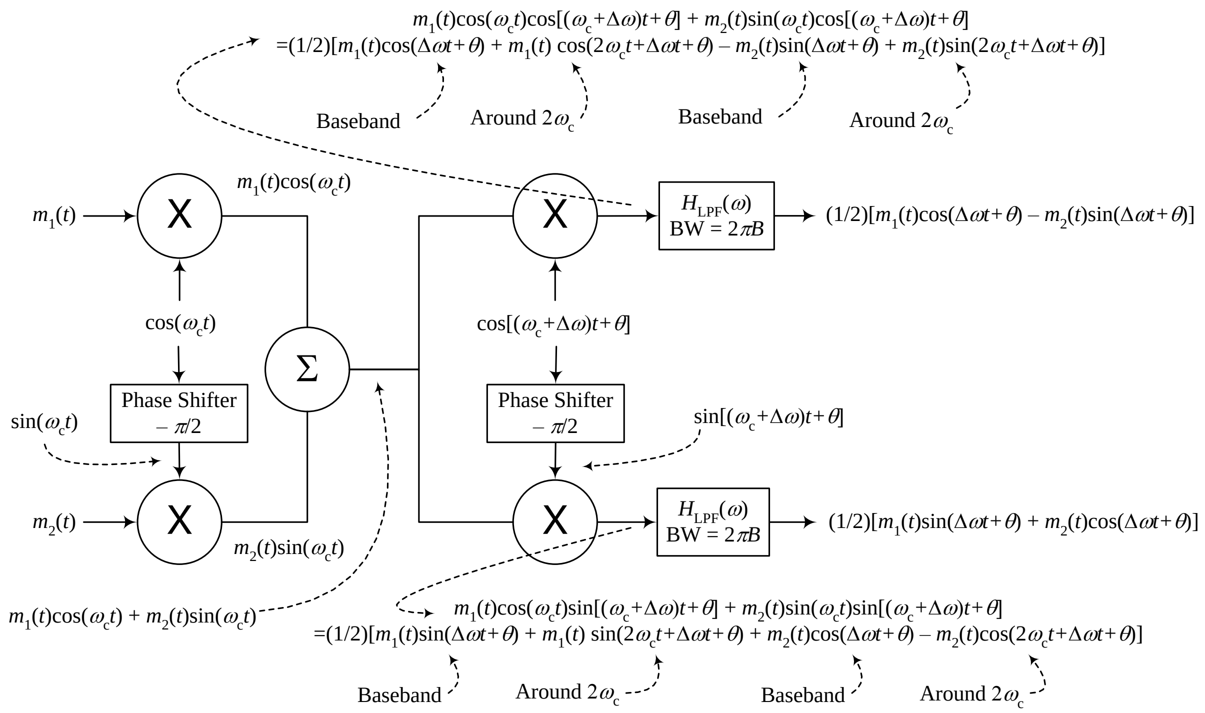
Consider the following block diagram of a Quadrature Amplitude Modulation (QAM) and Demodulation system:



QAM Modulator/Demodulator

Figure.5.24. QAM Modulator and demodulator

The modulator/demodulator system shown above clearly is able to modulate and demodulate two different signals without any interference. However, if the generation of the carrier at the demodulator had even small phase or frequency errors, the demodulated signals will interfere at the outputs. The following figure illustrate what happens when the carrier at the demodulator has a small frequency error $\Delta\omega$ (must be a small value much less than ω_c) and/or a small phase error θ.



QAM Modulator/Demodulator with Demodulator Carrier Phase and/or Frequency Error

If the carrier at the receiver has a small frequency error $\Delta\omega$ (but a phase error θ=0), we see that the two output signal become

$$r_1(t) = \frac{1}{2}\left[m_1(t)\cos(\Delta\omega t) - m_2(t)\sin(\Delta\omega t)\right]$$

$$r_2(t) = \frac{1}{2}\left[m_1(t)\sin(\Delta\omega t) + m_2(t)\cos(\Delta\omega t)\right].$$

Clearly, in this case, the output signals are not purely either of the two message signals but a combination. The ratio of message 1 to message 2 at the different outputs changes as a sinusoid with a frequency equal to the frequency error $\Delta\omega$.

If the carrier at the receiver has a phase error θ (but a frequency error $\Delta\omega = 0$), we see that the two output signal become

$$r_1(t) = \frac{1}{2}\left[m_1(t)\cos(\theta) - m_2(t)\sin(\theta)\right]$$

$$r_2(t) = \frac{1}{2}\left[m_1(t)\sin(\theta) + m_2(t)\cos(\theta)\right]$$

