



WCL RVP Hardware Architecture Specification

Revision 0.5

February 2024

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Revision History

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Reference Documents/ Links

- i. WCL RVP PDT SharePoint [link](#)
- ii. WCL Platform Architecture [link](#)
- iii. WCL Platform SAS documents [link](#)
- iv. WCL Platform CCB [link](#)

Document Conventions

The terms WCL, processor and SoC are used interchangeably in the document.

Small letter ‘b’ stands for bits, e.g. Mbps stands for Megabits per second. Capital letter ‘B’ stands for Bytes, e.g. MB stands for Megabytes.

All binary numbers will have a suffix ‘b’ at the end of the number, e.g. 00110b. Hexadecimal numbers will be mentioned with a prefix ‘0x’, e.g. 0x11FD. Decimal numbers will not have any suffix or prefix.

Capital letter ‘HDR’ stands for Header in the figures.

Items mentioned as **TBD** are open and yet to be closed from the design perspective.

Acronyms

Acronym	Description
WCL	Wildcat Lake
MTL	Meteor Lake
ARL	Arrow Lake
ADL	Alder Lake
AIC	Add-In Card
ALS	Active Level Shifter
BOM	Bill of Material
BP	Back Panel
BSSB	Boundary Scan Sideband
CC	Configuration channel
CRLS	Cost Reduced Level Shifter
DCI-OOB	Direct Connect Interface Out of Band
DDR	Double Data Rate
DnX	Download and execute
DP	Display port
DPC	DIMMs Per Channel
EC	Embedded controller
FP	Front Panel
GND	Ground return
HDMI	High-Definition Multimedia Interface
I3C	Improved Inter Integrated Circuit also known as Sense Wire
IIC or I2C	Inter-Integrated Circuit
KoZ	Keep-out Zone
LSPCON	Level Shifter Protocol Converter
MR	Maple Ridge

NOA	Node Observation Architecture
PCH	Platform Controller Hub
PD	Power Delivery
PD	Power Down
POR	Plan of record
PSS	Processor Secured Storage
RVP	Reference Validation Platform
SBU	Sideband use
SKU	Stock Keeping Unit
SML/SMB	System management link/Bus
SODIMM	Single Outline Dual Inline Memory Module
SPI	Serial Peripheral Interface
TBT	Thunderbolt
TCPC	Type-C port controller
TCPs	Type-C ports
TCSS	Type-C sub system
THC	Touch Host Controller
UFP / DFP	Upstream/Downstream Facing Port
USB	Universal Serial Bus
VBUS	Bus power
VISA	Visualization of Internal Signals Architecture
WIP	Work In Progress
XDP	eXtended Debug Port

1 Introduction

The scope of this document is to cover the overall functional architecture for the WCL RVPs including the debug and validation hooks. The document would describe the architecture and feature set of WCL RVP's and the design in detail.

1.1 Design Team

The key contacts for WCL RVP are given in Table 1 below.

Table 1 : Key Contacts for WCL RVP design

Role	Point of Contact
RVP Program Manager, Systems PDT, Boards & Kits	Sundarabhattar, Sinkaravelan
RVP Engineering Manager	Liew, Jia Lin
RVP Architect	Sharma, Deepak Parameswaran, Pharveen Tan, Adrian (PD Architect)
RVP Design Lead	Zakaria, Anas
RVP Design Engineers	Ch, Manjunath Devaraju, Ramya K S, Vachana Li, Kok Wai Ryan Lim, Kok Leng
RVP Power Delivery Lead	Au, Chun Ming
RVP PCB Layout Lead	Lee, Poh Ling (RVP1) Selvaraj, Balaji (RVP2)
Mechanical Team	Kaja, Ajmeer
Validation Lead & CSF	R, Hemananth

1.2

RVP Design SKUs

The WCL will have the SKUs as listed in Table 2. All the boards will have same implementation from PI / PnP perspective. All RVP boards will have PnP HDR place holders; however, only PnP BOM SKU RVPs will be stuffed with 2x7 HDRs.

There would be other design options provided on each board which are explained in the respective interface functional specification section of the document.

Table 2 : WCL RVP Design SKUs

RVP SKU	SKU Description	Remarks
ERB		
ERBa	WCL DDR5 SODIMM T3 ERB	
ERBb – BOM SKU	WCL DDR5 SODIMM Chrome SKU	Early enablement with DDR5 SKU and later fully migrates to LP5x.
RVP1		
RVP1a	WCL DDR5 SODIMM T3 RVP	Volume Runner, iPOR= 7200Mbps
RVP1b – BOM SKU	WCL DDR5 PPV SKU	
RVP1c – BOM SKU	WCL DDR5 PnP SKU	
RVP2		
RVP2a	WCL LP5x MD, x32, T3 RVP	iPOR = 7200Mbps
RVP2b – BOM SKU	WCL LP5x Socketed SKU	Deployment for EV, PnP teams, for different memory validation
RVP2c – BOM SKU	WCL LP5x Chrome SKU	
RVP2d – BOM SKU	WCL LP5x HSIO SKU	No separate HSIO RVP, requirement covered through BOM stuffing option
RVP2e – BOM SKU	WCL LP5x PnP SKU	
RVP2f – BOM SKU	WCL LP5x MECC SKU	

2 *Feature Set & HW-BOM*

2.1 **RVP Landing Zone**

RVP Landing Zone can be viewed in SharePoint site for the WCL RVP [here](#)

2.2 **Platform HW BOM**

The platform HW BOM is being defined at this point and will be provided at the below HSD-ES links.

[WCL Platform HW BOM](#)

2.3 **Platform Validation Configuration**

The platform validation configurations can be found in the below link.

WCL Validation configuration [link](#)

3 General Architecture

3.1 Platform Block Diagram

The functional block diagram of the system with all the interface routing and connectivity options are presented in Figure 1 and Figure 2. All the major interface options are mentioned in the figure. The validation hooks are not illustrated in the figure but will be covered in the design. The details of the validation hooks provided are covered in the respective sections.

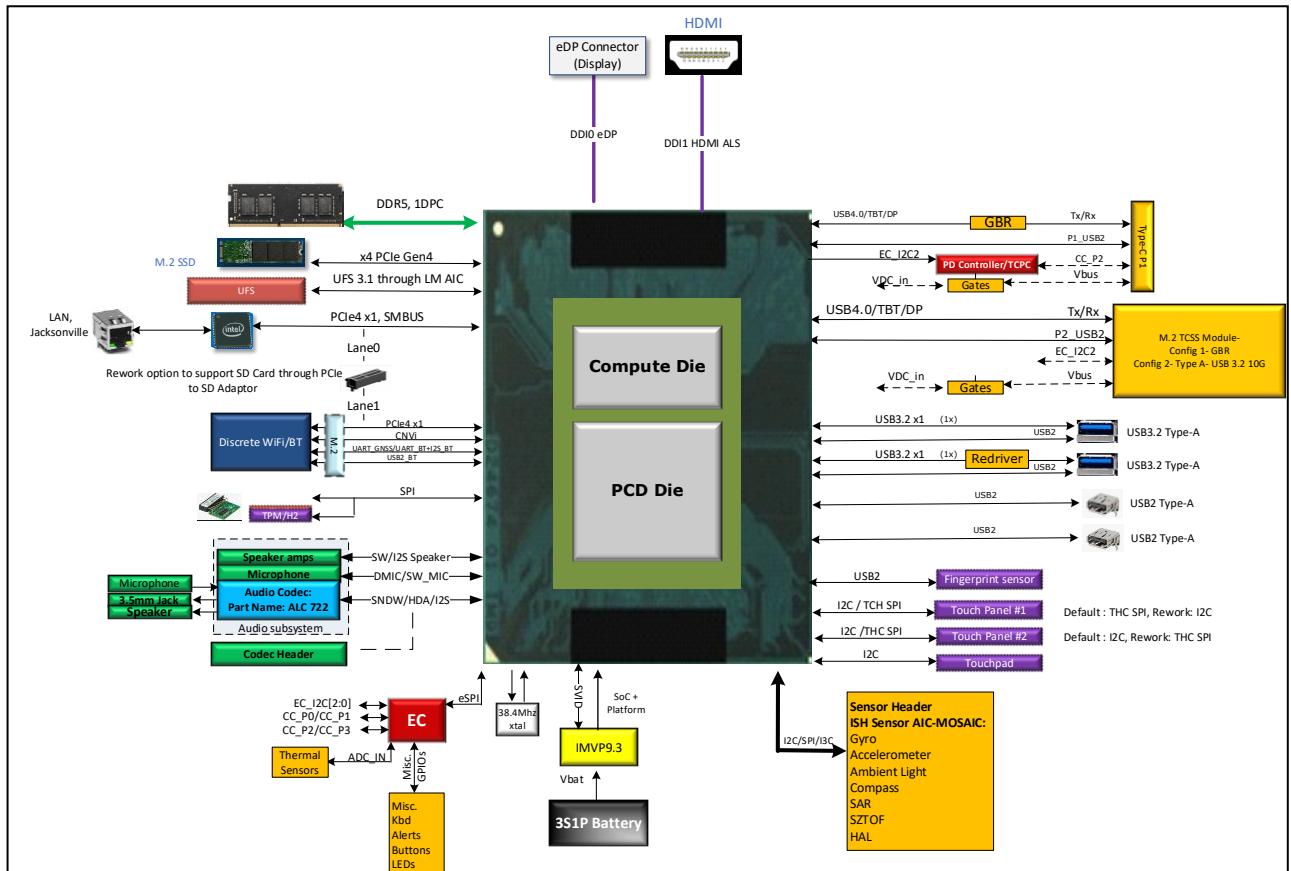


Figure 1 : RVP1 WCL T3 DDR5 RVP Block Diagram

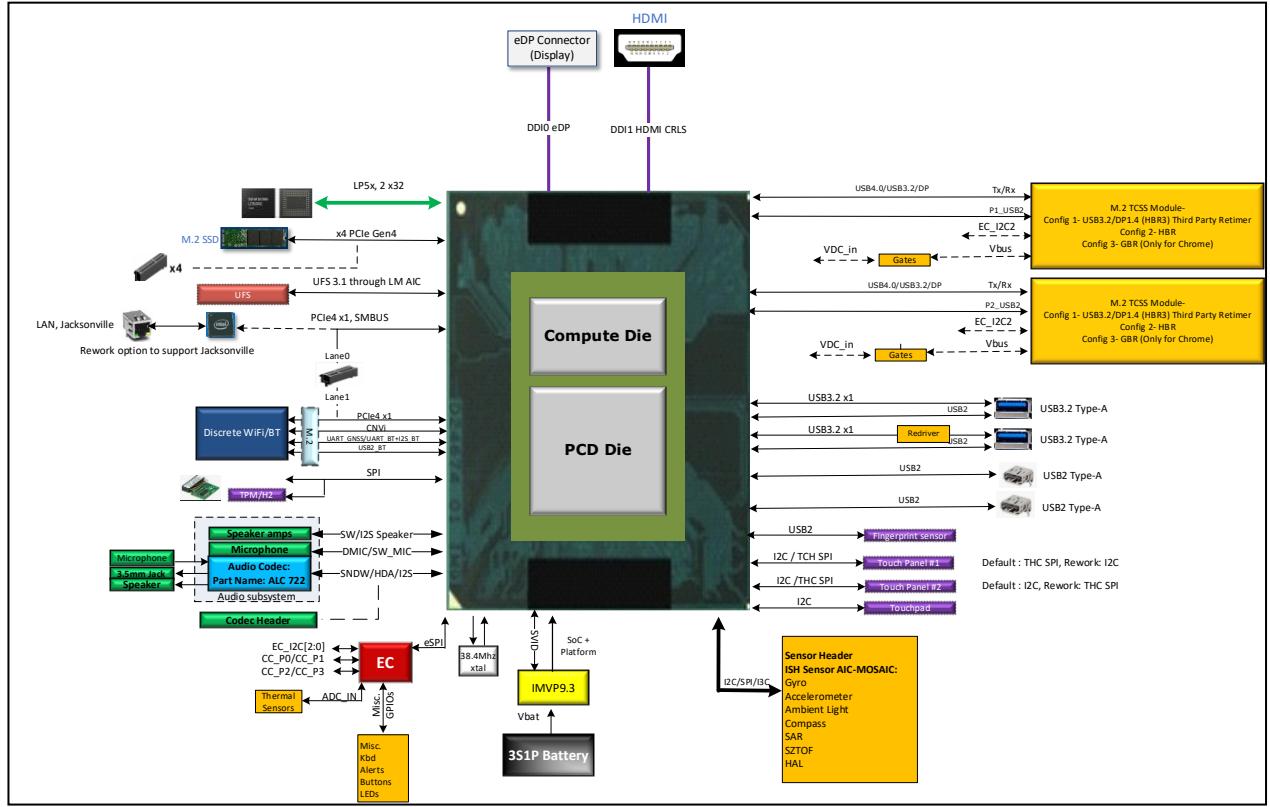


Figure 2 : RVP2 WCL T3 LP5x RVP Block Diagram

3.2 Wildcat Lake SoC Overview

WCL is a 2-die architecture, Compute Die (CDIE) and PCD die. PCD stands for Peripheral Controller Die and it contains all the traditional client IPs. WCL is first client platform to use UCIe to connect PCD to Cdie.

WCL's core architecture includes: PCore: Cougar, ECore: Darkmont, GFX XE3 Architecture and NPU architecture.

For more details, please refer [WCL SoC Overview HAS](#) and [WCL Product Specification HAS](#).

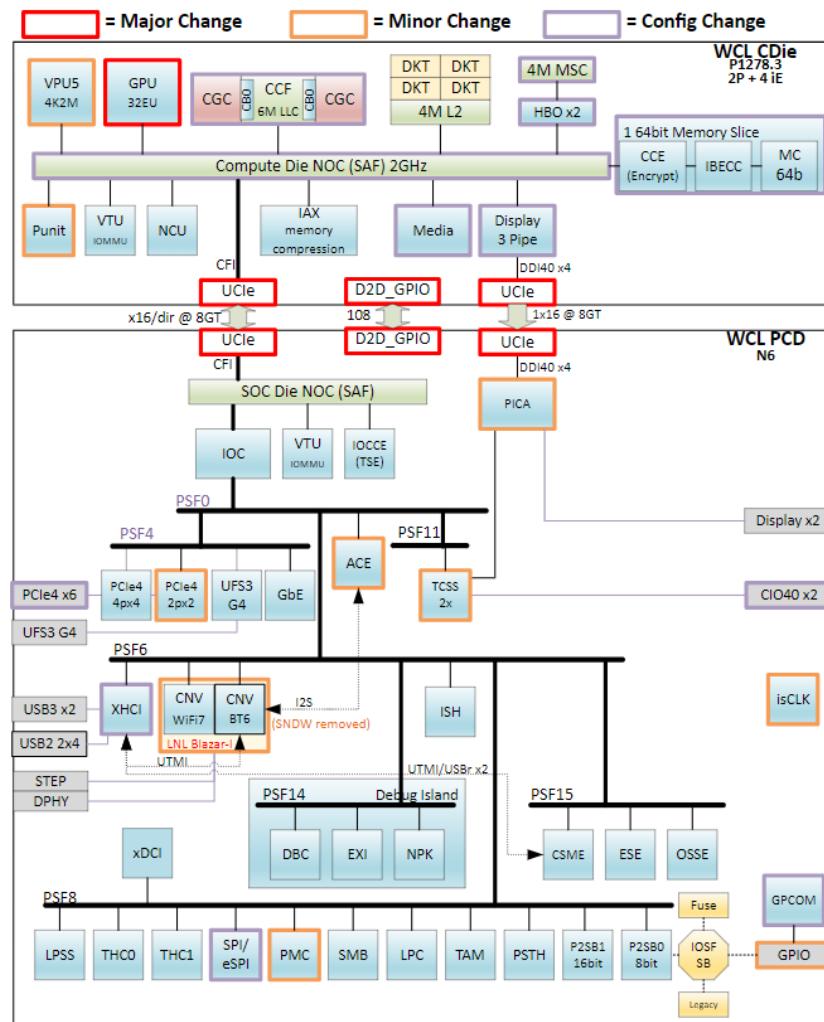


Figure 3 : WCL SoC Block Diagram

3.3 WCL RVP Platform SoC/ Interface Support Overview

WCL RVP supports WCL socketed down on the board. All the CPUs will be supported by WCL RVP design.

Table 3 : WCL RVP Supported CPU TDP Characteristics

Die Package	Product	TDP
WCL	2+4	15W
WCL	1+4	15W
WCL	0+4	15W

The major platform interface supported on the WCL RVP apart from debug, sideband and GPIO are listed below.

Table 4: WCL SoC/ RVP platform interface support summary

Interface	WCL RVP's
Memory	DDR5/LP5x
eDP/ DDI	1x4 eDP1.5b (HBR3)
HDMI	1x HDMI2.1b (6Gbps TMDS)
Concurrent Dual eDP Display	N/A
USB Type C	2 ports CIO40: USB4.0 + TBT4 + DP 2.1 (HBR3)
PCIe	X6 Gen4 (2 root port)
GbE (Muxed PCIe)	1x 1GbE Port (muxed with PCIe Gen4 port)
USB3.2 Gen2x1 10G	2 ports
UFS	1x2 UFS 3.1 Gear 4
USB2	8 ports USB 2.0
CNV (WiFi / BT)	Blazar-I WiFi7R2, BT6.x
SPI Interface	1 CSME SPI 2 THC SPI
Audio	1 HD-A 3 I2S 4 SoundWire 2 DMIC Interfaces
eSPI	eSPI with 2 chip select signals
LPSS	6 I2C Ports 2 I3C 2 GSPI/THC Ports 3 UART Ports
ISH	3 I2C Ports 1 SPI Bus 2 UART Ports 12 GPIOs
Thermal DIODE	PCH Thermal Diode
MLINK	1 Channel with CLK, DATA & RST
Integrated Clock Controller (ICC)	6 SRC Clocks 6 SRC Clock Req
SMBUS / SMLINK	2 SMLINK 1 SMBUS

3.4

Form Factor

The WCL RVP will follow a 7.35inch x 11.1inch form factor with 12 Layer PCB. Please refer to the Mechanical chapter for more details.

Generic Implementation Notes

- GND vias are spread across the board on both top and bottom sides, with clear marking on silk screen will be provided.
- All the socket caps will be specified in the schematics and can be removed in the customer version of the schematics or board.
- RVP design will follow the PDG for routing of all traces.
- All the LED will be placed on the TOP side and will be visible.

Note: Text highlighted in yellow color will be updated in subsequent versions of this RVP HAS document

4 Main Memory

4.1 Memory Controller

The WCL memory subsystem supports DDR5/LPDDR5/LPDDR5x memory technologies. RVP SKU memory configuration support would be as follows.

Table 5 : Memory Support for various RVPs

RVP SKU #	Config	Internal POR Transfer Rate (MT/s)	External POR Transfer Rate (MT/s)	Memory Device	Routing Topology	Supported Memory density		PCB Stack-Up / Routing Layer
						Min	Max	
RVP1 T3	DDR5 SODIMM	2R 7200	2R 6400	SODIMM	Point to Point	8GB	64GB	T3/6L 2 Layers
RVP2 T3	LPDDR5/x Memory Down 2x32	2R 7200	2R 6800	315 BGA	Point to Point	4GB	48GB	T3/6L 2 Layers

4.2 Memory Device BOM options

The following tables provide the Manufacturer Part number supported on WCL. The below table is based on initial HAS release. Contact MIO Team for the latest memory parts validated on the platform.

Refer to Platform BOM HSD Link for more details.

Table 6: Preferred Part List - Memory

Memory Type	Package	Manufacturer Part Number (Intel Part Number)	Speed (MT/s)	Module/DRAM density	Memory Config	Mfg
DDR5 SODIMM		TBD				
LPDDR5x		TBD				

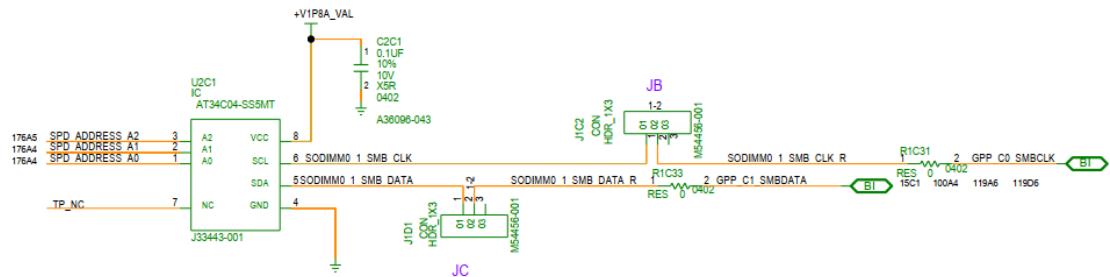
4.3 Memory SPD

Memory SPD (Serial presence detect) is a standardized way to automatically access information about a memory module or device. Refer Link of SPD Repository [SPD Files - BIOS Group BKMs - Intel Enterprise Wiki](#).

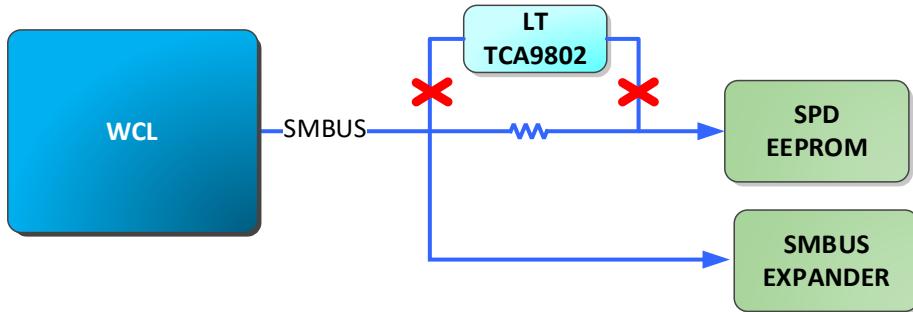
Table 7: Memory SPD info

RVP SKU #	Config	SPD
RVP1 T3	DDR5 SODIMM 1DPC	On the module
RVP2 T3	LPDDR5x Memory Down	BIOS Hard Coded/ SPD EEPROM ON RVP

Example Schematics Snapshot for SPD EEPROM;

**Figure 4 : LP5x Memory Down SPD EEPROM Schematic**

Scheme for voltage level translation for SPD EEPROM.

**Figure 5 : SPD EEPROM level translation option**

SPD present signal will be given on DIP switch instead on jumper for customer's convenience. The Level translator is optionally given in case VIL issue observed with SMBUS when interfacing with SPD EEPROM.

4.4 Routing Topology

This section deals with the routing topology to be adopted for DRAM routing on WCL RVP boards.

4.4.1 Topology for DDR5

DDR5 SODIMM routing on WCL will be point-to-point routing for all the DDR5 signals.

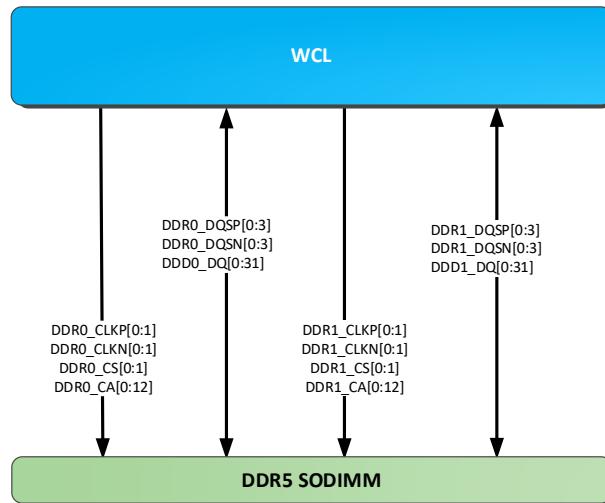


Figure 6 : DDR5 SODIMM Routing Topology for RVP1

Bit/Byte Swapping Rule:

- Bit swapping is allowed within each Byte for all memory technologies.
- DDR5: Byte Swapping is allowed within each x32 channel.
- ECC bits swap is allowed within ECC byte / nibble: DDR5 ECC[3..0].

4.4.2 Topology for LPDDR5x MB Down

The Address & command signals are routed with point-to-point topology with Data and Strobe signals in LP5x topology. This x32 device is common for T3 and T4 RVPs, illustrated in the figures below.

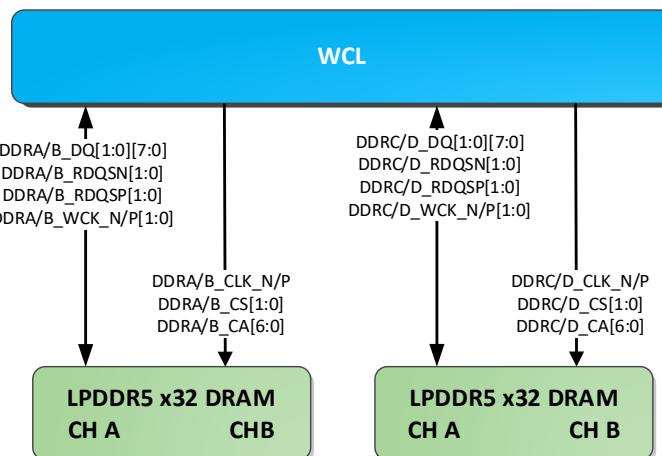


Figure 7 : LP5x Memory Down Routing Topology for RVP2

Bit/Byte Swapping Rule:

- Bit swapping is allowed within each Byte for all memory technologies.
- Byte swapping is allowed within a 16-bit channel.
- LPDDR5: x16 sub-channels can be swizzled within their x64 MC.
- When swapping channel DQ, the CA/CS signals must be swapped as well.

5 Display

There are 2 types of Display PHYs on WCL which are C10 PHY and C20 PHY. C10 PHY support 2 display ports in WCL which are DDIA with eDP 1.5/HDMI 2.1b TMDS and another dedicated DDIB port with HDMI2.1b TMDS only whereas the C20 PHY support TCSS display with DP-Alt mode. WCL only supports 3 pipes display with a maximum 4Kp60 HDR output for both internal and external.

5.1 Display Topology

There are two DDI ports on the CPU.

5.1.1 WCL RVP Display Topology

Refer to below table and block diagrams for WCL RVP's eDP/DDI display port configuration.

Table 8 : WCL RVP's eDP/ DDI port display configuration

Silicon Interface	RVP1: WCL DDR5 SODIMM RVP	RVP2: WCL LP5x MD RVP
DDIA (Default)	eDP 1.5 Panel Conn	eDP 1.5 Panel Conn
DDIA (Rework)	HDMI 2.1b TMDS compatible connector with ALS (Non-POR, for NEX Only)	NA
DDIB (Default)	HDMI 2.1b TMDS compatible connector with ALS	HDMI 2.1b with CRLS
DDIB (Rework)	NA	NA

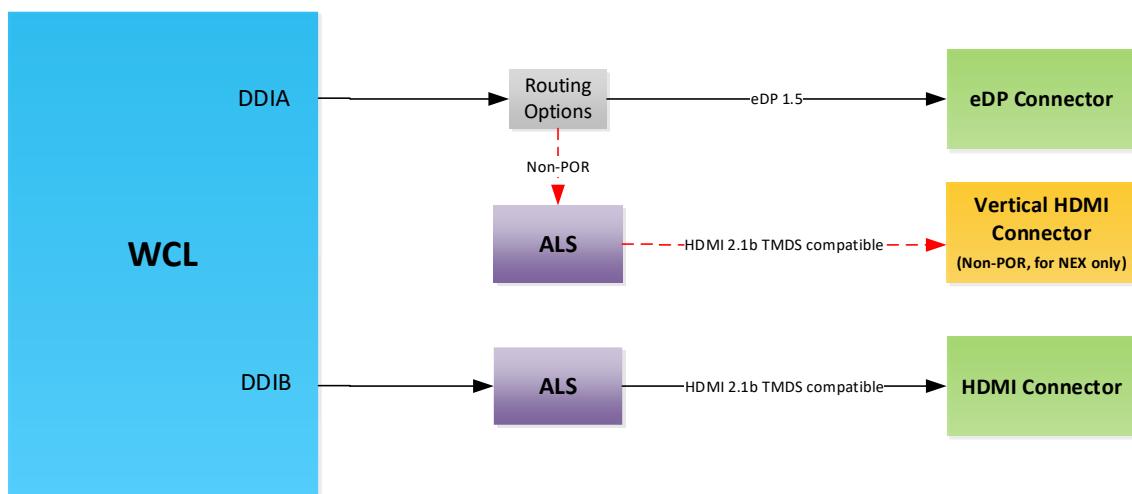


Figure 8 : WCL DDR5 SODIMM RVP1 display block diagram

Note: The DDIA rework option is only applicable for NEX team validation. All SW/ FW/ Validation/ Enablement activity to be owned by NEX team.

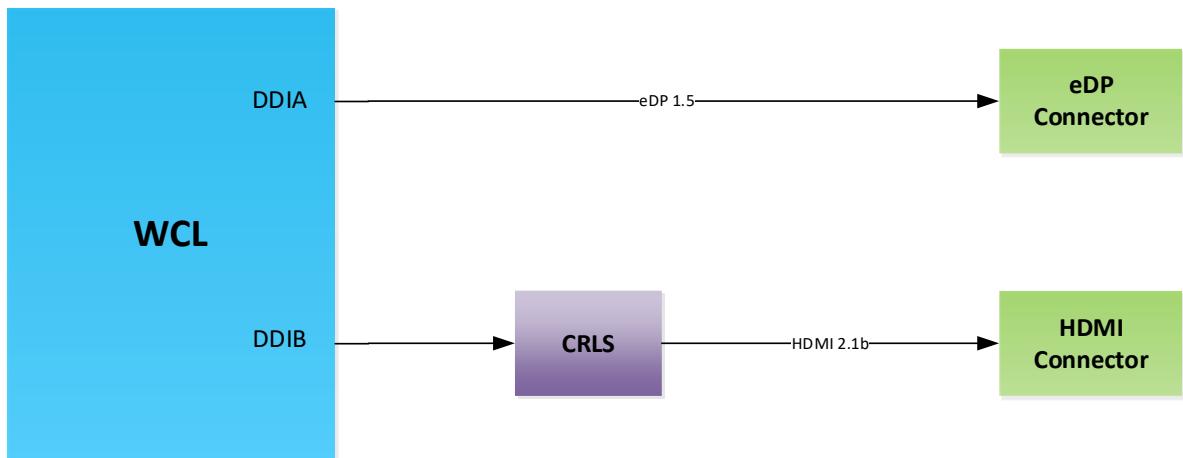


Figure 9 : WCL LP5x MD RVP2 display block diagram

5.1.2 OLED Panel Support

OLED panels are supported using OLED PMIC AIC to provide the required power changes. A cable from eDP 60-pin connector on RVP to be connected to OLED PMIC AIC. The output from that AIC will be connected to the OLED panel using another eDP 60-pin cable.

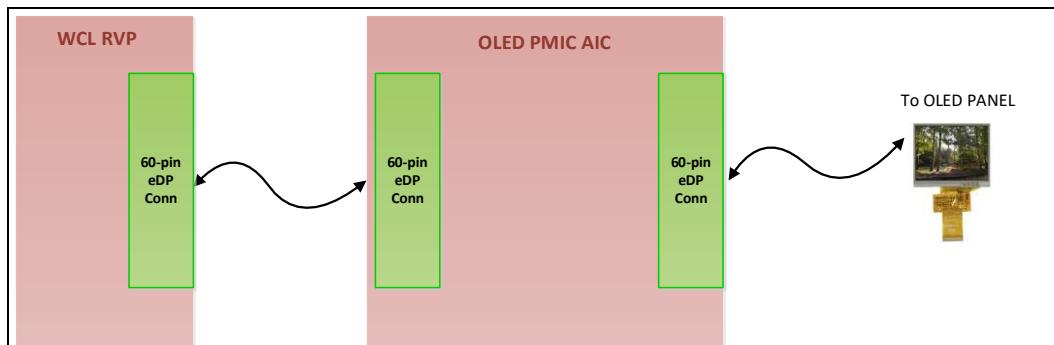


Figure 10 : OLED PMIC AIC support

5.2

Display Topology from TCSS ports

Type-C PHY on WCL supports TBT displays but doesn't support eDP muxing and native HDMI/DP. Type-C PHY can be used as alternate mode for DP on a physical Type-C port but can't be used as a dedicated DP or HDMI port with a DP or HDMI native connector. Refer to Type-C & Thunderbolt section for more details on the same.

Please refer to the Type-C section for the TCSS port mapping and block diagram for the various display topologies supported from TCSS ports.

5.3

3rd Party display re-driver support details.

Below table shows the 3rd party display re-driver device support list in WCL RVP's.

Table 9 : Display 3rd party devices support list

Device Name	MPN	IPN
HDMI 2.1 Redriver	PI3HDX1204CZHEX	M47631-001
Analogix PD and Redriver Integrated	ANX7495FN-AA-R	N44928-001
Texas Instrument (TI) – Redriver. (Used on TCSS Module, not on RVP)	TUSB1044IRNQT	K67220-001

5.4

DG Support

WCL RVP will **NOT** be supporting any third-party graphics card and DG MRB AIC.

6 Type-C & Thunderbolt

WCL supports integrated Type-C ports, supporting DP2.1 (HBR3), USB3.2, TBT3, TBT4 and USB4 protocols. The following figure shows functional block diagram of the Type-C ports on the WCL SoC. The block diagram is a super set implementation of RVP SKUs.

6.1

WCL RVP TCSS port configuration details

Refer to below table and block diagrams for the WCL RVP's TCSS Type-C and display port configuration.

Table 10 : WCL RVP's TCSS Type-C and display port configuration

Silicon Interface	Platform config requirement (all inputs)	RVP1: WCL - T3 PCB - DDR5 SODIMM	RVP2: WCL - T3 PCB - LP5x MD
TCP0 MB Short length	Type C USB4.0 / Thunderbolt Support Options: 1. TBT4 40G w/ single re-timer 2. USB4 20Gbps with single re-timer 3. USB4 20Gbps re-timerQ less (includes USB3/DP) 4. USB3/DP(HBR3) retimerless 5. TBT4 40G w/ Dual re-timer 6. TBT4 40G w/ cable topology 7. Discrete Barlow Ridge - Native DP2.1 UHBR20 retimerless FFC. 8. TypeC Port - USB/DP- 3rd Party 9. Type-A Con USB 3.2 Gen2 x1 10G without Redriver (from TCSS)	Config 1: M.2 Modular TCSS: USB-C Retimer Module. (Gothic Bridge Retimer)	Config 1: M.2 Modular TCSS: Third Party, Type C port - USB3/DP2.1 (HBR3) - Retimerless
		Config 2: M.2 Modular TCSS: Type-A Con USB 3.2 Gen2 x1 10G w/o Redriver	Config 2: M.2 Modular TCSS - TBT 40G Single Re-Timer. (Single Retimer HBR)
			Config 3: M.2 Modular TCSS: TBT 40G Single Re-Timer. (Gothic Bridge Retimer)
TCP1 MB Long Length	Motherboard Down Type C port - TBT 40G Single Re-Timer. (Single Retimer GBR Motherboard down)	Config 1: M.2 Modular TCSS: Third Party Redriver - USB3/DP 2.1 (HBR3) (Third party - Texas instrument and Analogix)	
			Config 2: M.2 Modular TCSS - TBT 40G Single Re-Timer. (Single Retimer HBR)
			Config 3: M.2 Modular TCSS: TBT 40G Single Re-Timer. (Gothic Bridge Retimer)

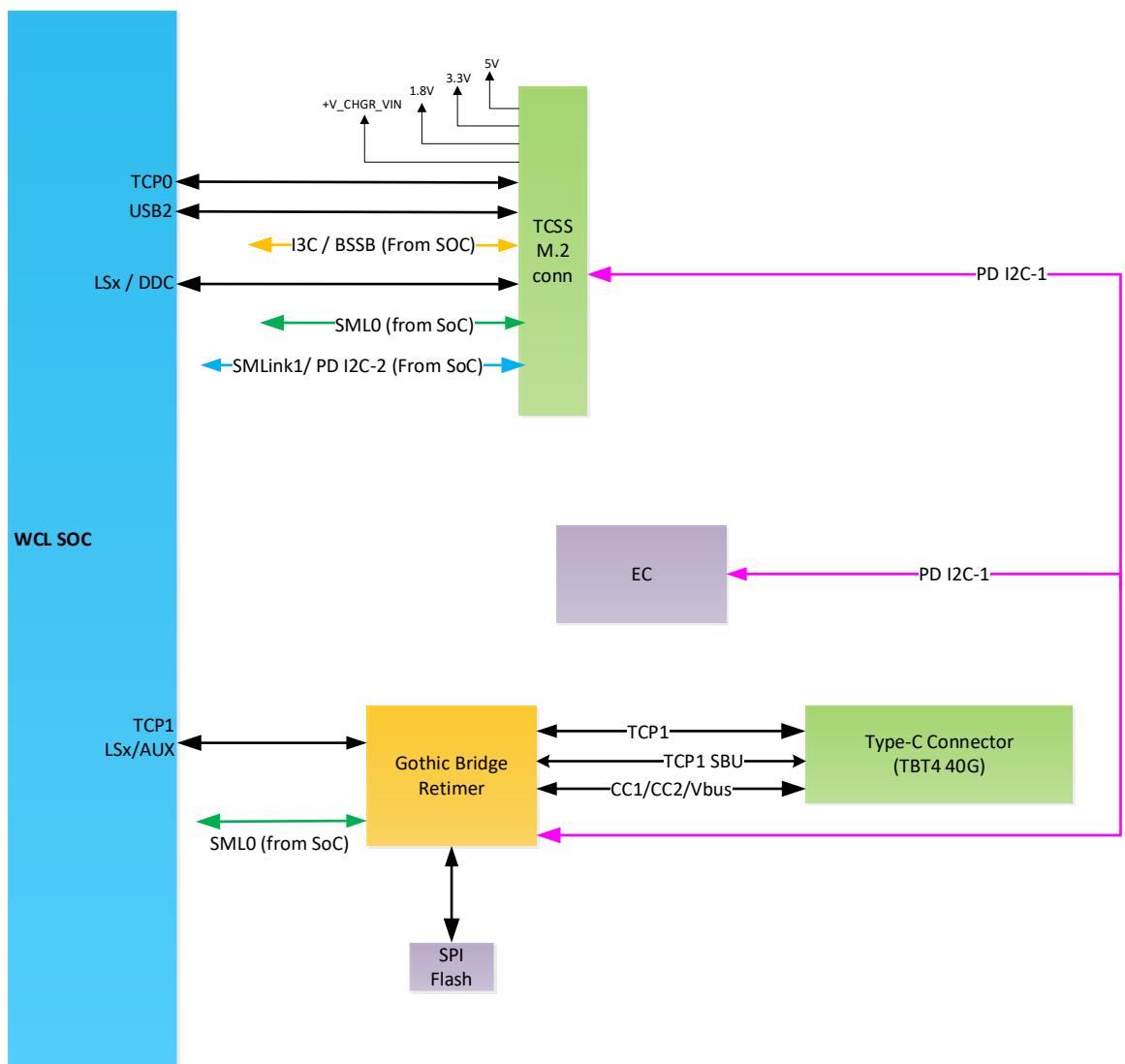


Figure 11 : WCL DDR5 SODIMM T3 RVP TCSS and Display high level clock diagram

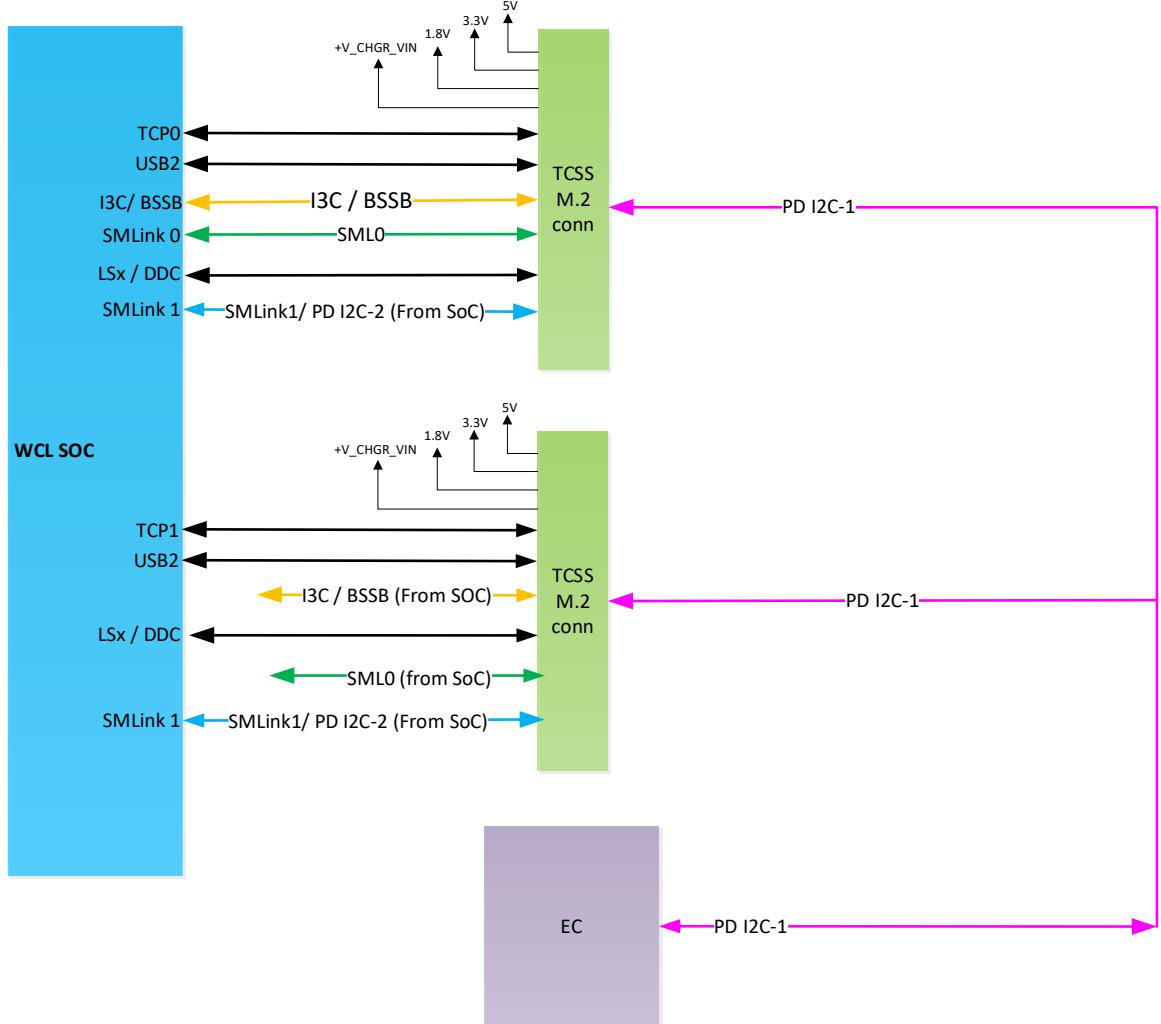


Figure 12 : WCL T3 LP5x RVP TCSS and display high level block diagram.

Note:

1. The port assignment & configuration may be changed as per layout feasibility.
2. The TCSS support only SPR on WCL, there is no EPR supported.
3. There will be no flash sharing supported between TCSS ports.
4. No PD AIC supported in WCL in both RVP SKUs.

6.2

Modular TCSS AIC support

Type-C IO components are generally placed on the motherboard. For each variety of IO requirements based on the SKU, separate efforts in terms of electrical, mechanical and development and validation efforts are needed. RVP supporting these configuration needs to support nearly 20+ configuration as Type-C validation topologies. This results in multiple RVP construction and reworks for each configuration.

Modular approach tends to reduce these efforts significantly and reduce the number of RVP configurations needed. Modular TCSS AICs have been developed to validate different configurations of ports (Type-C / HDMI / DP / USB3 (Type A) / eDP) without the need for building dedicated RVPs to support these configs, thereby, reducing the number of RVPs required and save on integration and validation cost. One RVP can support all Type-C validation. Modular TCSS AIC is a new feature being intercepted from PTL and carry forwarded on WCL platforms.

To enable modularity on RVP, the TBT /USB4 lanes from the SoC needs to be used as the data link for the different IO port requirements (TBT / USB-C / Type-A / DP / HDMI). The IO ports can be incorporated into a separate module which come in a specific formfactor (such as 30x30 mm here). With different modules, the system feature set can be varied according to the segment requirements. Based on IO requirements, different modules can be ordered and validated.

On WCL RVP, following table lists down the POR modules for different WCL RVP SKUs.

Table 11 : Modular TCSS AICs support on WCL RVP SKUs

TCP Ports	RVP SKUs	
	RVP1: WCL - T3 PCB - DDR5 SODIMM	RVP2: WCL - T3 PCB - LP5x MD
TCP0	Config 1: M.2 Modular TCSS: USB-C Retimer Module. (Gothic Bridge Retimer)	Config 1: M.2 Modular TCSS: Third Party, Type C port - USB3/DP2.1 (HBR3) - Retimerless
	Config 2: M.2 Modular TCSS: Type-A Con USB 3.2 Gen2 x1 10G w/o Redriver	Config 2: M.2 Modular TCSS - TBT 40G Single Re-Timer. (Single Retimer HBR)
		Config 3: M.2 Modular TCSS: TBT 40G Single Re-Timer. (Gothic Bridge Retimer)
TCP1	Motherboard Down Type C port - TBT 40G Single Re-Timer. (Single Retimer GBR Motherboard down)	Config 1: M.2 Modular TCSS: Third Party Redriver - USB3/DP 2.1 (HBR3) (Third party - Texas instrument and Analogix)
		Config 2: M.2 Modular TCSS - TBT 40G Single Re-Timer. (Single Retimer HBR)
		Config 3: M.2 Modular TCSS: TBT 40G Single Re-Timer. (Gothic Bridge Retimer)

Note:

- (a) Multiple configurations of modular TCSS AICs (such as TBT / USB Type-A/DP2.1(HBR3)) are available.
 - a. All these modular TCSS AICs are interchangeable on TCP0 and TCP1 ports (except for TCP1 of RVP1 SKU).
 - b. The above table lists the POR modules as per landing zone and does not restrict the usage of other modules.
 - c. All modular TCSS AICs are ‘plug and play’.
- (b) The eDP modular AIC is not support over M.2 Modular Type C port of any RVP Sku’s.

For more details on modular TCSS AICs and user guide, please refer below link:

<https://goto/tcssmodule>

User Guide : [LINK](#)

6.2.1 List of POR TCSS Modules

The list below shows the POR TCSS modules planned on WCL RVP

Note: Please refer <https://goto/tcssmodule> for the updated information

Table 12 : POR TCSS modules on WCL RVPs

Module Name	Module Class	Module No.	TA No.	Volume
TBT-40G HBR Retimer, TI-PD Module	100	103	N17292-100	Y
Type-A Redriver less Module	600	600	N24545-100	N
TBT-40G Gothic Bridge Module	TBD	TBD	TBD	N
TI PD, Retimerless USB3/DP2.1(HBR3) Type C	TBD	TBD	TBD	N
ANX PD, Retimerless USB3/DP2.1(HBR3) Type C	TBD	TBD	TBD	N
TI Redriver, USB3/DP2.1(HBR3) Type C	TBD	TBD	TBD	N
ANX Redriver, USB3/DP2.1(HBR3) Type C	TBD	TBD	TBD	N

6.3 Discrete TBT Barlow Ridge support

WCL RVP1 and RVP2 does not support Discrete TBT Barlow Ridge.

6.4 BSSB/I3C debug

6.4.1 I3C debug impact

The debug mode is entered through debug Accessory mode and the Analog Mux switching is handled by the PD controller. I3C/BSSB closed chassis debug feature on Type-C will only be provided on TCP0 port.

6.5 TBT Repeaters Support

- The SoC output is a muxed port that supports TBT4/DP2.1(HBR3)/USB3.2/USB4 protocols. PCIe is not supported as native or alternate mode.
- To support TBT protocol at 40Gbps, TBT retimer is implemented on the path. Each integrated TBT type-C port requires a retimer in WCL RVP. Aux/LSx signals are routed to the retimer where they are muxed internally.
- Hayden Bridge (HBR)/ Gothic Bridge(GBR) multiprotocol retimer is used on WCL RVP. Due to SI impact and high cost, retimer socket support is not provided on RVPs.

- SMBus would be connected to SML0 of SOC for vPRO support over TBT dock and shared with LPSS I2C (for one USBC port) for support programming of retimer in USB/DP only mode.

6.5.1

Hayden Bridge Retimer (HBR)

Hayden Bridge is a Type-C multi-protocol retimer to be used in on-board applications.

Hayden Bridge offers the ability to latch protocol signals into on-chip memory before retransmitting them onwards. It can be used to extend the physical length of the system without increasing high frequency jitter.

Hayden Bridge supports spec compliant retimer of following protocols:

- Display Port: four unidirectional DP lanes
- USB3.2 Gen1/2: two bi-directional USB lanes
- Thunderbolt/USB4: two bi-directional USB4 lanes
- Multifunction Display (MFD): two unidirectional lanes of DP and one bi-directional lane of USB3.2 Gen1/2

Few Features and limitations on HBR:

- Hayden Bridge device is not a symmetrical retimer. Its port B side should be always facing toward the Type-C device.
- Hayden Bridge cannot be used in multi-master applications
- Hayden Bridge doesn't implement high speed lane crossing function
- The pin type is defined to be fail-safe when it is designed to sustain voltage without current flowing into it, when there is no external power provided to the re-timer.
- Flash (1.8V, at least 50MHz clk) can be updated either through LSx or SMBUS interface.
- When operating in Bypass mode, no cable orientation supported, so BSBU1 pin will be always connected to LSTX_SBU1 pin and BSBU2 pin will be always connected to LSRX_SBU1 pin.
- High Speed Interface Insertion Loss
 - SoC to re-timer channel: 17dB@10GHz
 - Re-timer to Type-C connector channel: 4.5dB@10GHz (+ 0.5dB@10GHz for the type-C receptacle).
 - Re-timer to re-timer channel (for dual re-timer mode): 15dB@10GHz

6.5.1.1

Hayden Bridge I2C Addressing

Hayden Bridge supports standard I2C interface. It is used for communication between the internal link controller and PD controller on the M.2 Modular TCSS AIC.

The slave address of Hayden Bridge is configured through re-timer NVM. There are four supported configurations in each NVM. The selection between the address is done by POC_GPIO_7 and POC_GPIO_11 according to the below configuration:

Table 13 : Hayden Bridge I2C addressing

I2C Address	POC_GPIO_7	POC_GPIO_11 (master / slave)	HBR#
0x57	0	0	HBR#TCP0
0x56	0	1	HBR#TCP1

POC_GPIO_7 is I2C address select pin in HBR, while POC_GPIO_11 is a master / slave select strap pin in flash sharing mode.

Please refer below figure for more details on HBR numbering and I2C address correlation.

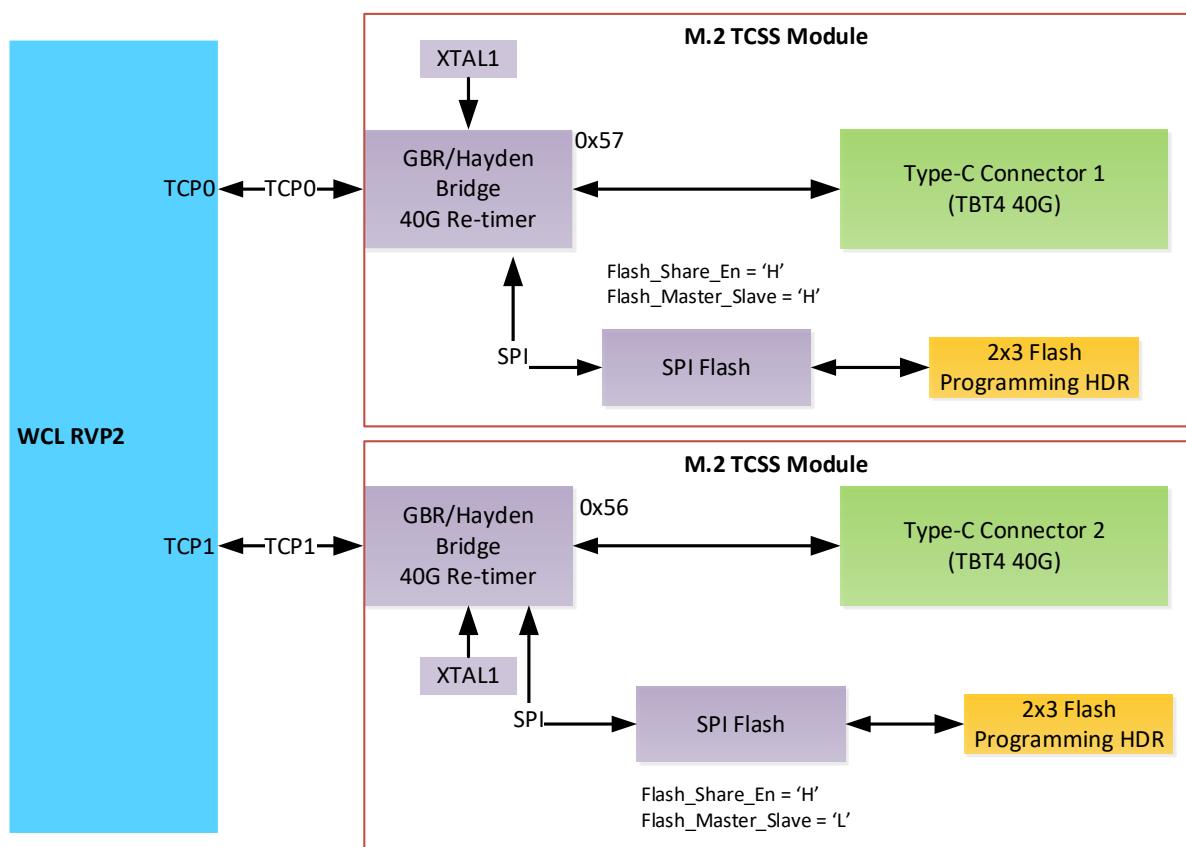


Figure 13 : I2C addressing scheme for GBR / Hayden Bridge re-timers

6.5.2

Retimer Flash Sharing

WCL RVP doesn't have Flash sharing for any of the Retimer supported in WCL RVP1 and WCL RVP2 SKU's.

SF100-dediprog header shall be provided for shared Flash initial programming. Below are the details of Dediprog Header.

- 1.27mm pitch 2x3 header is provided on RVP.
- Need Universal Adapter board and cable for programming - <https://www.dediprog.com/product/ISP-ADP-127>
- Cable as 2x4 header and Last two pins are NC in it. Hence leave last two pins unconnected and connect just 6 pins as below.
- Flash to be programmed in **RVP powered OFF**, Dediprog will be Master and 1.8V from the Dediprog shall be used on RVP



This FW programming needed only when the TBT interface is not up (initial stages of bring-up). Once the TBT interface is up and working, programming through a host is possible.

Alternatively, unstuffed independent Flash footprint will be provided for the Slave retimer when flash is shared on the board.

6.5.3

Legacy Display ports Support

- RVP doesn't support native HDMI connector over modular TCSS HDMI AIC.
- Secondary eDP is not supported over TCSS.
- Native DP ports are not supported on WCL RVP.
 - Only DP alt / tunneling mode is supported on type-C ports.

6.6

PD Controller Support

There is no motherboard down Standalone PD controller on WCL SKUs. WCL RVP1 support the Motherboard down config of Gothic Bridge Retimer which has the integrated PD Controller and the second port supports M.2 Modular TCSS. WCL RVP2 Modular TCSS AICs are supported on both ports. The TBT modular TCSS AIC has on board PD controller. WCL RVP2 also supports the low cost third party TCSS solution from Analogix and Texas Instruments.

M.2 Modular TCSS Port controller (TCPC) is only supported on Chrome WCL RVP SKU. Refer to [Chrome Requirements](#) section for more details.

6.6.1 On Board PD Controller

Not supported on WCL SKUs

6.6.2 Power Delivery Add-In-Card (PD AIC) Support

There is no PD AIC support on WCL RVP Sku's. WCL RVP supports only motherboard down GBR Retimer and M.2 Modular TCSS AIC.

6.6.3 SPR and EPR AIC support on WCL

On WCL platform, Type C ports TCP0 and TCP1 will support only SPR(20V) mode in both RVP1 and RVP2. There is no EPR (28V,48V) support in WCL platform.

6.6.4 PD Controller Communication

- PD controller communication could be over I2C or through GPIOs as below:
 - PD (slave) to PMC through USBC SML or SMlink1 Communication
 - PD (slave) to EC through I2C communication for UCSI communication
 - PD (master) to TBT retimer for configuration

6.6.5

PD and Retimer Debug Support

The WCL RVP1 having Onboard Gothic Bridge Retimer supports the below debug header on motherboard. The M.2 Modular TCSS AIC has no Header option provided on AIC instead Test points are provided for below signal debug capabilities.

- Individual JTAG headers (HDR_2X3) on all the retimers – PRESENT ON RVP
- EC to PD I2C header (HDR_1X3) – TBD
- PMC (USBC SML or SMLink1) to PD I2C header (HDR_1X3) – TBD
- Soc (SMLink0) to Retimer (HDR_1X3) – PRESENT ON RVP

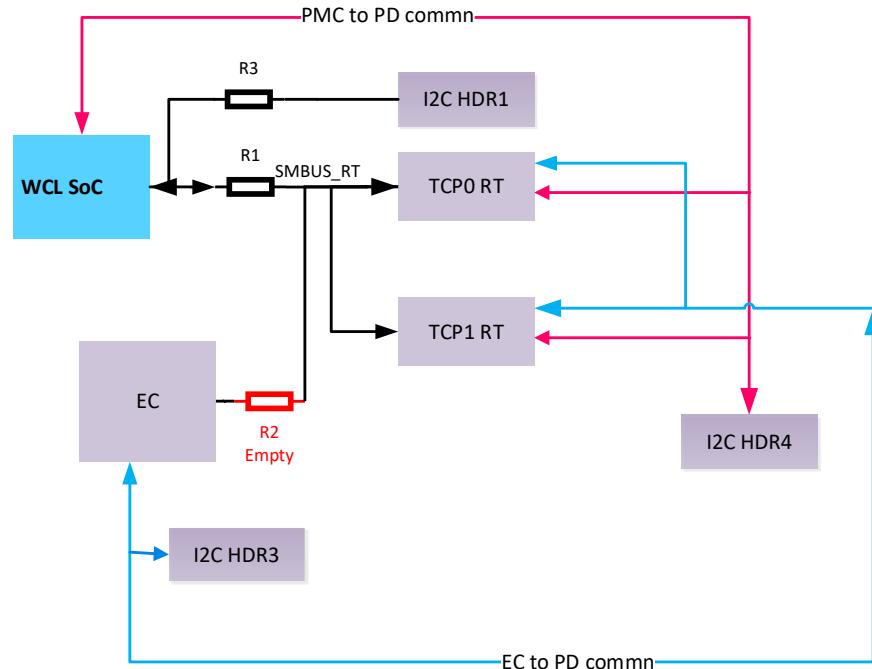


Figure 14 : PD/Retimer I2C debug headers

6.7

Download & Execute (DnX) Support

This feature allows to download and execute the content from another system over USB2.

To enter in DnX mode, the DnX forcedload GPIO should be asserted. In case of RVP, the DnX forcedload is asserted by EC based on button press. On RVP, the LED is available to indicate the DnX progress.

This is supported on lowest USB2 port number in SoC. In WCL, USB2.0 port-1 is the lowest port number from the SoC.

The USB2.0 port mapping on the type-C ports should be in incremental order, to support the device mode. The violation of the incremental order port mapping may affect the device mode operation. Refer USB section of this document for WCL RVP port mapping.

Example for correct incremental order port mapping

Table 14 : Correct incremental order for USB2.0 and TCP port mapping

TCP port number	USB 2 port number	Remarks
TCP0	USB2_1	PHY Ports Usable with TCSS IO are 1,2,5,6
TCP1	USB2_2	PHY Ports Usable with TCSS IO are 1,2,5,6

Example for incorrect incremental order port mapping

Table 15 : Incorrect incremental order for USB2.0 and TCP port mapping

TCP port number	USB 2 port number	Remarks
TCP0	USB2_2	Incorrect assignment; TCP0 is assigned with USB2_2; then USB2_1 should not be used in TCP1
TCP1	USB2_1	Incorrect assignment; TCP1 is assigned with USB2_1; then USB2_2 should not be used in TCP0

6.8

Feature list supported on WCL RVPs

The Table 16 provides the quick features list. The below table provides complete feature list supported on various WCL RVPs:

Table 16 : Various Type-C port Features in WCL RVPs

SL No	Features	Mode	RVP1: WCL - T3PCB – DDR5	RVP2: WCL – T3PCB – LP5x MD
1	Number of USBC ports		2	2
2	Power Profile - Consumer	5V-20V @ 5A	Yes	Yes
3	EPR Power Profile - Consumer	5V-48V @ 5A (WCL)	No	No
4	Power Profile – Provider (On board type-C ports)	5V @ 3A, 5V @ 1.5A. 1 port at 3A and other ports at 1.5A at a given time.	Yes	Yes
5	Power Profile – Provider (Modular TCSS AIC based type-C ports)	5V @ 3A, 5V @ 1.5A. 1 port at 3A and other ports at 1.5A at a given time.	Yes	Yes
6	POR PD controller	Modular PD AIC	Integrated GBR PD and Modular PD AIC	Modular PD AIC
7	USBC Internal cable topology	<u>5V@3A power profile</u> <u>FFC cable</u>	No	No
8	BC1.2 support for Chrome	<u>5V@1.5A provider</u>	No	No
9	Non-TBT, USB/DP direct port	DP/USB/PCIE tunneling	No	Yes
10	Native DP2.0 with Repeater	HBR3	Not POR	Not POR
11	USB3.2 redriver	USB3.2 Gen2x2	POR	POR
12	TBT - Single Retimer 40G	HB/GB retimer TBT/USB/DP	Yes	Yes
13	TBT - Retimer 20G	HB retimer TBT/USB/DP	No	No
14	Dual TBT retimer 40G	HB retimer TBT/USB/DP	No	No
15	USB4 Retimerless 20G	TBT/USB/DP	No	No
16	3 rd party redriver + TBT retimer	3 rd party Redriver + BB retimer TBT/DP/USB	No	No
17	dTBT Barlow Ridge support solder down	BR dTBT TBT/USB/DP	No	No
18	dTBT Maple Ridge + Burnside Bridge support	MR dTBT+BB TBT/USB/DP	No	No
19	DP-in (DP2.1 input) support for switchable graphics	Via dTBT Barlow Ridge Controller.	No	No

20	DP2.1 support over enhanced mini-DP connectors	DP2.1 output from SOC	No	No
21	DnX Support	DnX supported with external jumper or via EC	Yes. One port	Yes. One port
22	USBC debug support	USB3 DbC/ USB2 DbC/HTI Trace boxes ("Unitracer", "PRI7" or "VPlus")	Yes, 1 No's	Yes, 1 No's
23	USBC debug support	2-wire DCI-OOB over I3C platform mux / Debug accessory mode	Yes, 1 No's	Yes, 1 No's
24	USBC switching AIC support - Cswitch 2.0 ^v	Not supported on vertical ports.	Yes	Yes
25	USBC switching AIC support Cswitch Rev4.0 ^v	54mm spacing between Type-C (or other) Con	Yes	Yes
26	VPRO support	SML0 connection between retimer and PCH	Yes	Yes
27	Ardent connector		No	No

6.9

Chrome Connector Support

Chrome USB-C modular AIC based on TCPC shall be used for TCP0/1 ports. Refer to [Chrome section](#) for more details. WCL RVP doesn't support TCPC AIC as there is no PD AIC option provided on RVP.

6.10

Protection Circuit

Specific ESD protection diodes are provided for all the signals close to the Type C port connector. The Type-C connector has a higher pin density than legacy USB connectors. As a result, it is easier to accidentally short VBUS to adjacent pins. With the potential of having VBUS of up to 20 V, it is possible to have a short between the 20V and a 5V line (such as SBU, CC and so on). To protect against this potentially catastrophic event, VBUS short circuit protection is required. Short circuit protection on the SBU and CC lines are taken care in PD add-in card. No additional protector IC is provided on RVP board.

VBUS is also adjacent to the high differential lines, refer to the connector pinout in the Type C specification. These pins are protected using a series Resistor-Capacitor combination between the pins of the Type C connector and the chip. Refer to the Product Design Guide (PDG) document for more accurate details on the same.

7 HSIO

WCL platform supports various HSIO interfaces like PCIe Gen4, USB 3.2 Gen2x1, Gbe LAN to connect different peripheral devices from PCD Die.

7.1 WCL Platform HSIO support details

WCL PCD die supports:

1. 2x USB 3.2 Gen2x1(10G) lanes.
2. WCL PCD die supports 6 PCIe Gen4 lanes; 1 of the PCIe lane is muxed with Gbe LAN.

7.1.1 PCIe device support on WCL RVP

WCL RVP supports the following PCIe Devices/ IO connectors:

1. M.2 Key-M SSD Gen4
2. M.2 Key-E WLAN
3. WWAN [Non-POR]
4. Integrated Gbe LAN
5. x4 PCIe DT Slot1 (Open ended) – for SD 7.0 AIC
6. x4 PCIe DT Slot2 (Open ended) – RVP2 only, enable for EV & FV team

7.1.2 HSIO configurations in WCL RVP's

Based on the platform LZ, POR & platform requirement initial HSIO Mapping has been done for WCL Platform. RVP ModPHY Mapping table will be used by the soft strap team & BIOS team to configure the individual lane as per RVP recommendation. RVP Implementation will support multiple configurations by sharing the same lanes for different function, board rework and IFWI changes will be required to enable the shared feature which has different function.

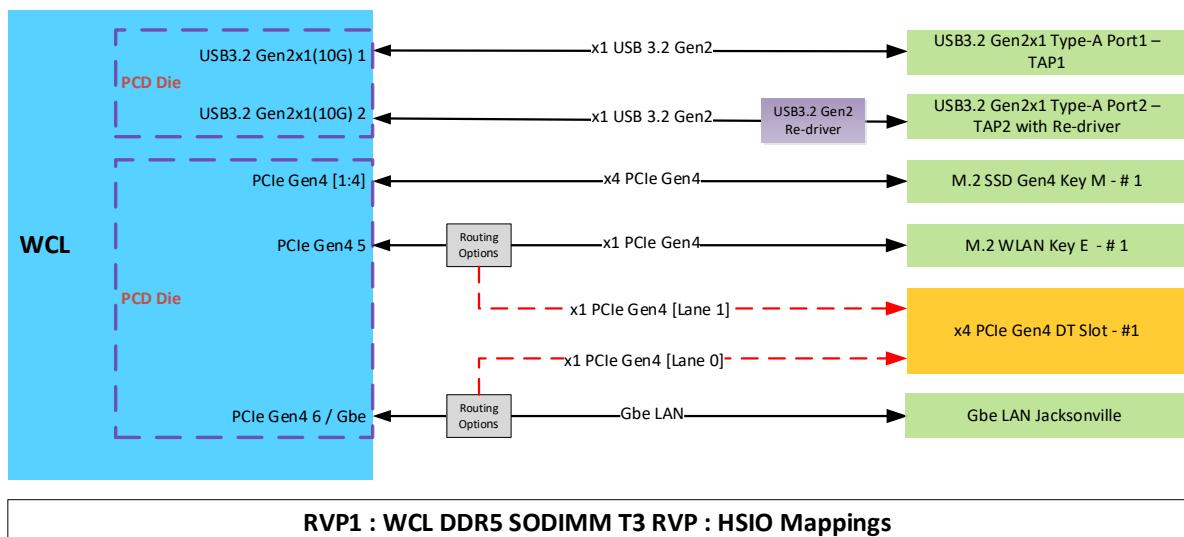
Table 17 : HSIO support on WCL Platform

Die	Port #	WCL HSIO ports				
		USB 3.2 10G	Gbe LAN	PCIe	PCIe Port Configs	
PCD Die	USB3.2 Ge2x1(10G) 1	Yes				x1
	USB3.2 Ge2x1(10G) 2	Yes				x1
	PCIe Gen4 1			Yes	x4	x2
	PCIe Gen4 2			Yes		x1
	PCIe Gen4 3			Yes	x2	x1
	PCIe Gen4 4			Yes		x1
	PCIe Gen4 5			Yes	x2	x1
	PCIe Gen4 6 / Gbe	Yes	Yes			x1

Table 18 : HSIO Mapping on WCL RVP's

WCL HSIO ports		RVP1: WCL - DDR5 SODIMM 1DPC T3		RVP2: WCL - LP5x Memory Down T3	
Die	Port #	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)
PCD Die	USB3.2 Gen2x1 (10G) 1	USB3.2 Gen2x1 Type-A Port1	-	USB3.2 Gen2x1 Type-A Port1	-
	USB3.2 Gen2x1 (10G) 2	USB3.2 Gen2x1 Type-A Port2 with Re-driver	-	USB3.2 Gen2x1 Type-A Port2 with Re-driver	-
	PCIe4 1	M.2 SSD Gen4 Key M	-	M.2 SSD Gen4 Key M	x4 PCIe DT Slot #2
	PCIe4 2				
	PCIe4 3				
	PCIe4 4				
	PCIe4 5	M.2 WLAN Key E	x4 PCIe Gen4 DT Slot #1 for SD Card – Lane 1	M.2 WLAN Key E	x4 PCIe Gen4 DT Slot #1 - Lane 1
	PCIe4 6 / Gbe	Gbe LAN Jacksonville	x4 PCIe Gen4 DT Slot #1 for SD Card – Lane 0	x4 PCIe Gen4 DT Slot #1- Lane 0	Gbe LAN Jacksonville

7.2 WCL RVP : HSIO Mapping


Figure 15 : RVP1 WCL DDR5 SODIMM T3 RVP : HSIO Mappings

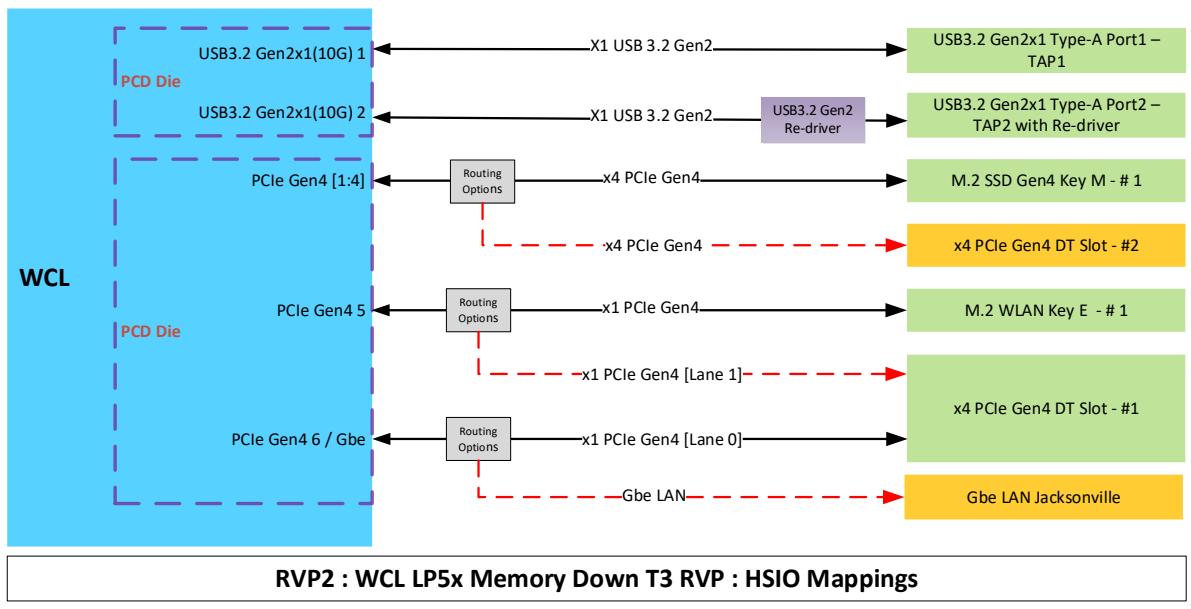


Figure 16 : RVP2 WCL LP5x Memory DownT3 RVP : HSIO Mappings

8

USB2.0

WCL PCD die supports 8 USB2.0 ports.

8.1 WCL RVP : USB 2.0 Mapping

Table 19 : WCL RVP-1 & RVP-2 USB 2.0 port mapping

USB2 Lane#	Topology 1 (Default)	Topology 2 (Rework)
USB2_P1	Type C port - various configurations – TCP0	USB2 Vertical Type-A (Only for PPV)
USB2_P2	Type C port - various configurations – TCP1	-
USB2_P3	USB2 Type-A – TAP1	-
USB2_P4	USB2 Type-A – TAP2 with Re-driver	-
USB2_P5	2x5 USB2 HDR #1 (FP)	WWAN (non-POR) – Only RVP1
USB2_P6		-
USB2_P7	FPS	2x5 USB2 HDR #2 (FP)(Only for PPV)
USB2_P8	M.2 WLAN Key E	

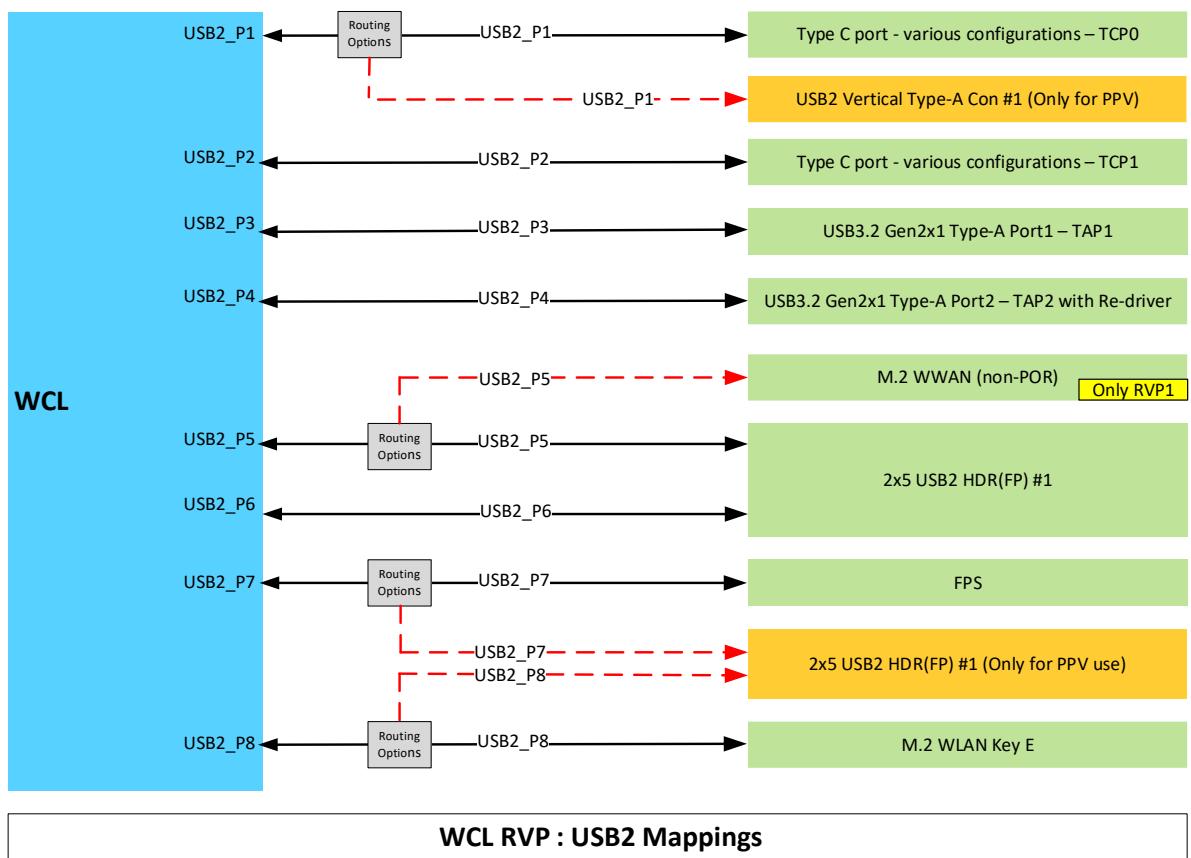


Figure 17 : WCL RVP1 & RVP2: USB2 Mappings

8.2

USB Overcurrent (OC) Protection

WCL PCD die has implemented programmable USB OC signals. 2 OC pins are to be shared across the Type-C, USB2.0 & USB3.2 Gen2x1 Type-A ports. This allows the platform designer flexibility in routing of the OC pins & allows for unused pins to be configured as GPIOs. The current limits for the USB3.2 Gen2x1 Type-A ports is set to 900mA typical.

Table 20: OC Protection from the individual OC protection controllers in WCL RVP

Pin Name	WCL Configuration
USB2_OCB_0	TBD
USB2_OCB_1	TBD

8.3

USB Signal Protection

WCL RVP shall have a CMC and ESD diodes for Signal protection.

8.4

USB Debug Support

Intel® DCI (Direct Connect Interface) is an Intel Technology that allows debug access by re-purposing a USB3.2 Gen 2x1 port. The advantage is debug functions & trace features can be connected using existing USB3 ports, rather than the usual additional connectors. It supports many debug functions & can be implemented “closed chassis”. The DCI connection supports run-control debug, validation, trace, DMA, OS Debug and scripting. DCI is implemented using 2 primary transport topologies:

- Intel® DCI.OOB (formerly BSSB)
- Intel® DCI.USB2/USB3 (formerly DbC)

Table 21: USB Debug Support on WCL RVP

Connector Details	Supported Topologies
Connector1: Type-A Walk-Up USB Port USB3.2 Gen 2x1_Port 1 & USB2_Port3	USB.DbC
Connector2: Type-A Walk-Up USB Port USB3.2 Gen 2x1_Port 2 & USB2_Port4	USB.DbC
Type C Port0: USB2_Port1	USB.DbC DCI.OOB – 2 Wire
Type C Port 1: USB2_Port2	USB.DbC DCI.OOB – 2 Wire

9

Clocks

WCL SOC is the primary clock generator for all sub-system on WCL RVP. The chipset has 2 major clock sources out of which all the sub-system clocks and external clock outputs are derived through internal PLLs. A high-level block diagram of the chipset clock interface is given below.

Table 22 : Clock Inputs on WCL

Clock Name	Description
RTCX1/ RTCX2	32.768KHz crystal input for Real time clock
Single ended Crystal RTCX1	Single-ended RTC crystal input by driving 32.768Khz CMOS clock on RTCX1 [Not used on RVP]
XTAL_IN/OUT	38.4MHz crystal input for iSCLK (integrated System Clock) block
CRF_CLKREQ	To be sent to iSCLK & CRF Quasar to Synchronize CRF & Quasar
SRCCLKREQB [5:0]	SRCCCLKREQB is used to support clock request protocol to enable or disable SRC clocks distribution to off-chip. In addition, the SRCCCLKREQB is also used for PCIe power management (L1.off, etc.).
OBS[1:0]MON_ISCLK	iSCLK monitoring pins for debug usage
SOC_REFRCOMP_ISCLK	Connected to an external precision resistor for Differential buffer, RCOMP between VSS and this pad.

Table 23 : Output signals from Clock function on WCL

Signal Name	Frequency & SSC Support	Description
GPP_V_7_SUSCLK	32.768KHz without SSC	Suspend clock that generated from the RTC crystal oscillator
CLKOUT_SOC_[0:5]_N/P	100MHz – Gen4 Capable with SSC	100MHz differential source clock for external PCIe Device
GPP_D_21_UFS_REFCLK	38.4 MHz without SSC	38.4MHz single-ended reference clock for external UFS device

WCL SOC supports 6 SRC CLK's & 6 CLKREQ signals. All SRC CLK's from SOC are Gen4 capable.

By default, CLKREQ will be enabled as Native GPIO function. To use these pins as a CLKREQ it needs to be mapped in the BIOS.

The Gbe LAN PHY needs 25MHz input which will be fed from an external crystal input. The Embedded controller has the external 32.768kHz crystal input as the default option along with SUS_CLK option driven from SOC. Any other interface specific clocks required for third party devices will be derived out of the external crystals specific to the device requirements.

9.1

WCL RVP : SRC Clock and CLK REQ Mapping

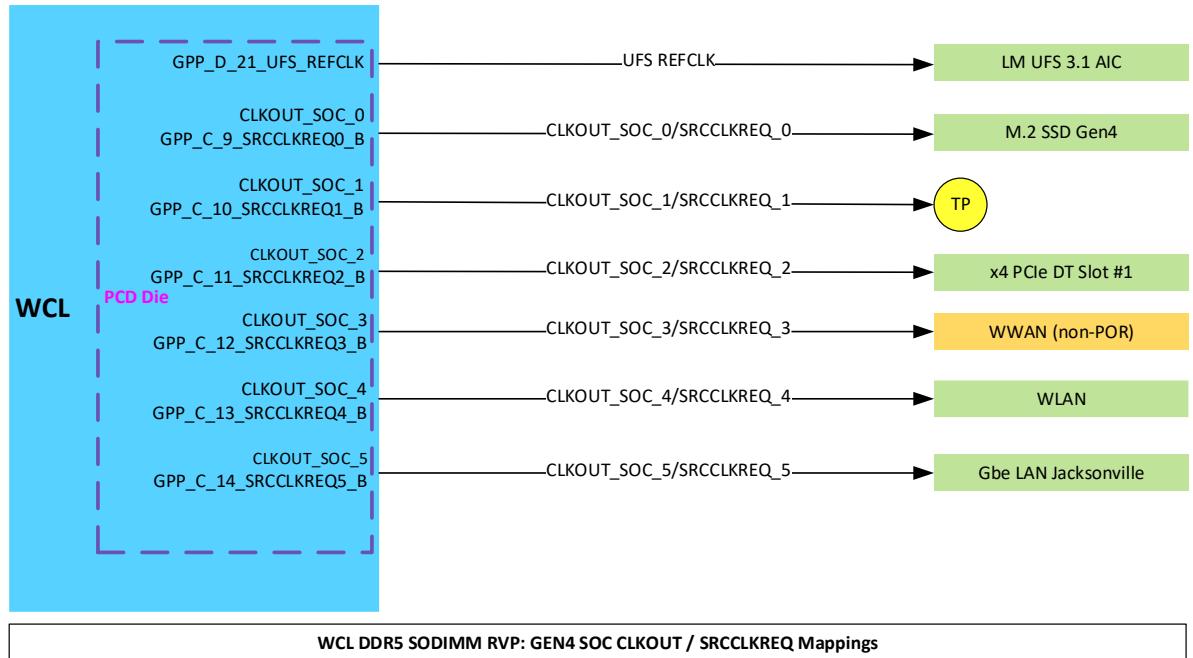


Figure 18 : RVP1 GEN4 SOC CLKOUT / SRCCCLKREQ Mappings

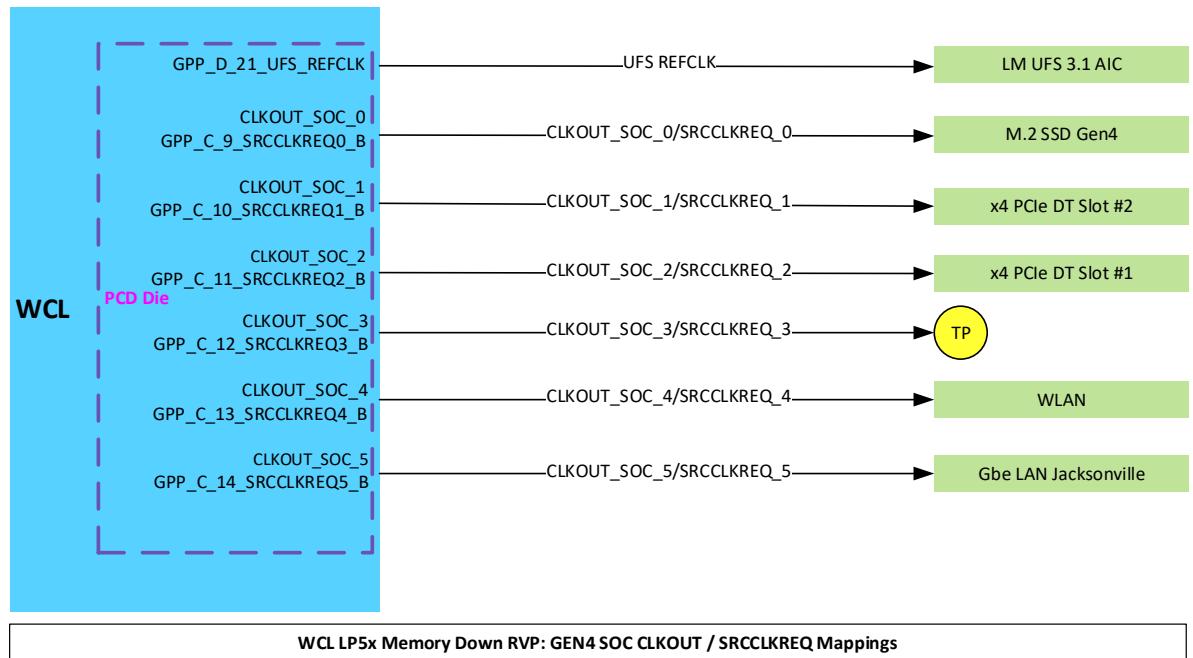


Figure 19 : RVP2 GEN4 SOC CLKOUT / SRCCCLKREQ Mappings

10 Storage

WCL supports different storage options whose high level block diagram & details are as below.

Table 24 : Storage options supported on WCL

Sl. No	Interface	WCL RVP
1	PCIe NAND SSD	Share same M.2 2280 connector interfaced Modules
2	SD CARD over PCIe	Bay Hub PCIe to SD Card reader (Through PCIe x4 slot)
3	UFS	Supported through Little mount AIC

10.1 WCL RVP: Storage support Mapping

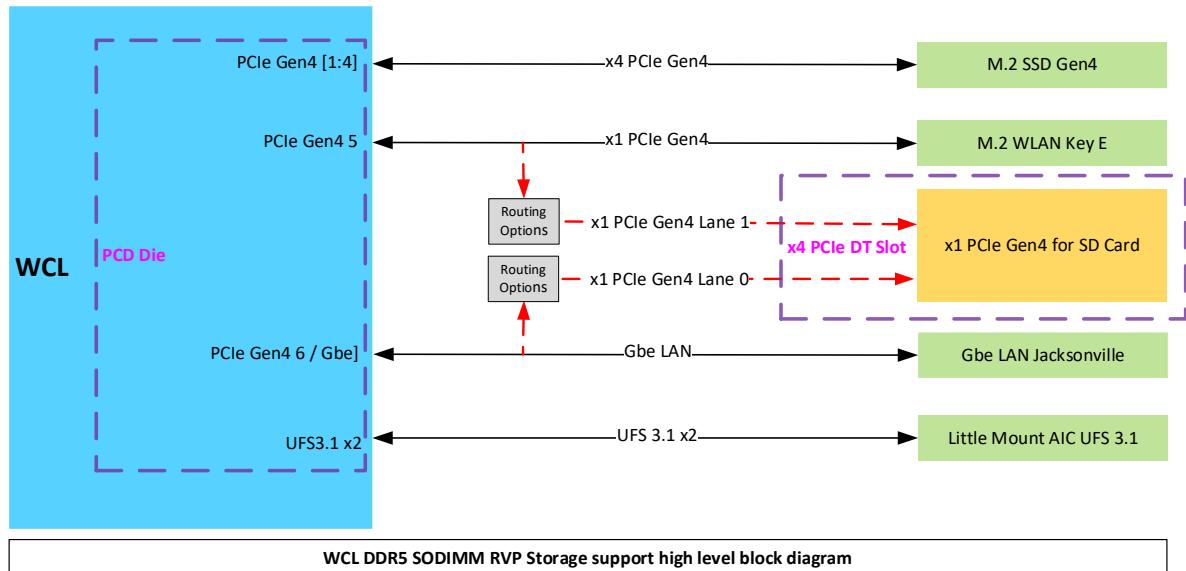


Figure 20 : RVP1 : WCL DDR5 SODIMM T3 RVP : Storage support

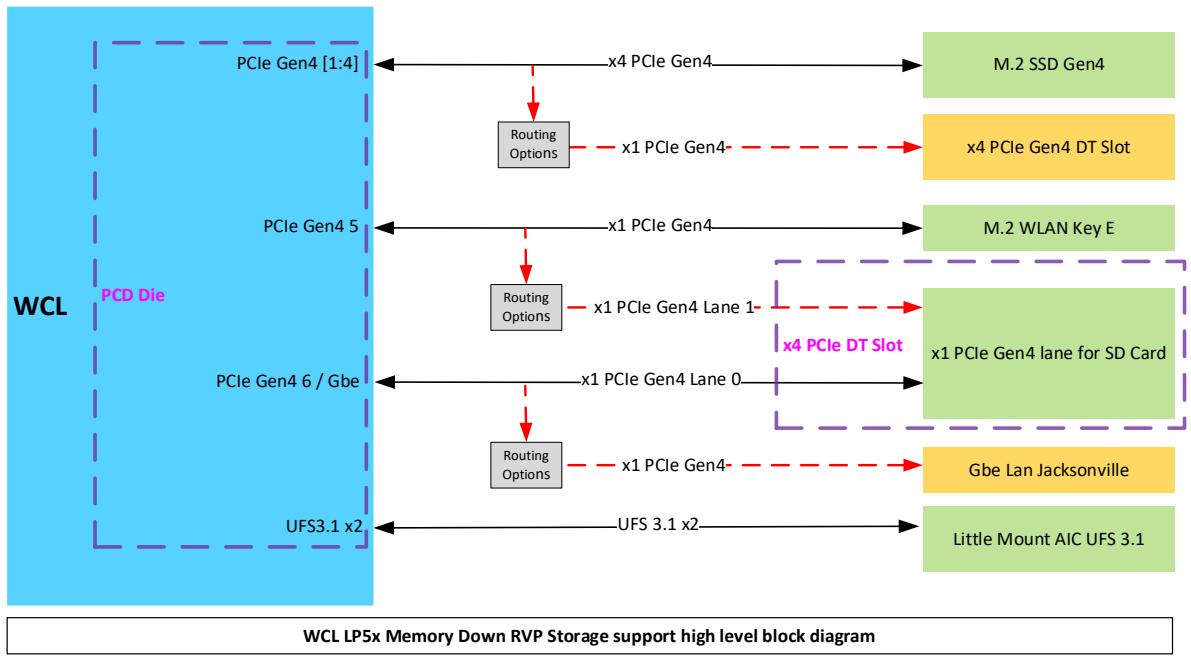


Figure 21 : RVP2 : WCL LP5x Memory Down T3 RVP : Storage support

10.2

M.2 Key-M Connector

WCL RVP's support M.2 SSD Key-M connectors following the PCI SIG M.2 spec. All the M.2 Key-M SSD ports will have RTD3 capability for PERST & WAKE signal coming from SOC.

10.2.1

Dynamic M.2 Key-M SSD sideband GPIO voltage level switching (3.3V vs 1.8V)

WCL platform supports 1.8V IO level only. Platforms need level shifter to support legacy M.2 SSD modules with 3.3V sideband GPIO signaling. Upcoming M.2 modules are coming up with two configurations:

1. Support both 1.8V/3.3V sideband GPIO signal level
2. Support only 1.8V sideband GPIO signal level

For supporting both legacy & upcoming SSD modules, we need dynamic switching of sideband GPIO voltage level between 3.3V & 1.8V.

WCL RVP supports dynamic M.2 Key-M SSD sideband GPIO voltage level (3.3V vs 1.8V) switching.

- VIO_CFG is a signal indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. It is output signal from M.2 Module. Sideband signaling is 3.3V when VIO_CFG signals is low and NC when sideband signaling is 1.8V.

10.2.2 Power Loss Notification (PLN) Support

A sudden loss of power can cause an SSD to lose user data in its volatile write cache & the 3 primary cause for power loss are:

- User presses & holds power button for more than power button overrise time (4s/ 10s/ Custom)
- Battery disconnected in case of notebooks & AC power loss in case of DT systems without UPS.
- Battery runs down.

This proposal will address first cause, the user turning off the power without going through the Windows shut-down process. It is proposed to connect Power Button signal passing through an Open Drain Buffer to M.2 SSD connector Pin 8 & a GPIO from EC to the same open drain buffer. This implementation will be on all the SKUs of the WCL RVPs.

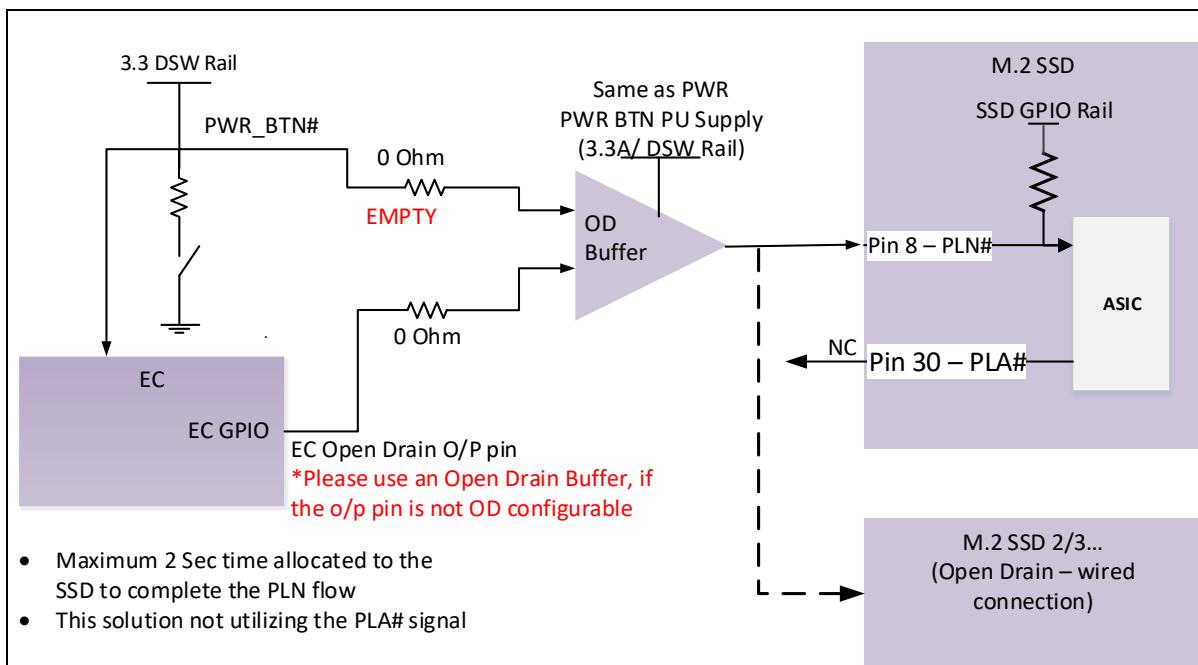


Figure 22 : Power Loss Notification circuit implementation

10.2.3 BIOS recovery architecture

NVMe BIOS recovery feature supports on SSD which is connected to PCIe Gen4 lane [1:4].

10.2.3.1 SPI Descriptor Recovery

SPI Descriptor recovery in WCL is achieved by Descriptor verification (Detection) and recovery by the SPI controller in SOC. Since the Descriptor is required for any firmware to be loaded, it can't be recovered by firmware component.

SPI Descriptor are used in SPI FLASH to access control of the SPI FLASH regions to different masters & specify various properties of these regions. If a SPI-Descriptor gets corrupted the platform will not

be bootable. To recover from SPI-Description corruption, the SPI flash will now contain 3 descriptors and the SPI controller in SOC is modified to read the subsequent descriptor if it finds a corrupted descriptor. This will enable the system to boot even in the presence of 2 corrupted descriptor.

There are 2 straps used for SPI Descriptor recovery, mentioned below:

Table 25 : SPI Descriptor Recovery Strap details

GPIO Pin	Strap Details	Strap Functionality	Comment
GPP_H1	SPI FLASH Descriptor Recovery strap	0= Recovery Disable (Default) 1= Recovery Enable.	Weak Internal 20K PD, Sampled at RSMRSTB.
GPP_H2	SPI Flash Descriptor recovery source selection strap	0=Flash descriptor recovery internal source (Default) 1= Flash descriptor recovery external source	Weak Internal 20K PD, Sampled at RSMRSTB.

10.2.3.2 NVMe Recovery

If the BIOS/CSME partition in the Flash is corrupted, this feature enables the EC to use an out of band mechanism (I2C/SMBUS) with the NVMe drive & rewrite the BIOS/CSME partition into SPI flash. This enables the system to boot in the presence of a corrupted BIOS partition in SPI-NOR. To support this feature, the following are implemented in the design,

- The firmware issue detection & recovery occur in pre-boot stage. Hence, EC and primary M.2 SSD shall be powered up and running before CPU/PCH is enabled.
- When NOT using the recovery mode, the SSD shall be power gated (off) in Sx.
- EC can override the SSD power while in Sx for the recovery.
- EC shall access M.2 SSD secondary partition over I2C/SMBus signals during recovery mode. Level translator is used to convert EC driven 3.3V I2C/SMBus signals to M.2 SSD 1.8V levels.
- EC shall have recovery indication signal (GPIO).
- Flash descriptor override strap is sampled at RSMRST in WCL silicon to enable CSME recovery in MAF mode. EC firmware needs to wait for 100ms before trying to access the SPI flash after FDO strap is sampled high to prevent any conflicting case where SoC & EC both are trying to access SPI flash.
- EC Recovery indication GPIO should drive Flash descriptor override strap (Active high) of SOC as high to hold CSME communication with Flash Chip.

Note: NVMe recovery in MAF mode is not POR for WCL RVP

- In MAF mode during BIOS/CSME recovery, platform power sequencing will be halted at SLP_S3. This is because in MAF mode, for EC to access the SPI flash the eSPI & SPI interface needs to be alive & for that we need RSMRST to be high. So, we can't halt at RSMRST, so we halt at SLP_S3 signal.
- In G3/SAF mode during BIOS/CSME recovery, platform power sequencing will be halted at RSMRST. This is because in G3/SAF mode, EC can directly access the flash so we can halt at RSMRST also.

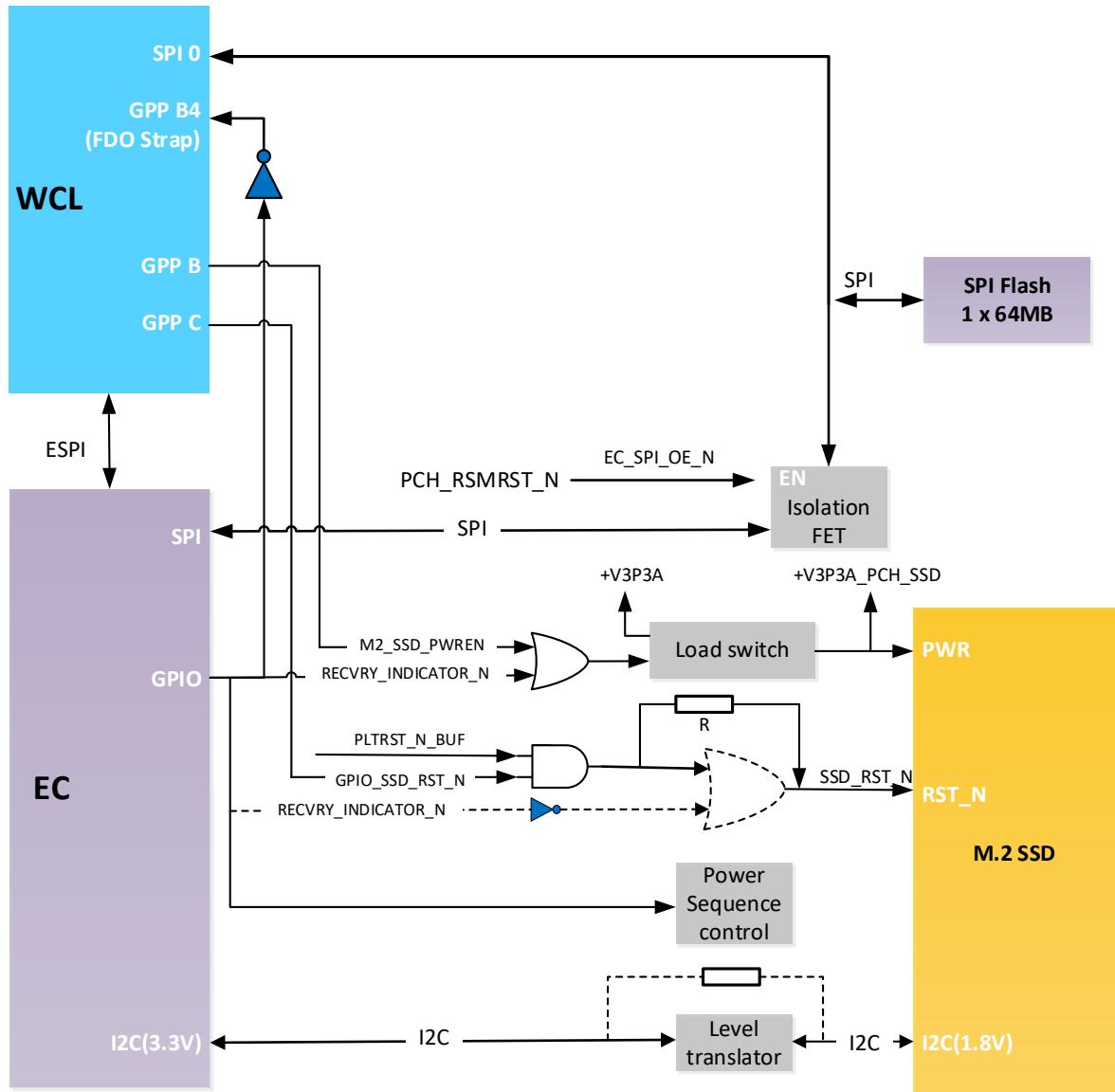


Figure 23 : NIST193 Recovery Hardware implementation block diagram

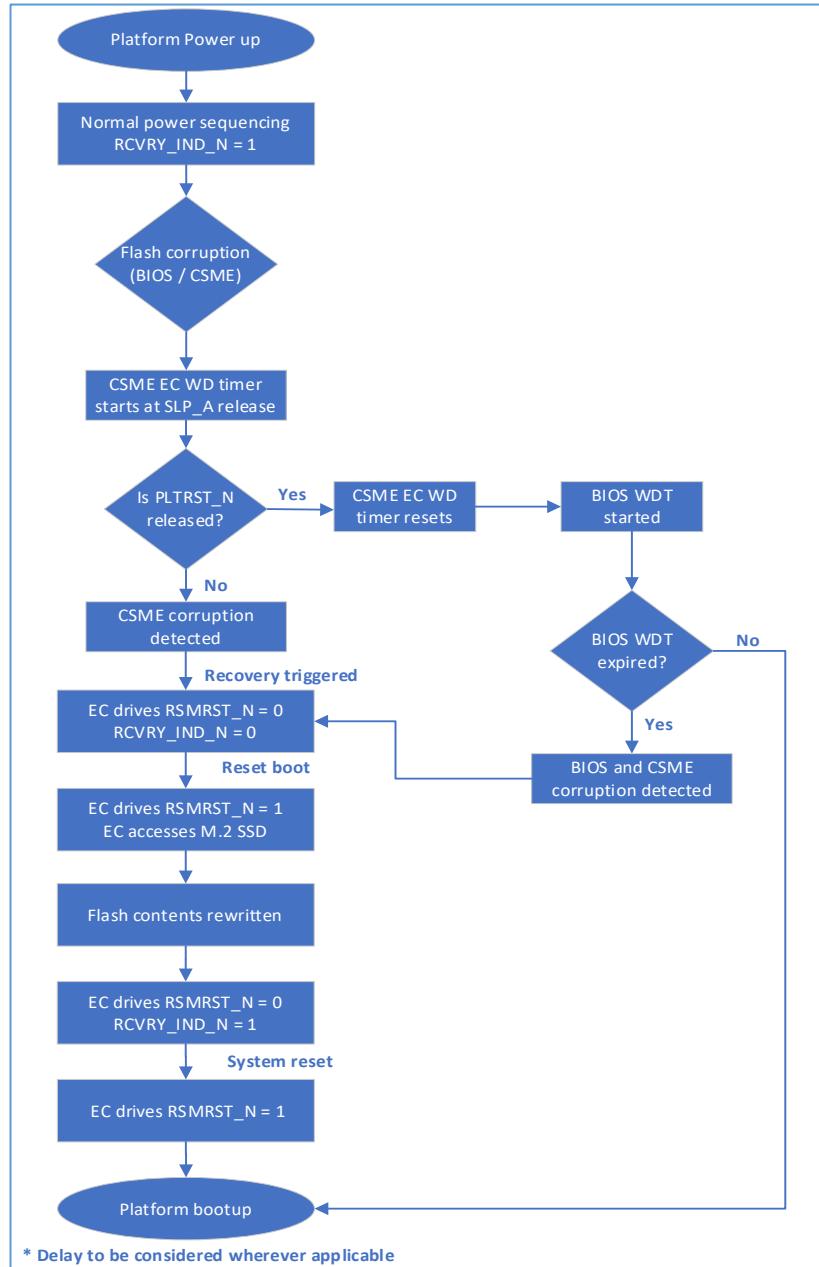


Figure 24 : MAF Recommended Platform Flow

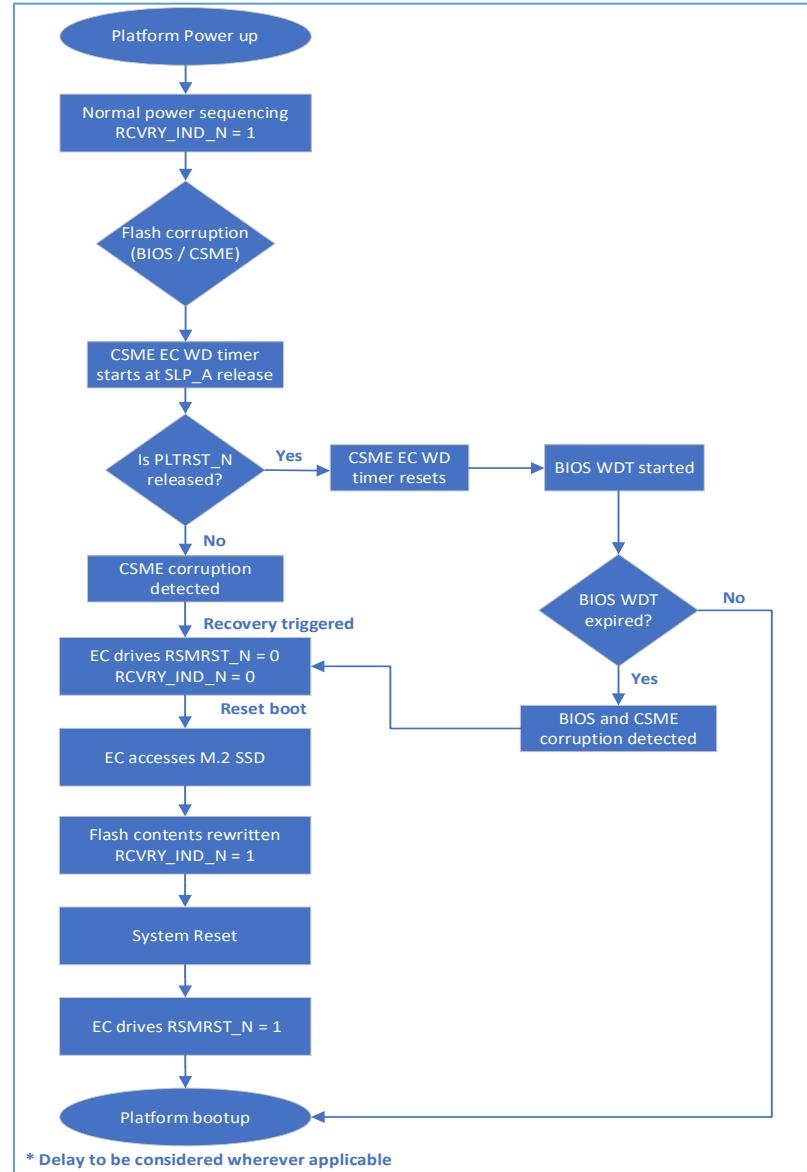


Figure 25 : SAF/G3 Mode recommended Platform Flow

10.3 SD 7.0 card over PCIe

On the WCL RVP the PCIe to SD card interface is validated using the Bay Hub SD 7.0 PCIe to SD bridge IC based AIC & will be plugged on to x4 PCIe DT Slot.

10.4 UFS3.1

UFS 3.1 x2 Gear 4 is supported in WCL RVP. Little mount connector is used for UFS AIC plugging. UFS storage supported on all WCL RVP SKU. UFS power rails work in S0/S0ix Platform state. No RTD3 support for UFS power rails. UFS two lanes fitted with CMC (EMC requirement) with bypass option.

UFS device soldered on LM (Little mount) UFS AIC and UFS cards plugged on the B2B connector (IPN# E21540-001) provided on RVP.

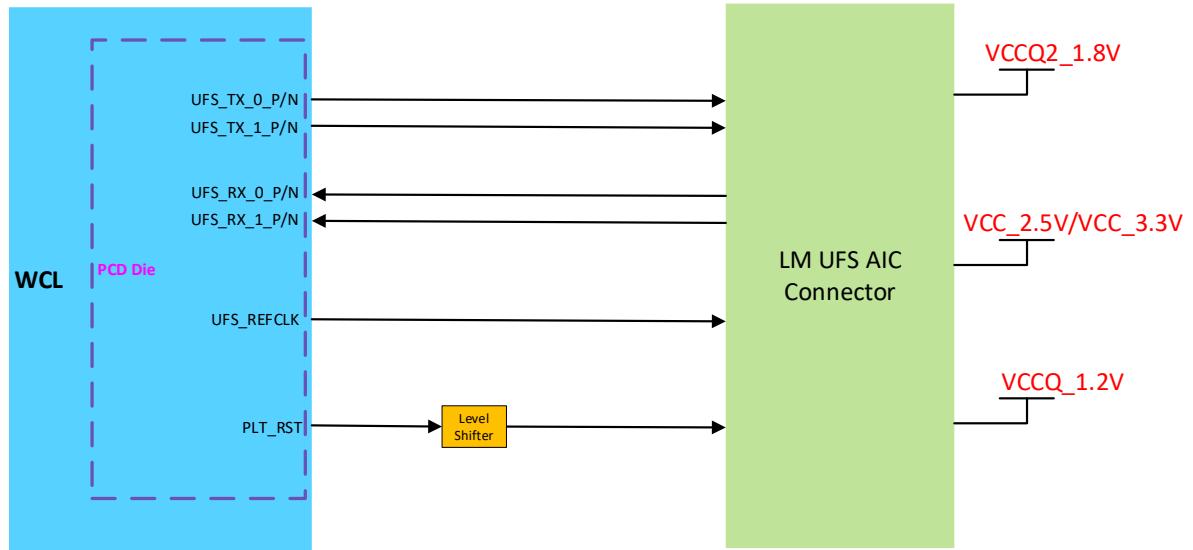


Figure 26 : WCL UFS AIC CONN high level block diagram

11 Connectivity

The primary connectivity interface for the WCL RVP lies with the Chipset. The WCL chipset supports integrated connectivity CNVi core which eliminates the need for an external WiFi chip. The other connectivity options are GbE LAN and WWAN. Table 26 gives the list of Modules supported on WCL RVP SKUs as connectivity solutions.

Note: In WCL RVP there is no RTD3 support for both WLAN and WWAN and the corresponding load switches for enabling power is no longer supported.

Table 26: Connectivity Support on WCL RVP boards

Interface Name	Module Name	Remarks
Integrated CNVIO	Garfield Peak 2, Filmore Peak 2	M.2 Key E Socket 3
Discrete WLAN+BT	Gale peak 2	M.2 Key E Socket 3
WWAN(Non-POR)	Maple Spring	M.2 Key B Socket 2
Gbe LAN	Jackson Ville Module	RJ-45 Jack
PCIe	Fox-Ville Add-In Card (Non-POR)	x1 PCIe AIC

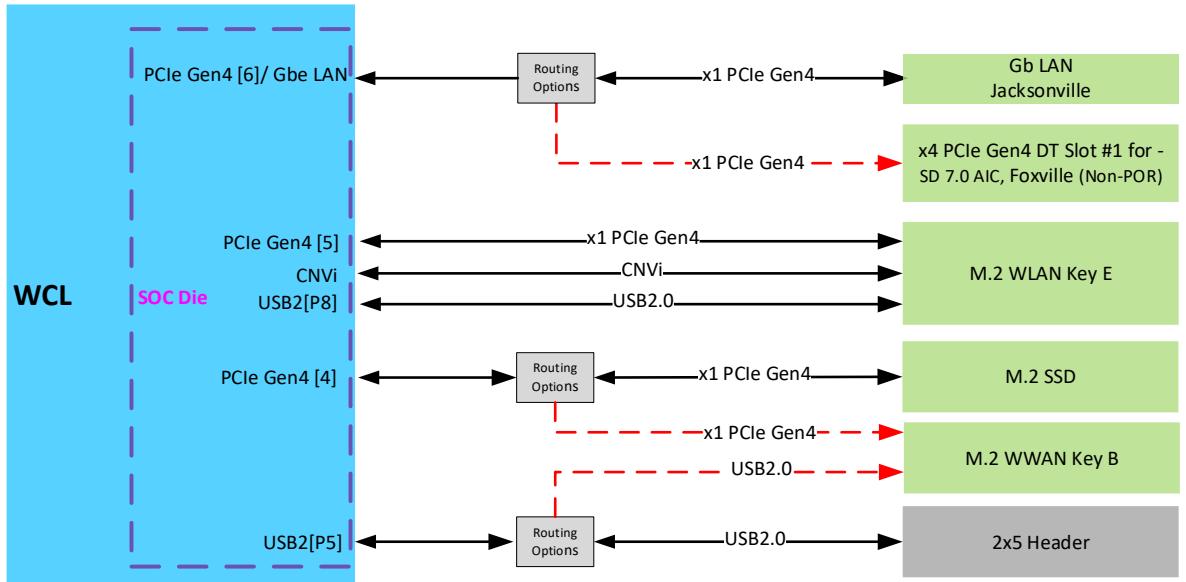


Figure 27 :RVP1 WCL DDR5 SODIMM T3 RVP Connectivity Block Diagram

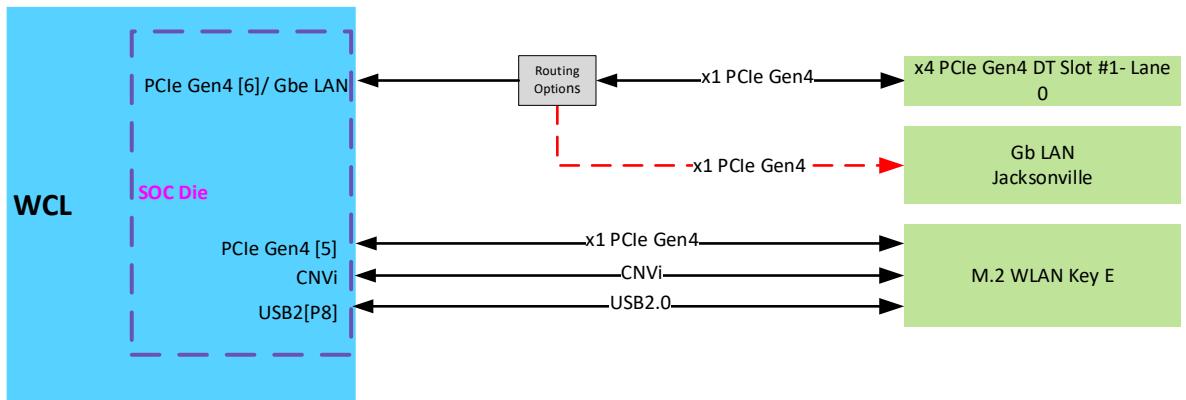


Figure 28 : RVP2 WCL LP5x Memory down T3 RVP Connectivity Block Diagram

11.1

Connectivity Integration (CNVi)

The RVP supports a M.2 Hybrid Key E slot for Wireless connectivity solutions, it supports a Combo WiFi + BT M.2 module. The Wi-Fi interfaces are over integrated CNVi or x1 PCIe port while the Bluetooth connectivity is supported over CNVi, USB2 or UART+I2S interfaces based on modules is getting plugged in.

Connectivity integration (CNVi) is a general term referring to a family of connectivity solutions which are based on the hard macro(Blazar) embedded within Intel Silicon. Besides the Blazar, the CNVi contains an external RF companion module (CRF) and RF antennas. This module will be implemented

as a M.2 (2230) module solution on WCL RVP. The RF companion will be Filmore Peak 2, Garfield Peak based M.2 Key E module with provision for connecting the external RF antennas.

For Integrated WiFi and Bluetooth, CNVi DPHY TX/RX, STEP I/F/CNVio gen2 and RGI/BRI signals are used respectively. For discrete WiFi x1 PCIe is used and for discrete Bluetooth-USB2.0 and UART signals are used.

In the below diagram, all necessary signals from WCL to the M.2 Key E connector has been shown.

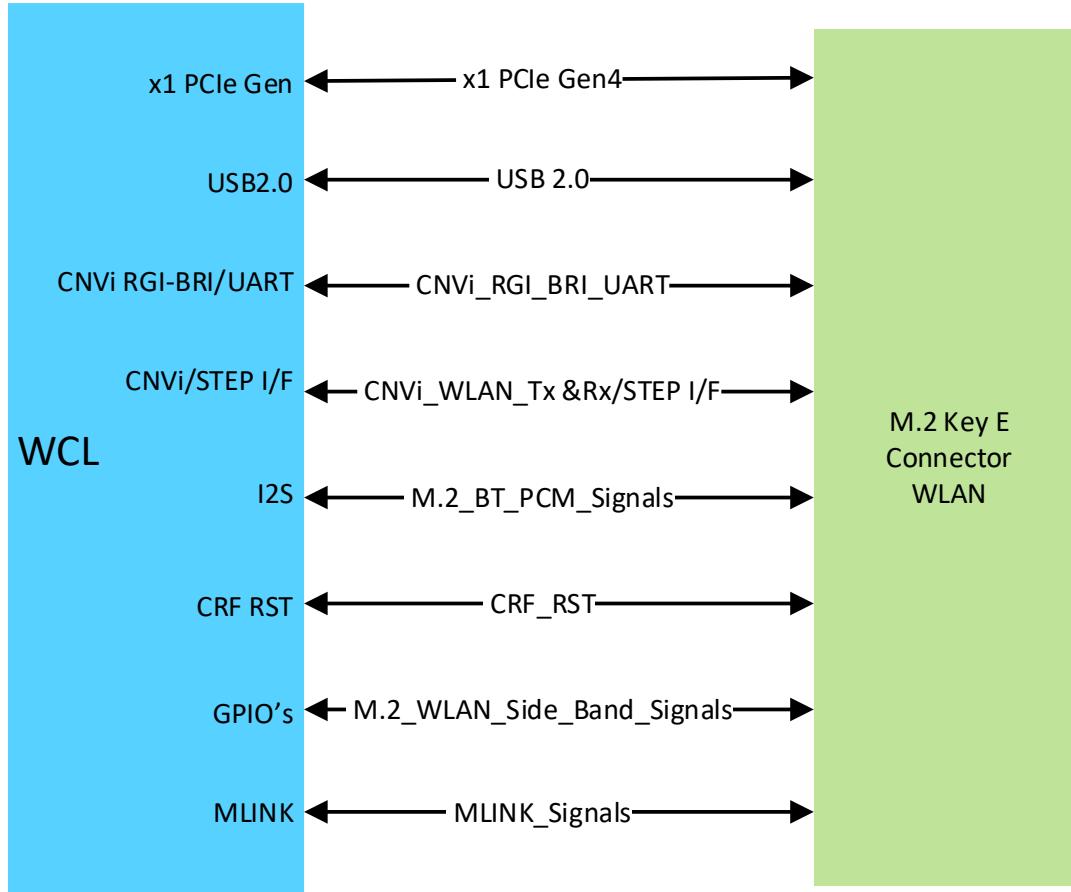


Figure 29 : WCL RVP M.2 Key E WLAN implementation high level block diagram

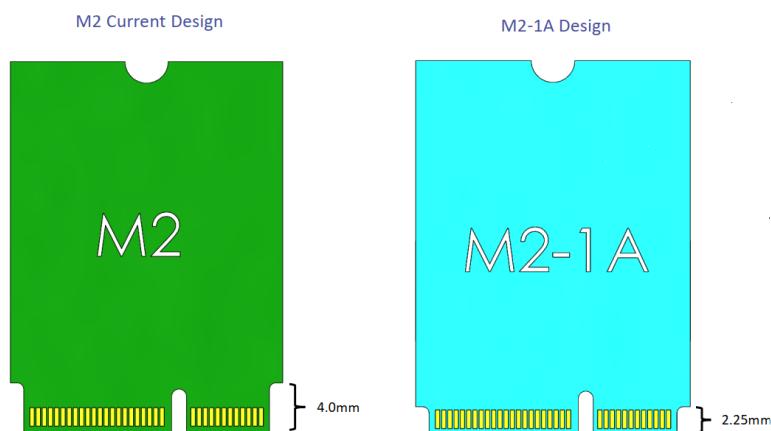
Table 27: Interface Details for WLAN Module

Description	Interface Name/ Signal Name	Support on WCL RVP
WIFI	<ul style="list-style-type: none"> CNVi DPhy & STEP PCIe CLINK(CSME) 	Yes
BT DATA	<ul style="list-style-type: none"> USB2.0, BRI 	Yes
WLAN M.2 Control	<ul style="list-style-type: none"> RGI RF_RESET# WIFI_RFKILL# BT_RFKILL#1 WLAN_LED# BT_LED# 	Yes
BT AUDIO	<ul style="list-style-type: none"> PCM 	Yes
RF Coexistence	<ul style="list-style-type: none"> UART_RX UART_TX UART supports Real-Time Coexistence 	Yes

11.1.1 M.2-1A Key E Connector

Next generation WLAN modules need more power to meet performance and feature targets. M2 specification is restricting these features due to the limited current supply (2.5A) allowed in the connector specification.

The new M.2-1A connector will support 1A per pin, With 4pin it will support 4A. New mechanical key allowing current M.2 and New M.2-1A insertion but does not allow M.2-1A to work in old M.2 connectors.

**Figure 30 : New M.2-1A design**

11.2

WWAN M.2 Module (Non- POR)

WCL RVP supports M.2 7560 Socket 2 WWAN module. Single PCIe lane, x1 interface, and USB2.0 interface is routed to M.2 WWAN Key B connector. The USB 2.0 interface is used only during the production testing and debugging activities. Figure 31 below shows the interface connectivity of WWAN Module to WCL.

Note: WWAN connectivity interface is not POR for WCL. RVP will provide a x1 PCIE based M.2-1A connector on RVP1 DDR5 SODIMM T3 SKU to support the hardware needed for WWAN enablement. This is done to be ready for any future requirement for WWAN testing or any POR changes with respect to WWAN based on marketing/CCE feedback. This needs to be accompanied by CCB to enable SW/FW support for the same.

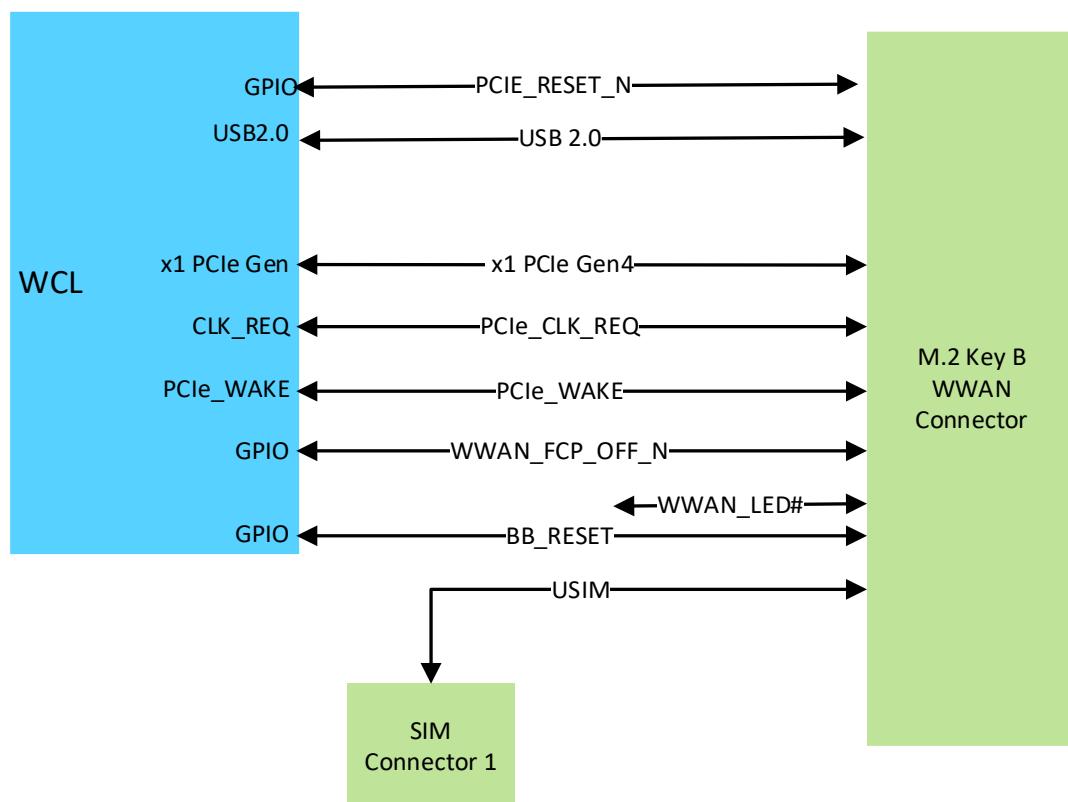


Figure 31 : WCL RVP M.2 Key-B WWAN implementation high level block diagram

Further details on SIM Card Signals, Module WAKE and Reset etc. are listed in below table.

Table 28: Interface Details for Maple Spring

Description	Interface Name/ Signal Name	Support on WCL RVP
Inter-processor Communications	PCIe USB 2.0	Yes
USIM with Card Detect	SIM_CLK, SIM_RESET, SIM_IO, SIM_PWR, SIM_DETECT	Yes
WWAN M.2 Control	FULL_CARD_POWER_OFF# RESET# PERST# W_DISABLE# LED#1 DPR (Body SAR)	Yes
Global Positioning (GPS/GLONASS)	TX_BLANKING, FINE_TUNE_AIDING (FTA)	Yes
CSME	I2C	No
RF Coexistence	UART_RX UART_TX UART supports Real-Time Coexistence	No**

**NOTE: Module does not support RF coexistence, but RVP has provision to test the Coexistence.

An LED is used to provide status indications to users via system provided indicators. LED#1 is an active low open drain output signal intended to drive system-mounted LED.

Table 29: LED Indicator description for WWAN

State	Definition	WWAN State
OFF	The LED is emitting no light	Not powered
ON	The LED is emitting light in a stable non-flashing state	Powered registered but not transmitting or receiving
BLINKING	State Blinking	TX / RX activity in progress

11.2.1 M.2-1A Key B Connector

Next generation WWAN modules need more power to meet performance and feature targets. M.2 specification is restricting these features due to the limited current supply (2.5A) allowed in the connector specification.

The new M.2-1A connector will support 1A per pin (Total 5A). New mechanical key allowing current M.2 and New M.2-1A insertion but not allow M.2-1A to work in old M.2 connectors.

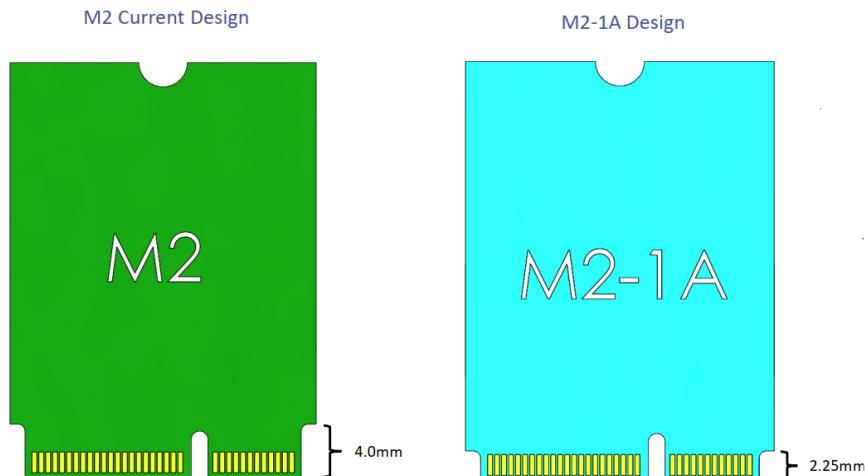


Figure 32 : New M.2-1A design

11.3 GbE LAN

WCL RVP supports Wired Gigabit Ethernet interface through on-board Intel 1000Base-T PHY LAN Controller I219 (Jacksonville) that connects to PCH through an x1 PCIe interface. The LAN PHY operates in Gen1 PCIe mode.

2.5G Base-T MAC/PHY LAN Controller I225 (Foxville) based wired Ethernet will be validated through AIC. SMLink would be provided for the Foxville AIC. However, Foxville AIC is non-POR in WCL.

The LED indications for connectivity status of GbE LAN are listed in table below.

Table 30: LED definition for RJ45 Connector

LED Function	State Description
Speed	OFF: 10Mbps GREEN: 100Mbps YELLOW: 1Gbps
Activity	GREEN: Link is up there no activity on the lines GREEN BLINKING: Tx / Rx or both Activity on the lines

RVP supports standard x4 PCI express desktop slots from SOC which can be used to plug-in a x1 or x4 Network Interface Cards for enabling the validation of third-party connectivity solutions.

11.3.1 Jackson Ville Controller

The Ethernet Connect I219 is a single-port Gigabit Ethernet Physical Layer Transceiver. It connects to an integrated Media Access Controller (MAC) through a dedicated interconnect.

- I219 supports operation at 10/100/1000 Mb/s data rates.
- Provides IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications.
- Support for the Energy Efficient Ethernet (EEE) 802.3az specification.
- IEEE 802.3u auto-negotiation conformance
- Supports carrier extension (half duplex)
- 802.1as/1588 conformance
- No support for Gb/s half-duplex operation
- Intel® vPro support with appropriate Intel chipset components.
- Ultra-Low Power at cable disconnect (<1 mW) enables platform support for connected standby.
- PCIe-based interface for active state operation (S0 state)
- SMBus-based interface for host and management traffic (Sx low power state)

11.3.2 Foxville Controller (Non-POR)

The Intel® Ethernet Controller I225 (I225) is a single-port, compact, low power Gigabit Ethernet (GbE) controller. It is a fully integrated GbE Media Access Control (MAC) and Physical Layer (PHY) device, offering 10/100/1000/2500 Mb/s data rates. The interface-to-host system is a one lane PCI Express* (PCIe*) Gen 2 version 2.1

- 802.1q VLAN support
- 802.3az EEE support
- Support for AMT / Intel® vPro™ Technology
 - Host onboard & Dock
 - Intel Stable Image Platform Program (SIPP™) support
- Automatic polarity correction
- Network proxy/ARP Offload
- MDC/MDIO management interface
 - MDI Lane Swap design support
- Smart speed operation for automatic speed reduction on faulty cable plants
- Power Optimizer Support

On the WCL RVP the Foxville controller is validated by using the Foxville AIC plugged on to x1 PCIe DT Slot

12 Audio

WCL RVP supports ALC722 (SDCA V1.0) compliant Soundwire based codec down on the board through Sound wire. The codec drives on-board 3.5mm board jack along with DMIC and SPKR application via JS header through transducer AIC. The rest of the Audio features must be supported through add-in-cards through audio headers JA, JD, JE & JH. By default, SNDW will be connected to the onboard Codec. JH header is used to provide additional power options to the Audio AIC.

Onboard validation includes ALC722 Codec Jack, DMIC & SPKR through sound wire single lane/multilane configuration. Other validation will be performed on 6th Gen Realtek AIC and Cirrus/TI Audio AIC's.

Table 39: WCL RVP Audio interface landing zone details

RVP SKU's	RVP Feature	Device Supported in RVP
RVP 1: WCL SODIMM T3 PCB- Base SKU	Audio Options- <ul style="list-style-type: none"> 1. Audio Jack Codec ALC722 Solder Down 2. Audio HDR - JA (HDA/I2S Codec Support) 3. Audio HDR - JD (DMIC support) 4. Audio HDR - JE (SNDW Codec support) 5. Power HDR -JH (RFU PWR support) 6. Audio HDR – JS (Codec DMIC & SPKR support) 7. I2S2 to M.2 Key-E for BT 	Soldered Down: Realtek ALC722-CG (on-board RVP) AIC: Realtek ALC712-VB (Gen6.x AIOC) Realtek ALC245 (Gen3.x AIOC) Cirrus CS42L43 (Cohen) AIOC V3 Realtek Gen41 Transducer (Speaker / DMIC)
RVP 2: WCL LP5x Memory Down T3 PCB		

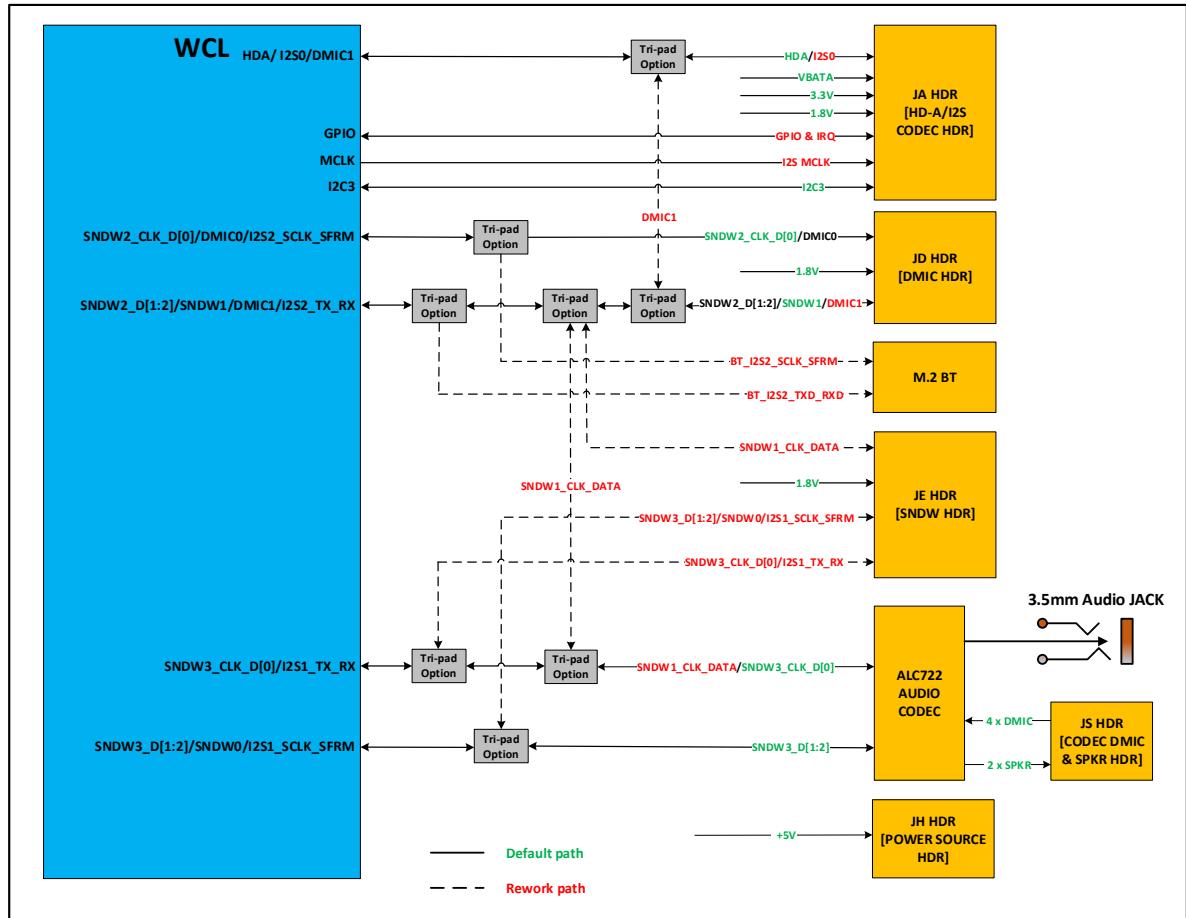


Figure 33: WCL RVP Audio high level block diagram

12.1 ALC722 SNDW on-board CODEC

The ALC722-CG is compliant to SDCA v1.0[MIPI04], where SDCA stands for SoundWire Device Class for Audio architecture that standardizes the interface for software to control the audio function through a SoundWire interface.

- The ALC722 integrates a headphone amplifier can drive 15-ohm headphone & supports legacy Universal Audio Jack.
- An integrated stereo Class-D amplifier directly drives the speakers. The Class-D amplifier is designed to drive speakers with as low as 4Ω impedance. Its maximum output power is 2.8W per channel at 5V power supply. The advantage of an integrated Class-D amplifier in the ALC722 is high efficiency with lower power consumption.
- The ALC722 has two stereo digital microphone inputs.

WCL RVP enables dedicated 12-pin header [JS] on RVP to connect Realtek Gen4.x transducer card for this on-board configuration using a Y-cable solution as shown below.

- SNDW3 multilane connects to ALC722 codec by default, SNDW1 single lane can be enabled with a rework option.

Realtek GEN4.x card (same as existing GEN 3.1 transducer card) supports 4xDMIC's and 2x SPKR assembly.

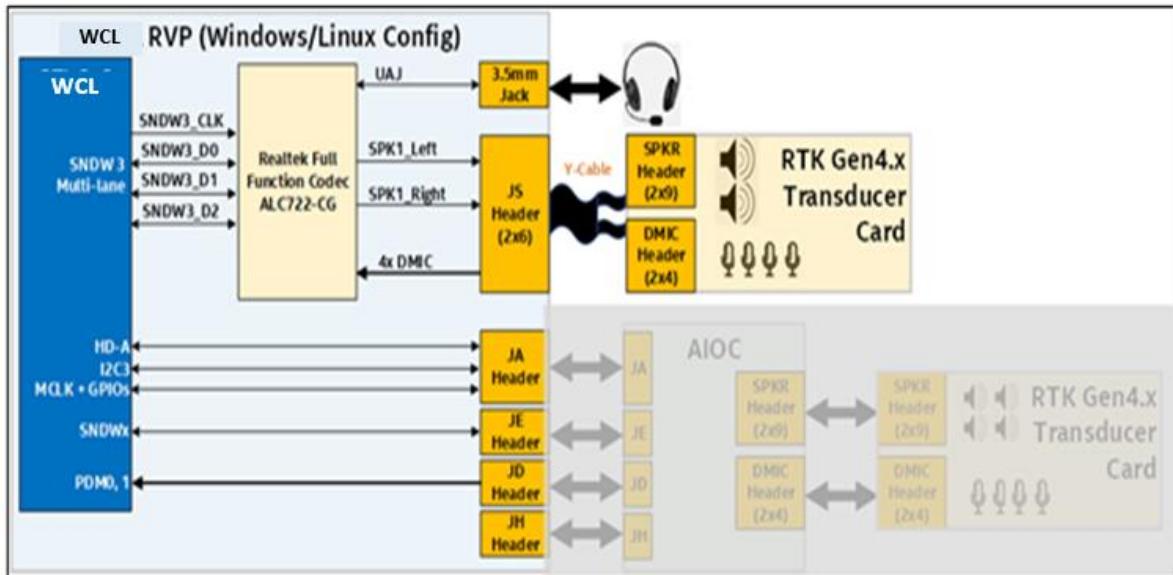


Figure 34: WCL RVP Audio ALC722 on-board configuration

12.2

Audio AIC validation configurations

Refer below table for AIOC supported CODECs versus validation configuration details.

Table 40: WCL RVP Audio Windows/Linux build validation configuration table

Star definition	5 Star Config	4 Star config1	3 STAR1	3 STAR 2	2 Star config1
Audio Codec	Multilane ALC722-CG (onboard RVP)	HDA ALC245 + 4x Codec DMIC AIOC Gen 3.0	ALC712-VB+ ALC712-VB attached 2ch DMIC AIOC Gen 6.0	Cirrus AIC-v2 based Config: Cohen CS42L43	HDA ALC245 + 4x Codec DMIC AIOC Gen 3.0
Speaker	2 speaker from ALC722	2 speaker from ALC245	2 speaker from ALC712-VB	2 speaker from Cohen	2 speaker from ALC245
DMIC connected to	Codec	codec	Codec	codec	codec
WoV (BIOS only)	Enable	Enable	Enable	Enable	Enable
Default Endpoint	Speaker-DMIC	Speaker-DMIC	Speaker-DMIC	Speaker-DMIC	Speaker-DMIC
Audio driver	ISST	ISST	ISST	ISST	ISST
Codec driver	ACX/SDCA	Enabled - Model?	Enabled - Model?	Enabled - Model?	Enabled - Model?
BT Audio offload(BIOS) - Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
USB audio offload	Enabled	Enabled	Enabled	Enabled	Enabled
SSID	TBD	TBD	TBD	TBD	TBD

WCL RVP2 CHROME sku supports following validation use-cases, without need for any resistor rework.

- I2S config using Praxton Audio Interposer (+ Chrome Audio AIC):
 - Codec (JA – I2S0) + Amp (JE – I2S1) + DMIC (JD – PDM0,1)
 - Dedicated GPIO for Codec_IRQ.
- SNDW config using on-board codec ALC722:
 - SNDW1 single lane configured by default. SNDW3 Multilane can be chosen in future with resistor stuff/un-stuff.

Figure 35: WCL RVP Audio CHROME SoC pin configuration

	Chrome
xxgpp_d_9_i2s_mclk1_out	I2S0
xxgpp_d_10_hda_bclk_i2s0_sclk_hdacpu_bclk	
xxgpp_d_11_hda_sync_i2s0_sfrm	
xxgpp_d_12_hda_sdo_i2s0_txd_hdacpu_sdo	
xxgpp_d_13_hda_sdi_0_i2s0_rxd_hdacpu_sdi	
xxgpp_d_16_hda_RST_B_dmic_clk_a_1	PDM1
xxgpp_d_17_hda_sdi_1_dmic_data_1	
xxgpp_s_0 sndw3_clk i2s1_txd	I2S1
xxgpp_s_1 sndw3_data0 i2s1_rxd	
xxgpp_s_2 sndw3_data1 sndw0_clk dmic_clk_a_0_i2s1_sclk	
xxgpp_s_3 sndw3_data2 sndw2_data1 sndw0_data0 dmic_data_0_i2s1_sfrm	
xxgpp_s_4 sndw2_clk dmic_clk_a_0_i2s2_sclk	PDM0
xxgpp_s_5 sndw2_data0 dmic_data_0_i2s2_sfrm	
xxgpp_s_6 sndw2_data1 sndw1_clk dmic_clk_a_1_i2s2_txd	SNDW1
xxgpp_s_7 sndw3_data3 sndw2_data2 sndw1_data0 dmic_data_1_i2s2_rxd	

12.3

Audio Headers

WCL silicon supports only 15 audio functionality pins. SoC muxing consideration is driven by CCG Platform team (comprising of Audio Domain Architects, as well as Platform EIO stakeholders) to balance between total GPIO pins needed/reserved for Audio while meeting primary requirements for the different segments (Windows, Chrome, IOT, etc). Pin muxing with reduced pin count for the WCL SoC is shown in the below table.

Table 31: WCL Audio pin muxing

SoC Pin Name	SoundWire 3	SoundWire 2	SoundWire 0/1	DMIC	I2S / PCM	HD-A
xxgpp_d_10_hda_bclk_i2s0_sclk_hdacpu_bclk					I2SSCLK[0]	HDA_BCLK
xxgpp_d_11_hda_sync_i2s0_sfrm					I2SSFRM[0]	HDA_SYNC
xxgpp_d_12_hda_sdo_i2s0_txd_hdacpu_sdo					I2STXD[0]	HDA_SDO
xxgpp_d_13_hda_sdi_0_i2s0_rxd_hdacpu_sdi					I2SRXD[0]	HDA_SDIO
xxgpp_d_16_hda_rst_b_dmic_clk_a_1				DMIC_CLKA[1]		HDA_RST#
xxgpp_d_17_hda_sdi_1_dmic_data_1				DMIC_DATA[1]		HDA_SD1
xxgpp_d_9_i2s_mclk1_out					I2SMCLK[0]	
xxgpp_s_0_sndw3_clk_i2s1_txd	SNDW_CLK				I2STXD[1]	
xxgpp_s_1_sndw3_data0_i2s1_rxd	SNDW_DATA[0]				I2SRXD[1]	
xxgpp_s_2_sndw3_data1_sndw0_clk_dmic_clk_a_0_i2s1_sclk	SNDW_DATA[1]		SNDW_CLK	DMIC_CLKA[0]	I2SCLK[1]	
xxgpp_s_3_sndw3_data2_a_sndw2_data1_sndw0_data0_dmic_data_0_i2s1_sfrm	SNDW_DATA[2]	SNDW_DATA[1]	SNDW_DATA[0]	DMIC_DATA[0]	I2SFRM[1]	
xxgpp_s_4_sndw2_clk_a_dmic_clk_a_0_i2s2_sclk		SNDW_CLK		DMIC_CLKA[0]	I2SCLK[2]	
xxgpp_s_5_sndw2_data0_a_dmic_data_0_i2s2_sfrm		SNDW_DATA[0]		DMIC_DATA[0]	I2SFRM[2]	
xxgpp_s_6_sndw2_data1_sndw1_clk_dmic_clk_a_1_i2s2_txd		SNDW_DATA[1]	SNDW_CLK[1]	DMIC_CLKA[1]	I2STXD[2]	
xxgpp_s_7_sndw3_data3_sndw2_data2_sndw1_data0_dmic_data_1_i2s2_rxd	SNDW_DATA[3]	SNDW_DATA[2]	SNDW_DATA[1]	DMIC_DATA[1]	I2SRXD[2]	

WCL RVP supports different codec validation via AIC connected through JA, JD, JE & JH headers. Refer below section for each audio header pin details supported for Windows/Linux vs Chrome configuration when BT-audio is not enabled.

12.3.1

JA Header[HDA/I2S header]

JA header is used to provide clock & data transmission in HDA mode & I2S mode. For HDA mode, Realtek GEN3 AIC (ALC245) will be used along with the transducer card. In SNDW mode, it will be used as power source for AIC. Refer below table for the header pinout vs silicon pin mapping details.

Table 32: Audio Header (JA) Connection

JA Header Pin Number	SoC Signal Name	Header Signal Definition
JA.1	GPP_D_10_HDA_BCLK_I2S0_SCLK_HDACPU_BCLK	HDA_BCLK_I2S0_SCLK_HDR
JA.2	NA	GND
JA.3	xxgpp_d_16_hda_RST_B_DMIC_CLK_A_1 /GPP_D_9_I2S_MCLK1_OUT	HDA_RST_N_I2S_MCLK1_HDR
JA.4	NA	+V1P8DX_AUDIO_JA
JA.5	GPP_D_11_HDA_SYNC_I2S0_SFRM	HDA_SYNC_I2S0_SFRM_HDR
JA.6	NA	GND
JA.7	GPP_D_12_HDA_SDO_I2S0_TXD_HDACPU_SDO	HDA_SDO_I2S0_TXD_HDR
JA.8	NA	+V3P3DX_AUDIO_JA
JA.9	GPP_D_13_HDA_SDIO_0_I2S0_RXD_HDACPU_SDIO	HDA_SDIO_I2S0_RXD_HDR
JA.10	NA	+VBATA_V5DX_AUDIO_JA
JA.11	GPP_D_17_HDA_SDIO_1_DMIC_DATA_1 /GPP_E_19_PMC_I2C_SDA	HDA_SDIO_1_GPIO_EN_HDR
JA.12	NA	RESERVED(key)
JA.13	GPP_H_7_I2C3_SCL_UART1_TXD_A_ISH_UART1_RXD	I2C3_SCL_AUDIO_HDR
JA.14	GPP_H_6_I2C3_SDA_UART1_RXD_A_ISH_UART1_RXD	I2C3_SDA_AUDIO_HDR
JA.15	GPP_F_17_THC1_SPI2_CS_B_A_ISH_SPI_CS_B_GSPI1_CS0_B(WIP)	CODEC_IRQ_HDRX45
JA.16	NA	GND

12.3.2 JD Header

The JD header can be configured to drive 2-SPKR/4-SPKR using ALC1320 stereo amplifier codecs on Realtek GEN6 AIC or it can drive 6-SPKR using 6x Jamerson CS35L56 smart amplifiers on cirrus v3 AIC and it can be used to connect 4xDMIC's directly (via Transducer card). Refer below table for the header pinout vs silicon pin mapping details.

Table 33: Audio Header (JD) Pinout

JD Header Pin Number	SoC Signal Name	Header Signal Definition
JD.1	GPP_S_4 SNDW2_CLK_DMIC_CLK_A_0_I2S2_SCLK	DMIC0_CLK_SNDW2_CLK_HDR
JD.2	GPP_S_5 SNDW2_DATA0_DMIC_DATA_0_I2S2_SFRM	DMIC0_DATA_SNDW2_DATA0_HDR
JD.3	NA	GND
JD.4	NA	V1P8DX_DMIC_JD
JD.5	GPP_S_6 SNDW2_DATA1_SNDW1_CLK_DMIC_CLK_A_1_I2S2_T XD /GPP_D_16_HDA_RST_B_DMIC_CLK_A_1	DMIC1_CLK_SNDW1_CLK_SNDW2_D ATA1_HDR
JD.6	GPP_S_7 SNDW3_DATA3_SNDW2_DATA2_SNDW1_DATA0_DMI C_DATA_1_I2S2_RXD/GPP_D_17_HDA_SDIO_1_DMIC_DATA_1	DMIC1_DATA_SNDW1_DATA0_SND W2_DATA2_HDR
JD.7	NA	GND
JD.8	NA	RESERVED(key)

12.3.3 JE Header

The JE header can be used to drive ALC712-VB full function codec or ALC713-VB UAJ codec in multilane operation on Realtek GEN6 AIC. It can also drive Cohen CS42L43 jack codec in multilane operation on Cirrus v3 AIC. Refer below table for the header pinout vs silicon pin mapping details.

Table 34: Audio Header (JE) Pinout

JE Header Pin Number	SoC Signal Name	Header Signal Definition
JE.1	GPP_S_2_SNDW3_DATA1_SNDW0_CLK_DMIC_CLK_A_0_I2S1_SCLK	SNDW0_CLK_SNDW3_DATA1_I2S1_CLK_HDR
JE.2	GPP_S_3_SNDW3_DATA2_SNDW2_DATA1_SNDW0_DATA0_DMIC_DATA_0_I2S1_SFRM	SNDW0_DATA0_SNDW3_DATA2_I2S1_SFRM_HDR
JE.3	NA	GND
JE.4	NA	+V1P8DX_V5DX_AUDIO_JE
JE.5	GPP_S_6_SNDW2_DATA1_SNDW1_CLK_DMIC_CLK_A_1_I2S2_TXD	SNDW1_CLK_HDR
JE.6	GPP_S_7_SNDW3_DATA3_SNDW2_DATA2_SNDW1_DATA0_DMIC_DATA_1_I2S2_RXD	SNDW1_DATA0_HDR
JE.7	NA	GND
JE.8	NA	RESERVED(key)
JE.9	GPP_S_0_SNDW3_CLK_I2S1_TXD	SNDW3_CLK_I2S1_TXD_HDR
JE.10	GPP_S_1_SNDW3_DATA0_I2S1_RXD	SNDW3_DATA0_I2S1_RXD_HDR

12.3.4 JH Header

JH header will be used as additional power source in 4-SPKR/6-SPKR configuration. It also provides, SUS_CLK connection as always-on-clock for future use (Smart DMIC use-cases), PLT_RST_N is routed additionally so that when AIOC is powered from external supply and power recycle is done for RVP, PLT_RST_N can be used to ensure AIOC power recycle in such cases.

Table 35: Audio Header (JH) Pinout

JH Header Pin Number	SoC Signal Name	Header Signal Definition
JH.1	NA	V5DX_AUDIO_JH
JH.2	NA	V5DX_VBATA_AUDIO_JH
JH.3	NA	RESERVED(key)
JH.4	NA	GND
JH.5	GPP_B_13_PLTRST_B/GPP_V_4_SLP_S3_B/PRIM_VR_BFR_OUT	PLT_RST_PWREN_HDR
JH.6	GPP_D_9_I2S_MCLK1_OUT MIC_PRIVACY_HDR/GPP_V_7_SUSCLK	MIC_PRIVACY_I2S_MCLK_SUS_CLK_HDR

12.3.5 JS Header (On-board audio codec DMIC & SPKR Header)

New 12-pin header JS header is used to connect on-board ALC722 codec DMIC and SPKR load using Y-cable on transducer AIC. It can drive 4xDMIC & 2 SPKR's.

Table 36: Audio Header (JS) Pinout

JS Header Pin Number	Codec Pin Name	Header Signal Definition
JS.1	DMIC_CLK	CODEC_DMIC_CLK_HDR
JS.2	DMIC_DATA12	CODEC_DMIC_DATA12_HDR
JS.3	NA	GND
JS.4	NA	+V1P8DX_DMIC_JS_HDR
JS.5	NA	GND
JS.6	DMIC_DATA34	CODEC_DMIC_DATA34_HDR
JS.7	NA	GND
JS.8	NA	RESERVED(key)
JS.9	SPK_OUT_L+	CODEC_SPKR_OUT_L_P_HDR
JS.10	SPK_OUT_L-	CODEC_SPKR_OUT_L_M_HDR
JS.11	SPK_OUT_R+	CODEC_SPKR_OUT_R_P_HDR
JS.12	SPK_OUT_R-	CODEC_SPKR_OUT_R_M_HDR

12.4 Privacy Microphone Protection Feature

Privacy microphone protection feature is POR in WCL RVP.

The ACE (Audio Context Engine) IP offers a microphone privacy protection scheme through a HW DMA (Dynamic Memory Access) data zeroing mechanism if parameter (Microphone Privacy Enable) MICPVCE = 1.

The HW will take in a privacy signaling input from the GPIO pin (which typically connects to a mic disable switch), indicating the current user privacy mode setting on the system.

If the mic disable switch is turned on, and the DfMICPVCP.DDZE policy register indicates privacy mode is enabled, the HW will interrupt DSP FW (if link management is offloaded) / host SW (if link management is not offloaded) indicate the mic disable entry (allow DSP FW / host SW to gracefully [the audio capture stream without any audible glitches), and then mask the data from the microphone to zeros after a time-out period programming in DfMICPVCP.DDZWT register. It also turns on a privacy indicator output through the GPIO pin (which typically connects to a privacy LED).

When the mic disable switch is turned off later, the HW will unmask the data from the microphone (immediately) and interrupt DSP FW indicating the mic re-enabling (allow DSP FW / host SW to gracefully unmute), as well as turning off the privacy LED indication through the GPIO pin.

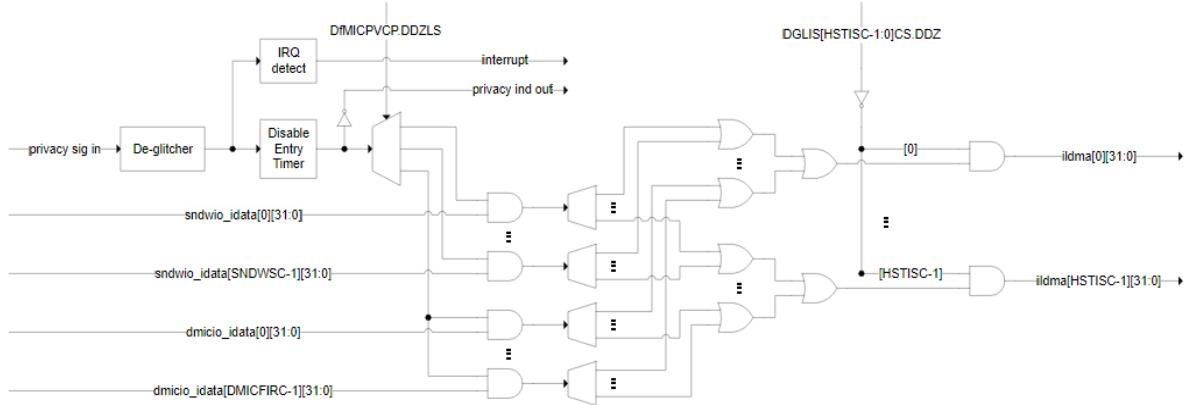


Figure 36: Privacy microphone protection conceptual diagram

Reference :

https://docs.intel.com/documents/iparch/ace/ACE%20IP/3.x/Integration%20Specs/WCLSM/WCLSM_ACE3.x_Integration_HAS.html#privacy-microphone-protection

Below table represents the **privacy sig in & privacy ind out** signal description.

SIGNAL NAMES	TYPE	DESCRIPTION
PVC_SIG_IN	I	Privacy Signaling Input: Privacy microphone disable signaling input, typically for connection to a switch. Asserted high to indicate the microphone disabled state (HW will ensure the data output from the microphone is masked to zero).
PVC_IND_OUT	O	Privacy Indicator Output: Privacy microphone disable indication output, typically for connection to an LED. Asserted high to indicate the microphone disabled state (after HW has masked the data output from the microphone to zero).

Figure 37: Privacy microphone protection signal description

Note: These pins are typically associated with DMIC interface, but also usable by microphone connected over SoundWire interfaces.

WCL RVP uses SoC pins MIC_MUTE and MIC_MUTE_LED to support microphone privacy protection. The below diagram represents RVP implementation.

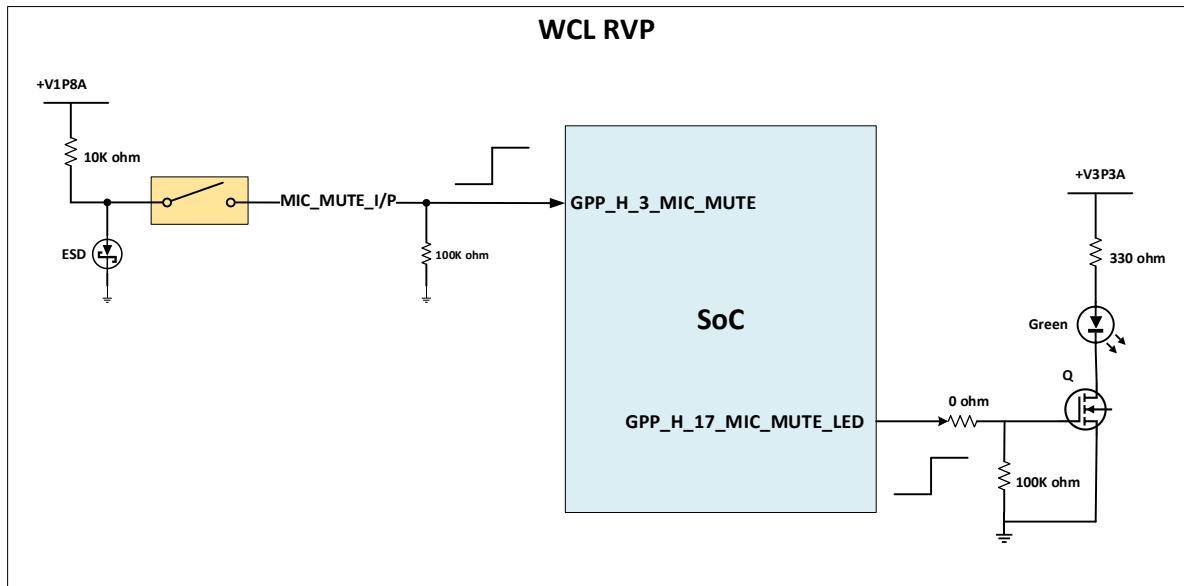


Figure 38: WCL RVP audio MIC privacy support block diagram

The following table represents MIC privacy operation through SoC pins using DIP switch control as supported in WCL RVP.

SIGNAL NAME	DESCRIPTION
GPP_H_3_MIC_MUTE	Mic mute - Indicate the user privacy mode setting on the system (ON : gate the clock to the mic, OFF : ungate the clock to the mic)
GPP_H_17_MIC_MUTE_LED	Mic mute led- Led to Indicate the user privacy mode setting on the system. (ON : gate the clock to the mic, OFF : ungate the clock to the mic)

Figure 39: WCL RVP MIC privacy feature SoC signal description

Refer below table for MIC mute operation using DIP switch control.

MODE	DIP SWITCH POSITION	LED INDICATION
MIC mute OFF - Default	OFF - OPEN	OFF
MIC mute ON	ON - CLOSED	ON (Green)

13 Serial Interfaces- SPI, eSPI, SMBus, SM Link, MLink/CLink

This chapter discusses about the various serial interfaces namely SPI, eSPI, THC-SPI, SMBus, SMLink, MLink. The SPI, eSPI and THC-SPI are functionally similar IPs. The mapping of all serial ports is as shown below. The mapping is subjected to change based on the inputs from design or validation teams.

Notes:

1. For probing these signals, test points will be provided by opening the via masks on the SOC side. For the device side, series resistors or pull ups close to the device will be used for probing. If there are no components available near the end device for probing, then the test points will be provided closest to the device. However, if the test points are adding additional vias and violate the SI guidelines, then test points will not be provided.
2. For all the serial interfaces, for only one of the ports, A dummy test structure consisting on VCC pull up resistor (empty), load capacitor to ground(empty) and 0-ohm series resistor(populated) sharing pads as close as possible to SOC side and device side will be implemented.
3. Following options are not provided on RVP for any of the LPSS / ISH / Serial interfaces: TLA footprint, midbus probes, Beagle headers, Aardwark support.
4. The mapping of ports and GPIOs will be same for all the RVP SKUs to ease software effort. Deviations will be mentioned in the specific sections.

13.1 SPI & THC SPI Ports

The WCL SOC provides Serial Peripheral Interfaces (SPI) for connecting BIOS Flash, TTK3 and TPM. Which is 1.8V IO voltage only with maximum speed of 50MHz.

The SPI0 (CSME SPI) interface consists of 3 chip-select signals. It is allowing up to two flash memory devices (SPI0_CS0# and SPI0_CS1#) and one TPM device or TTK3 device (SPI0_CS2#) to be connected to the SOC working in quad-mode. The SPI0 interfaces support 1.8V only.

A rework option would be provided for the 32MB SPI flash part working at 100MHz, 1 Load only on the SPI0 bus.

Legacy touch can be supported from GSPI. But since THC is POR for WCL, only THC based touch connections will be provided on RVP. GSPI based touch support is not provided.

The GPIO interface is multiplexed with THCO, implementing one Chip Select signal (SPI0_CS#) and is intended for integrated touch implementation, also working in quad-mode. GPIO supports 1.8V only. THC/I2C/GSPI signals are all muxed internally in the PCH as a HID device port (there are 2 HID ports on WCL) and will be programmable through the BIOS GPIO Configuration (as alternate functions). This requirement is no board reworks needed to switch among bus selection within the same HID port, HID port definition was introduced in ADP-LP.

Refer to the BIOS Flash Interface (SPI) section for detailed explanation on the Flash sharing mechanisms.

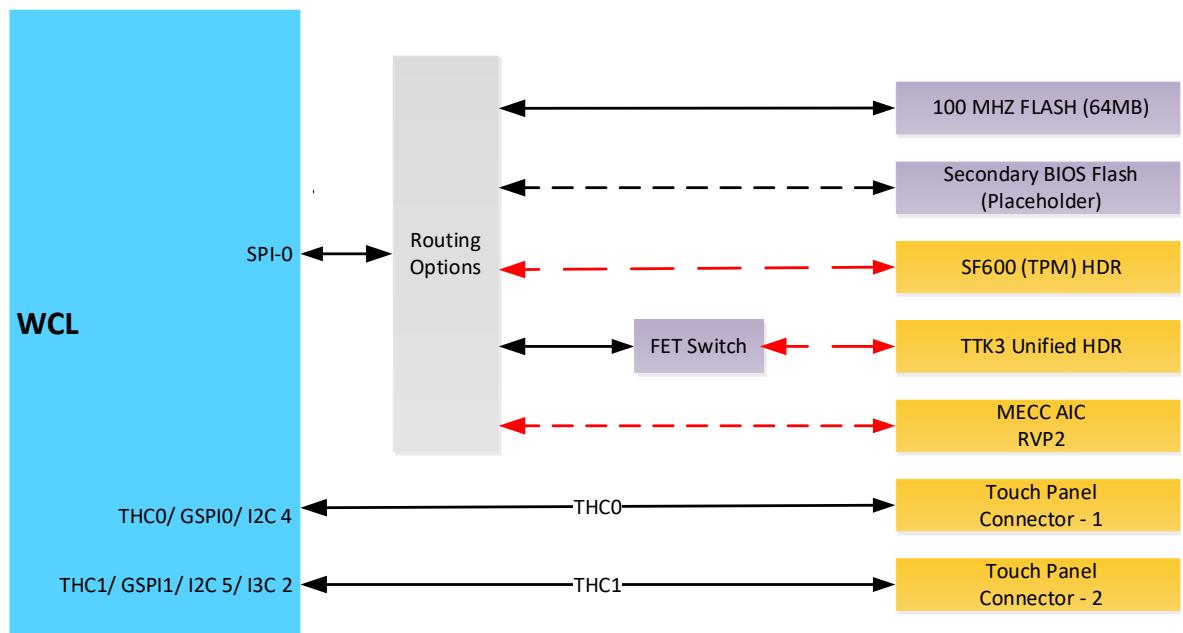


Figure 40: WCL RVP SPI & THC SPI Interface support

13.2 eSPI Port

The PCH eSPI (Enhanced SPI) controller supports the following features:

- Support for 20MHz, 25MHz, 33MHz and 50MHz bus operation.
- 1.8V support only
- Up to quad mode support with 2 Chip Select signals.
- In-band messages for communication between the SOC and slave device to eliminate side-band signals
- Real time SPI flash sharing, allowing real time operational access by the SOC and slave device.
- MAF & SAF modes
- PECl over eSPI

On WCL RVP, eSPI interface is for the communication between EC and SOC. This port can run at max of 50MHz and IO voltage is 1.8V. The eSPI pins will be routed to ESPI Bus Header with appropriate reworks.

eSPI also has an option, as illustrated in the figure below to be connected to the MECC connector for other EC support and eSPI bus header.

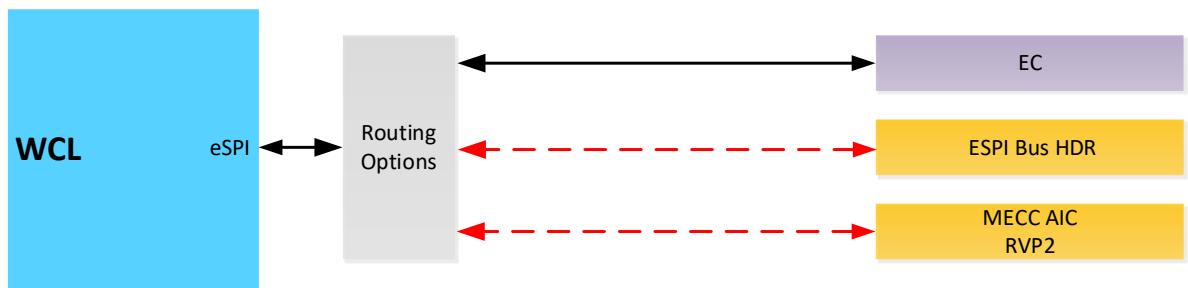


Figure 41: WCL RVP eSPI Interface support

13.3

SMBus & SMLink

SMBus Controller IP is SMBus 2.0 compliant and provides a mechanism for the SOC to initiate communications with the SMBus peripherals (slaves) or allows external attached peripherals to write or read to the SoC. SMBus controller supports 100 kHz, 400 kHz, 1 MHz operation.

On WCL RVP, the SMBus is interfaced to PCIe Slot, Memory SPD (SODIMM), PSS EEPROM, FRU EEPROM, ESPI Bus Header, SOC MIPI60 Connector, PM Side Band Header using a SMBUS Bus expander. Figure 42 gives the list of devices on the SMBUS and their read/write addresses.

SOC implements 2 SMLink controllers for the 3 SMLink interfaces, SMLink0, SMLink0B and SMLink1. The interfaces are intended for system management and are controlled by the Intel® ME. And they can run at frequencies up to 1MHz.

On WCL SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.

SMLink0 is routed to Jacksonville, x4 PCIe Slot, USB-C Connector and. SMLink0B is routed to TBT Retimer, USB-C Connector, MECC and EC on WCL RVP. SMLink1 is routed to PM Sideband Header, MECC and PD A

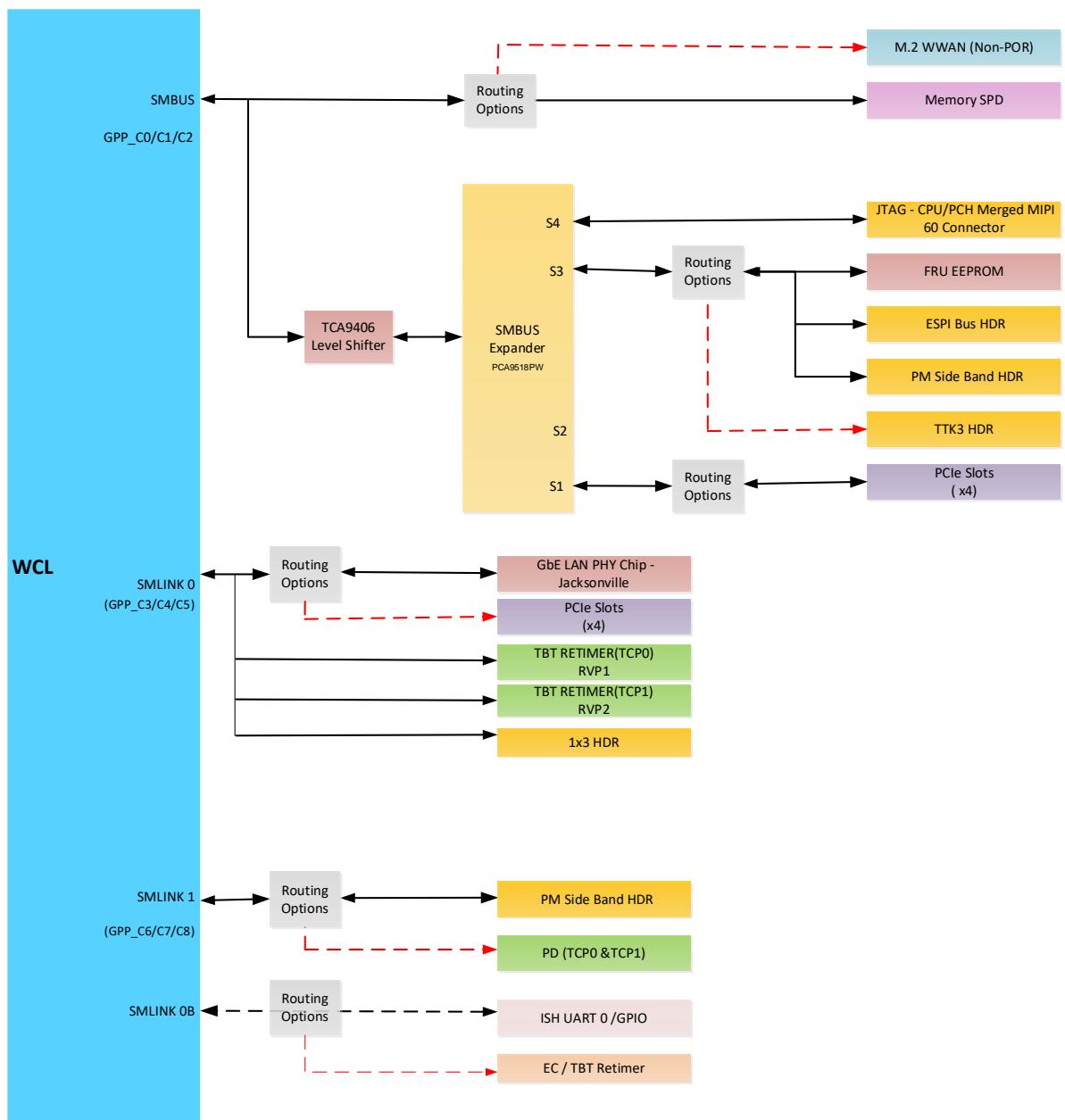


Figure 42: WCL RVP SMBus & SMLink support

13.4

MLink / CLink

M-Link interface is the management communication link between the SOC and Intel Wireless cards. It enables Manageability to support low power interface of Intel WiFi network interfaces. Supported in S0 and Sx power states. Single Clink controller to connect to external C-link device or as a internal C-link connection with CNVi.

Note: Clink has also been called Manageability link (MLink) in some documentation

The M.2 WLAN card Link Status can be monitored with help of C-Link signals from the M.2 Module. The signal routing option is provided through a tri-pad, to the WLAN module, 2x4 Header and SOC.

Table 37: CLink Interface Signals

Signal Name	Type	Description
CL_RST#	O	Wi-Fi* CLINK host bus reset for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK reset pin on the Intel® vPro™ Wi-Fi* module.
CL_DATA	I/O	Wi-Fi* CLINK host bus data for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.
CL_CLK	O	Wi-Fi* CLINK host bus clock for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

14 Embedded Controller

WCL RVP will support MEC1723 Microchip Embedded Controller (EC) onboard. MEC1723 supports ESPI mode of operation. LPC mode will not be supported in WCL. EC controls the preliminary platform power sequencing and does system and power management. EC is the platform thermal controller that monitors and throttles CPU or controls CPU Fan. The key functionalities of EC on the platform are illustrated in below figure.

Note: EC part (144-pin WFBGA package) used in WCL design is **MEC1723NB0-I/SZ**

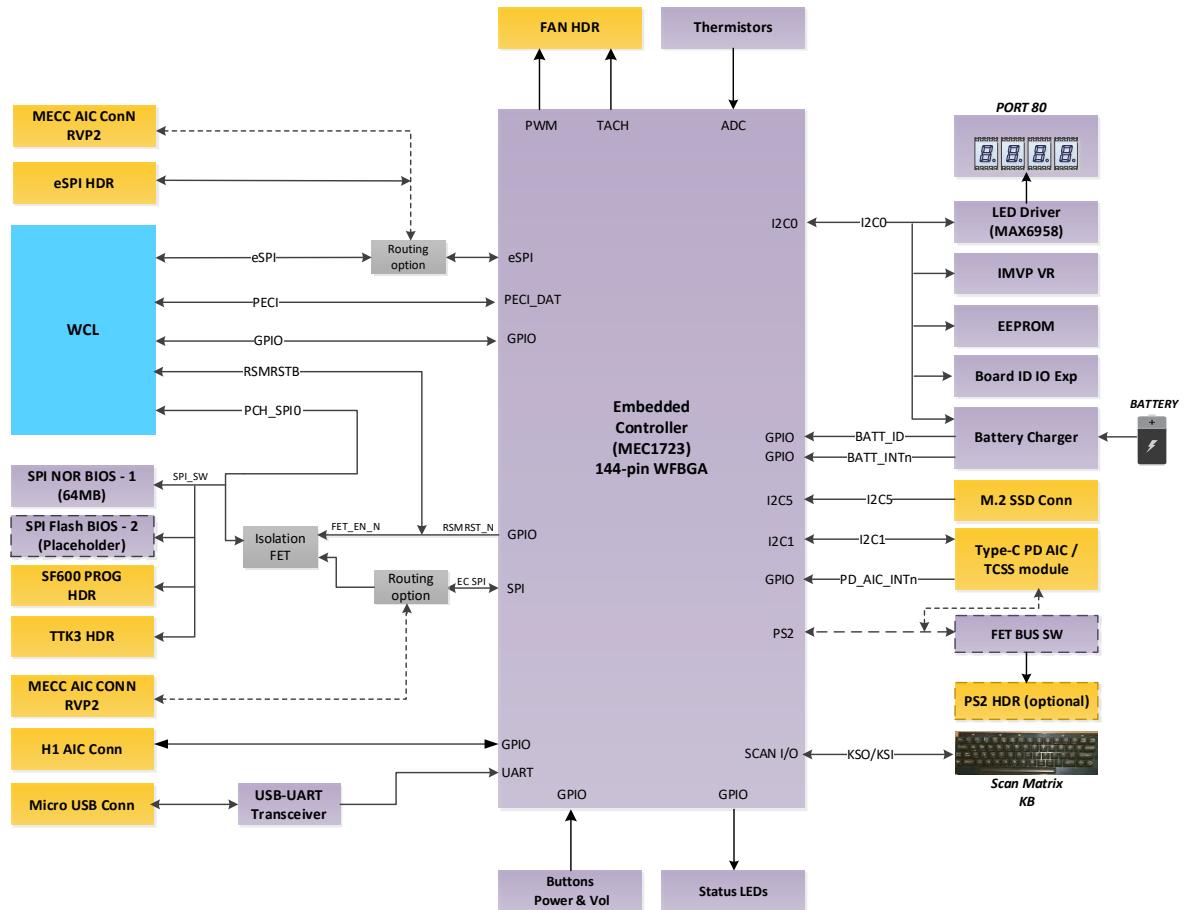


Figure 43: Embedded Controller Block Diagram

The EC subsystem consists of:

- Thermal Management functions like CPU Fan control, Chassis Fan control, PECI, DIMM temperature etc.
- Platform Power management like Power sequencing, Sx and Deep Sx entry/exits.
- Any CEC specific Modern Standby requirements to be implemented inside EC
- Handles the Board-ID, Fab-ID, BOM SKU-ID, messages to the BIOS.
- RVP design will support all three i.e., SAF, MAF, G3 Flash configuration, default will be MAF.
- 2x14 pin eSPI header will also be supported.
- Switching between MAF / SAF / G3 will be through resistors only. No jumper can be provided as it impacts SI and leads to Signal Integrity issues.
- Separate PMR resistors will be added for 1.8V and 3.3V rails going to EC.
- EC GPIO mapping yet to be updated and shared with EC team.
- MECC connector will be supported for validating the EC from different vendors.

External PS2 Keyboard alone will be supported.

The RVP supports LED for CAPSLOCK, NUMLOCK and SCROLL LOCK. The EC error code table with on-board LED status is given below.

Table 38: EC error code indication

Error type	Error code	Caps Lock LED	Scroll Lock LED	Num Lock LED
No Error	0	Off	Off	Off
RSMRST#_PWRGD	1	Off	Off	Flash
PM_SLP_S5#	2	Off	Flash	Off
PM_SLP_S4#	3	Off	Flash	Flash
PM_SLP_S3#	4	Flash	Off	Off
PM_SLP_A#	5	Flash	Off	Flash
ALL_SYS_PW_RGD	6	Flash	Flash	Off
PLTRST#	7	Flash	Flash	Flash

It is to be noted that,

- KSC Thermal Shutdown is indicated by flashing of Num_Lock and Caps_Lock LEDs alternatively.
- The above errors are displayed by EC on Port80 as EC 01 to EC 07. These errors are not EC errors, and these errors represent the platform status.

14.1

MECC AIC Support

MECC AIC connector(200-pin) is supported for windows RVP for validating the external EC over AIC. Chrome BoM SKU is supported through onboard Chrome AVL EC MEC1727N-B0-I/SZ-CHR0 part.

Chrome SKU doesn't support the MECC AIC option. Chrome SKU uses H1 & Servo AIC same as MTL-P for Chrome SKU.

Note: MECC connector is supported only on RVP2(LP5x T3 MECC RVP2) SKU. It is not supported on all other RVP SKUs.

Table 39: MECC Connector

MFG	Mfg. Part Number	IPN Number
Amphenol	84535-191LF	N15428-001

MECC connector pinout details are shared over [Link](#)

14.2

Flash Sharing

WCL RVP supports both MAF, SAF and G3 flashing configuration. There is no dedicated Flash to EC. SOC GPIO is used for flash selection strap pin refer Pin strap section for more details.

EC shared flash (SOC SPI NOR).

- Shared SPI Flash: Currently a Composite image. Update is done by BIOS. Top swap allows recovery.
- Slave Attached EC Flash. Lot of security features in EC. (Apple uses EC as a root of trust, Google uses BIOS based root of trust)).

14.3 EC – I2C IO Expander

I2C based IO expanders are provided to handle Board-ID, Fab-ID, BOM SKU-ID and some IO requirement. EC I2C mapping is provided in the below table.

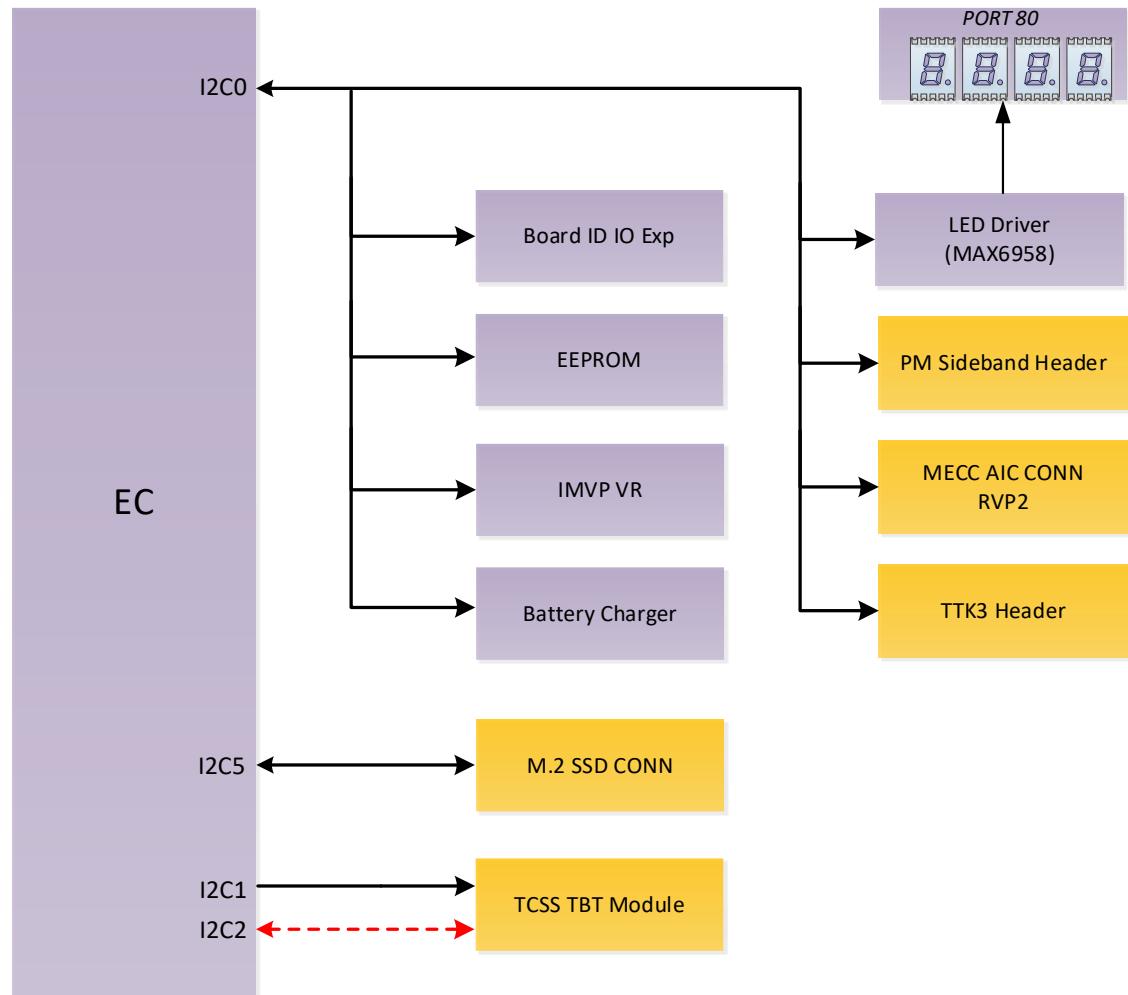


Figure 44: EC- I2C Block Diagram

14.4

EC – Headers

Below sections includes connector and pinout details of the connectors used in EC section.

14.4.1

eSPI Sideband Header

Table 40: eSPI Sideband Header and Pinout

MFG	Mfg. Part Number	IPN Number
Samtec	ASP-175166-01	H46981-001

Signal Name	Pin #	Pin #	Signal Name
ESPI_CLK_HDR	1	2	GND
ESPI_CS0_HDR_N	3	4	NO PIN
SHM_TRIG_PLT_RST_R	5	6	+V5A_VAL
ESPI_IO3_HDR	7	8	ESPI_IO2_HDR
+V3P3A_VAL	9	10	ESPI_IO1_HDR
ESPI_IO0_HDR	11	12	GND
SMB_CLK_S3	13	14	SMB_DATA_S3
+V3.3A_1.8A_R1 TPM	15	16	ESPI_CS1_HDR_N
GND	17	18	TP_GPPC_A8_CLKRUN_R_N
ESPI_RST_HDR_N	19	20	ESPI_ALERT0_HDR_N
NO PIN	21	22	NO PIN
ESPI_ALERT1_HDR_N	23	24	GPPC_E7_EC_SMI_N
TP_GPP_A8_CLKRUN_R_N	25	26	TP_EC_RSVD
+V5A_VAL	27	28	TP_PASL_DRQ1_N

14.4.2

PS2 KB HEADER (Optional)

Table 41: PS2 KB and Pinout

MFG	Mfg. Part Number	IPN Number
SAMTEC	TSM-105-01-G-SV-P-TR	K88184-001

Pin #	Signal Name
1	PS2_KB_CLK_FB
2	+V5_PS2
3	GND
4	GND
5	PS2_KB_DATA_FB

14.4.3 Scan Matrix Keyboard Header

Table 42: Scan Matrix Header and Pinout

MFG	Mfg. Part Number	IPN Number
Ipex	20542-028E-01	H24635-001

Pin #	Signal Name
1	KBC_SCANIN<6>
2	KBC_SCANIN<0>
3	KBC_SCANIN<1>
4	KBC_SCANOUT<6>
5	KBC_SCANIN<3>
6	KBC_SCANIN<2>
7	KBC_SCANOUT<15>
8	KBC_SCANIN<5>
9	KBC_SCANIN<4>
10	KBC_SCANOUT<10>
11	KBC_SCANOUT<14>
12	KBC_SCANIN<7>
13	KBC_SCANOUT<13>
14	KBC_SCANOUT<11>
15	KBC_SCANOUT<8>
16	KBC_SCANOUT<7>
17	KBC_SCANOUT<9>
18	KBC_SCANOUT<12>
19	KBC_SCANOUT<3>
20	KBC_SCANOUT<2>
21	KBC_SCANOUT<1>
22	KBC_SCANOUT<4>
23	KBC_SCANOUT<5>
24	KBC_SCANOUT<0>
25	LED_NUMLOCK
26	LED_CAPSLOCK
27	+V3.3A_KBC
28	NC

14.4.4 Keyboard Backlight Header

Table 43: KB Backlight Header and Pinout

MFG	Mfg. Part Number	IPN Number
Ipex	20542-006E-01	H24575-001

Pin #	Signal Name
1	+V5S_KBD_BKLT
2	+V5S_KBD_BKLT
3	NC
4	NC
5	KBD_BKLT_CTRL_FET
6	KBD_BKLT_CTRL_FET

14.4.5 Fan Header

Table 44: Fan Header and Pinout

MFG	Mfg. Part Number	IPN Number
Molex	51021-0400	A36295-009

Pin #	Signal Name
1	FAN_CONN_PWM_IN
2	CPU_TACHO_R_FAN
3	GND
4	+V5_FAN_SUPPLY

14.5 Front Panel Header

Table 45: Front Panel Header and Pinout

MFG	Mfg. Part Number	IPN Number
WIESON TECHNOLOGIES CO., LTD	AC2100-0009-042-HH	K96810-001

Signal Name	Pin #	Pin #	Signal Name
FRONT1(Pull up to 5V)	1	2	FRONT2 (Pull up to 5V)
TP_SATA_LED_N	3	4	GND
GND	5	6	PWR_CONN_D
RST_PUSH_N_D	7	8	GND
+V5A_VAL	9	10	Key
NC	11	12	GND
GND	13	14	Key
BC_ACOK_DSW	15	16	+V5A_VAL

14.6

PM Sideband Header

Table 46: PM Sideband Header

MFG	Mfg. Part Number	IPN Number
Molex	87832-4020	C12536-002

Signal Name	Pin#	Pin #	Signal Name
PM_PWRBTN_N	1	2	ALL_SYS_PWRGD
PM_RSMRST_N	3	4	SMB_BS_DATA_PORT80_R
PM_SLP_S5_N	5	6	SMB_BS_CLK_PORT80_R
PM_BATLOW_N	7	8	
PM_SLP_S3_N	9	10	SIDEBOARD_TIME_SYNC_0
PM_SLP_S4_N	11	12	SML1_DATA_R
+V3P3A	13	14	SML1_CLK_R
EDM_SOC_IOE_PM_HDR	15	16	GND
RTC_RST_N	17	18	EDM_BASE_PM_HDR
SMC_WAKE_SCI_N	19	20	EDM_GCD_PM_HDR
	21	22	BC_ACOK_EC_IN
PS_ON_SW_N	23	24	PM_SLP_A_N
	25	26	PM_PCH_PWROK
	27	28	SRTC_RST_N
	29	30	RSMRST_PWRGD_N
PM_SYSRST_N	31	32	PM_SLP_SO_N
+V1P8A	33	34	BUF_PLT_RST_N
SMB_DATA_S3_J	35	36	SYS_PWROK
SMB_CLK_S3_J	37	38	EDM_CORE_PM_HDR
+V3P3S_VAL_J	39	40	+VRTC_BATT

15 BIOS Flash Interface (SPI)

WCL RVP supports native SPI interfaces SPI0. The SPI0 is used for flash and TPM while THC SPI1 and THC SPI2 are used for Touch interface.

WCL RVP supports 1.8V 64MB flash on SPI0 interface. Windows RVP will use 1x 64MB part default and Chrome RVP will use 64MB default.

TPM AIC should be plugged into the same header used for BIOS flashing on SPI0.

WCL RVP will support 1.8V compatible SPI devices for MAF/SAF and G3 mode. RPMC for 1.8V devices will be default supported on WCL RVP. SPI devices will support 100MHz clock rates. No 3.3V SPI support from WCL SOC.

Default Device supported on RVP will be 64MB 1.8V with RPMC. Jumper for Flash Descriptor Override will be supported. Also, RVP allows to boot the platform while Dediprog SF600/SF100 programmer is connected to the platform.

WCL RVP has placeholder for second flash on SPI0 to support dual flash topology which is not POR.

The SPI0 interface of SOC is shown in below diagram.

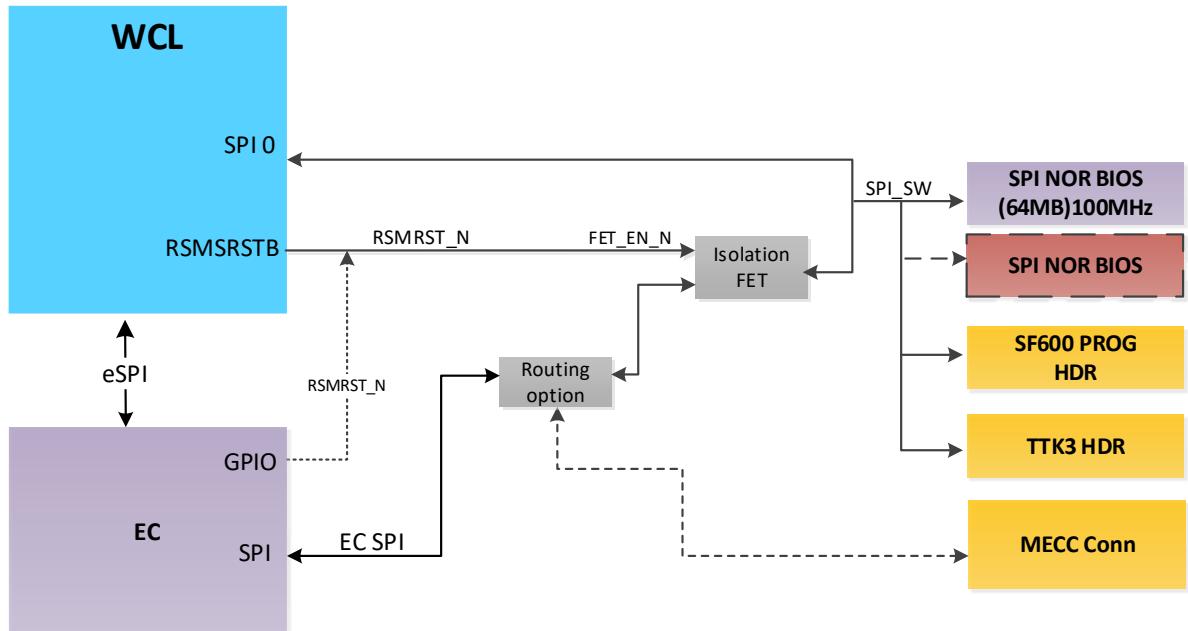


Figure 45: BIOS Flash interface (SOC-SPI0)

NOTE: WCL SPI0 buffer type is Fail Safe Buffer so isolation FET needed from SoC to Flash especially in SAF and G3 Flash Sharing configuration.

15.1

EC Flash Topology

EC FW image is stored in either external SPINOR or embedded flash. The embedded flash should have enough space to store the entire FW and any Non-Volatile data. ECs without embedded flash requires an external SPI flash, either dedicated or shared with SOC. Three types of flash sharing mechanisms shall be supported on WCL RVP designs.

- G3 flash sharing
- MAF - Master attached flash sharing <default option for platform default>
- SAF - Slave attached flash sharing.

WCL RVPs shall support all the flash sharing mechanisms. Reworks change into SAF or G3 from MAF will be minimized comparing to previous RVPs.

15.1.1

G3 Flash Sharing

In this mechanism, the SPI lines from flash part are connected to both SOC and EC either directly or switch. Due to security concerns and flash access limitation, this is the least recommended option in all the flash sharing mechanisms.

- The RSMSRST# from EC is used for controlling the flash access and switched only once during G3 exit.
- EC accesses the SPINOR only when RSMSRST# is asserted and tri-states the SPI lines on de-assertion.
- On G3 exit (with RSMSRST# asserted) EC loads the entire image in its internal SRAM and releases RSMSRST# for SOC to access the flash. This doesn't require eSPI to be operational.
- Some isolation FETs required if SOC doesn't tristate the lines when RSMSRST# is asserted.

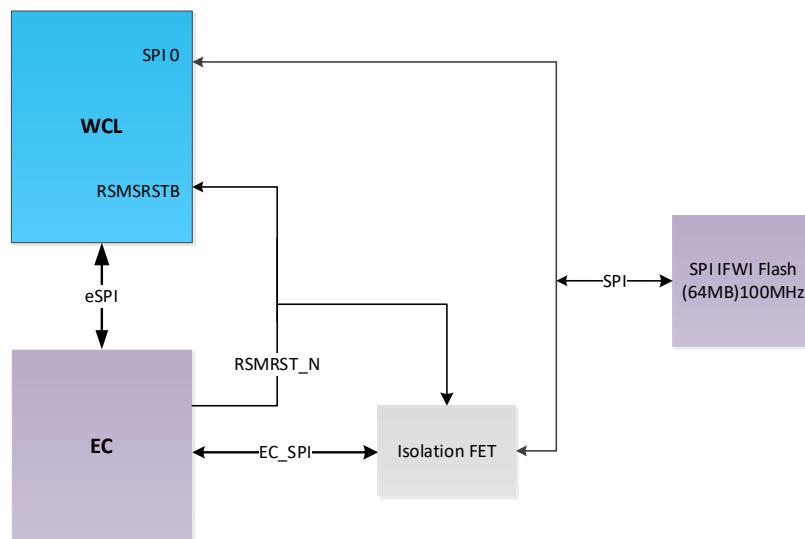


Figure 46 : G3 Flash Sharing high level block diagram

15.1.1.1 Flash update

- Requires host to update the EC region in shared SPINOR without EC involvement.
- Update is like any other OEM regions like BIOS.
- Host can support Full image update or EC region update.
- UEFI Capsule update is the minimum requirement with BIOS signature verification.
- FW recovery
 - Intel SOC is not responsible for EC FW recovery.
 - OEMs may support through alternate options
 - Use other interface that is active in S5 (typically used in service center)
 - Implement non updatable block (ROM) in EC that brings up the system to S0 for flash update.

15.1.1.2 Master Attached Flash Sharing (MAF)

MAF is one of the Flash sharing mechanisms where SOC is the master which access flash over SOC SPI Controller and EC sharing the same flash will access over eSPI. MAF will be default the configuration for the WCL.

Here the SPI flash is connected to SOC and EC accesses the flash over eSPI.

- Requires eSPI interface to be up and initialized by both SOC and EC.
- On G3 exit, EC de-asserts RSMRST#(GPIO055), initializes eSPI, reads its image from SPINOR over eSPI, loads into its internal SRAM and notifies PCH. This is handled by the ROM in EC chip before giving control to the downloaded FW image.
- The downloaded flash image continues the power sequencing until SOC is out of reset and BIOS starts executing.
- This flash sharing mechanism also allows access during runtime which is handled by the downloaded EC FW image.
- Soft strap in descriptor to restrict EC to access EC FW region only.
- EC image Offset 1000H.

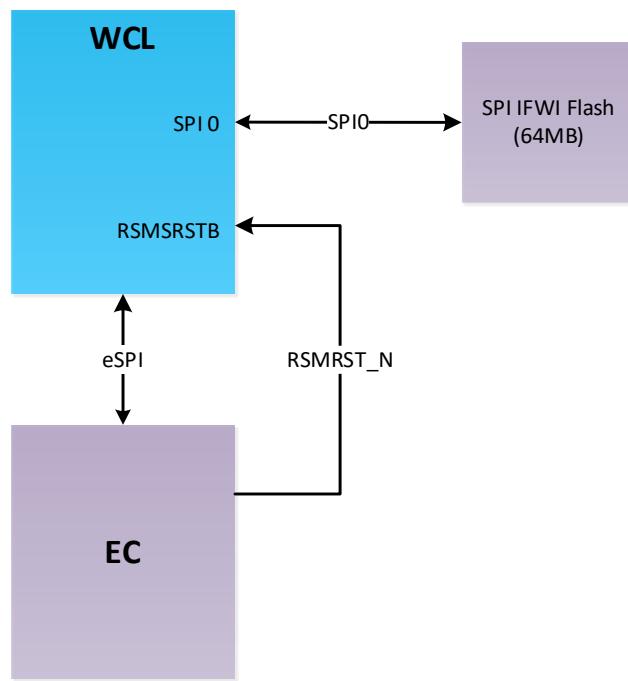


Figure 47 : MAF high level block diagram

15.1.2 Slave Attached Flash Sharing (SAF)

SAF is one of the Flash sharing Mechanism where EC is the master which access flash over its SPI Controller and PCH sharing the same flash will access over eSPI. MEC1723 Microchip Embedded Controller can support SAF mode flashing. Rework is required on RVP to support SAF.

WCL SOC is allocated dedicated regions (for each of the supported masters) within the eSPI slave-attached flash devices. SOC has read, write, and erase access to these regions, as well as any other regions that maybe permitted by the region protections set in the Flash Descriptor. The Slave will optionally perform additional checking on SOC provided address. In case of an error due to incorrect address or any other issues it will synthesize an unsuccessful completion back to the eSPI Master.

The SAF supports Flash Read, Write and Erase operations. It also supports the RPNC, Read SDFP and Read JEDEC ID commands.

In this topology, the SPI flash is connected to EC and SOC accesses the flash over eSPI.

- On G3 exit, EC loads its entire image into its internal SRAM, verifies the image (if supported as root of trust), and then de-asserts RSMRST# for PCH/SOC to access flash over eSPI.
- EC must meet the timing requirements for the SAF to avoid FW access latencies to avoid any impact to responsiveness or boot time.
- EC should enable the access to regions based on soft straps in the descriptor.

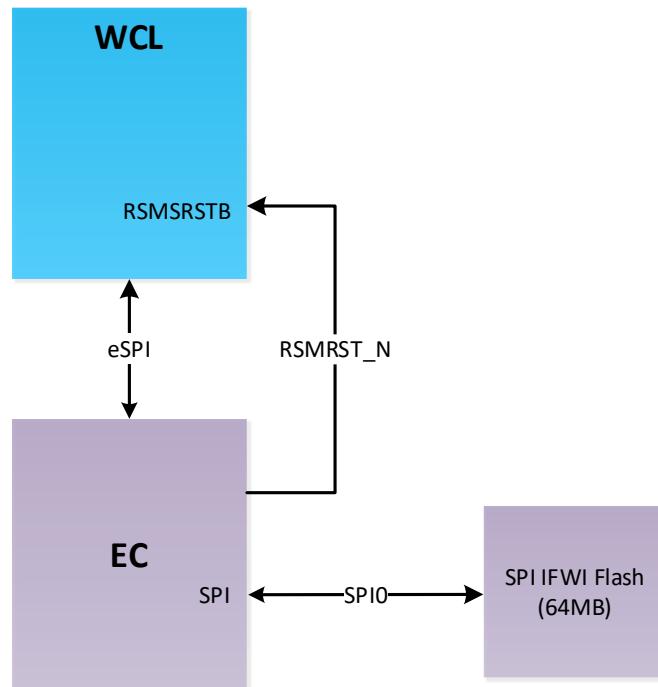


Figure 48 : SAF high level block diagram

16 Low Power Sub Systems (LPSS)

Initial allocation of each port is given in the block diagram of the respective sub-sections.

Disclaimer: The LPSS architecture is yet to be finalized. There are changes expected, and same will be updated.

Notes:

1. For probing these signals, test points will be provided by opening the via masks on the SOC side. For the device side, series resistors or pull ups close to the device will be used for probing. If there are no components available near the end device for probing, then the test points will be provided closest to the device. However, if the test points are adding additional vias and violate the SI guidelines, then test points will not be provided.
2. For all the serial interfaces, for only one of the ports, A dummy test structure consisting of VCC pull up resistor (empty), load capacitor to ground(empty) and 0-ohm series resistor(populated) sharing pads as close as possible to SOC side and device side will be implemented.
3. Following options are not provided on RVP for any of the LPSS / ISH / Serial interfaces: TLA footprint, midbus probes, Beagle headers, Aardwark support.
4. The mapping of ports and GPIOs will be same for all the RVP SKUs to ease software effort. Deviations will be mentioned in the specific sections.

16.1

I2C/I3C

The SOC implements 6 I2C controllers for 6 I2C interfaces (I2C0-I2C5), capable of maximum bit rate of 3.4 Mbps (High-speed mode). Each interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock (SCL). The following are the constraints considered for I2C mapping:

1. Camera sensors and touch screen / touch pad cannot be on the same I2C bus.
2. Each camera connector needs a separate I2C bus to avoid address conflict since all the camera sensors have same I2C address. In older platforms the address conflict is resolved by doing a rework and a software work around. But on WCL this needs to be fixed. Hence allocating one I2C per camera connector in WCL RVP.

Each I2C interface can support the following Speed & power options:

- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- Fast mode plus (up to 1 Mbps)
- High speed mode (up to 3.4 Mbps)
- 1.8V support only

WCL supports 3- I3C interfaces and I3C interface.

- Support backward compatibility for Fast Mode and Fast Mode Plus. Slave device clock stretching is not supported.
- Single Data Rate (SDR) 12.5 Mbps, Dual Data Rate (DDR) 25 Mbps
- Support In-band Interrupt (IBI)
- Support Hammock Harbor time synchronization

Table 47: I2C/I3C device mapping

Bus	Device Mapping
I3C (Debug BPK I3C)	Modular TCSS TCP0 I3C Debug
I2C 0/ I3C 0	1X3 HDR as I2C0
I2C 1/ I3C 1	SV DIPSW HDR /MECC AIC as I2C1
I2C 2/ MFUART 2	M.2 WLAN MFUART 2
I2C 3/ UART1/ ISH UART1A	Track PAD/ Audio/ PSS/ Power meter/TTK3/EDP
I3C 3A/ Display Sideband	Display sideband GPIO
I2C 4/ THC	Touch Panel Con 1 (I2C & THC mode)
I2C 4A/ ISH I2C 2/ MFUART0	M.2 WLAN MFUART 0 / ISH HDR as ISH I2C2
I2C 5/ THC	Touch Panel Con 2 (I2C & THC mode)
I2C 5A/ MFUART 0/ ISH GP	ISH GPIO's

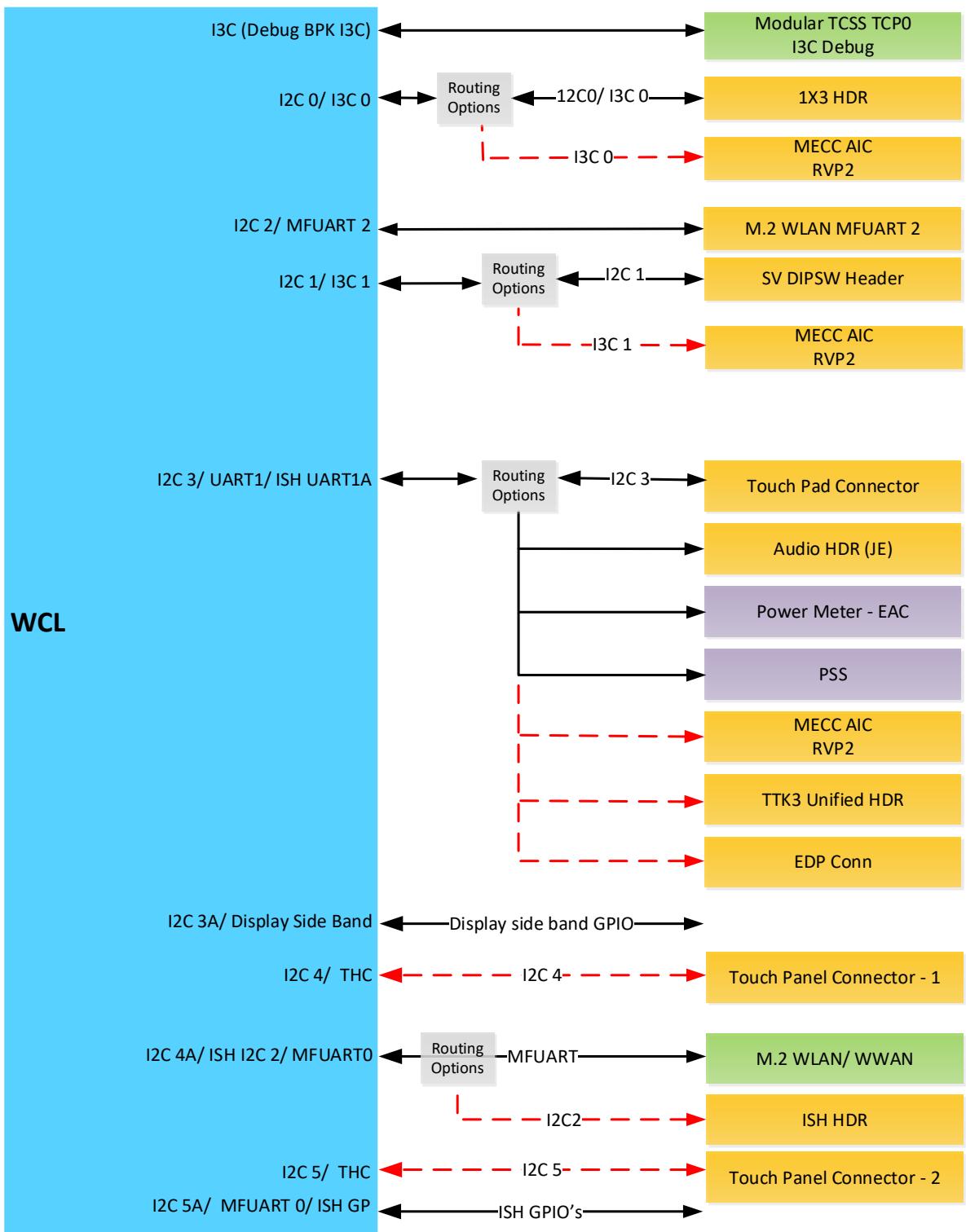


Figure 49: LPSS I2C/I3C high level Block Diagram

16.1.1 I2C Device Details

The table below provides the devices connected to the LPSS I2C/I3C subsystem.

Table 48: I2C/I3C device details

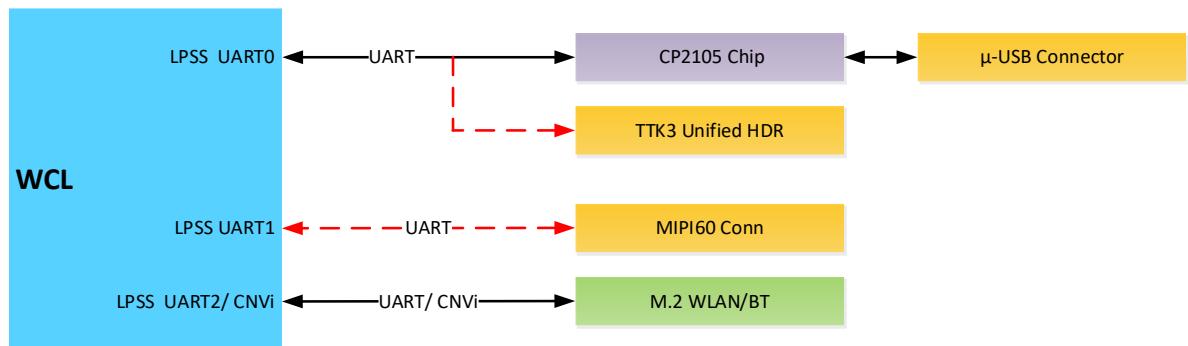
Device	Speed	7 Bit address Set	7 Bit Address Options	I2C IO Voltage
Touch Pad	400KHz	0x2C	0x2C	3.3V
Touch Panel-2	400KHz/ 1MHz	0x5C (General Study)	0x5C	1.8V
Touch Panel-1	400KHz/ 1MHz	0x5C (General Study)	0x5C	1.8V
PSS	400KHz	0x6E	0X68 or 0x6A or 0X6C or 0X6E	1.8V
Power meter Chip#1	100KHz/ 400KHz/ 1MHz (FM+)	0x18	Configurable through resistor	1.8V
Power meter Chip#2	100KHz/ 400KHz/ 1MHz (FM+)	0x1E	Configurable through resistor	1.8V
Power meter Chip#3	100KHz/ 400KHz/ 1MHz (FM+)	0x11	Configurable through resistor	1.8V
Power meter Chip#4	100KHz/ 400KHz/ 1MHz (FM+)	0x15	Configurable through resistor	1.8V
Power meter Chip#5	100KHz/ 400KHz/ 1MHz (FM+)	0x13	Configurable through resistor	1.8V
Power meter Chip#6	100KHz/ 400KHz/ 1MHz (FM+)	0x12	Configurable through resistor	1.8V
Power meter Chip#7	100KHz/ 400KHz/ 1MHz (FM+)	0x16	Configurable through resistor	1.8V
Power meter Chip#8	100KHz/ 400KHz/ 1MHz (FM+)	TBD	Configurable through resistor	1.8V
Power meter Chip#9	100KHz/ 400KHz/ 1MHz (FM+)	TBD	Configurable through resistor	1.8V
CONNECTIVITY - GBIT LAN - JACKSONVILLE LAN PHY CHIP		0xC8 (Read) , 0xC7 (Write)		3.3V
FRU EEPROM	100KHz/400KHz	0xAD(Read), 0xAC (Write)	Configurable through resistor	3.3V

16.2 UART

The LPSS Subsystem includes 3 UART ports. The UART ports communicate with serial data port devices compatible with the RS-232 interface protocol. The device map for the LPSS-UART interfaces on WCL are as shown below.

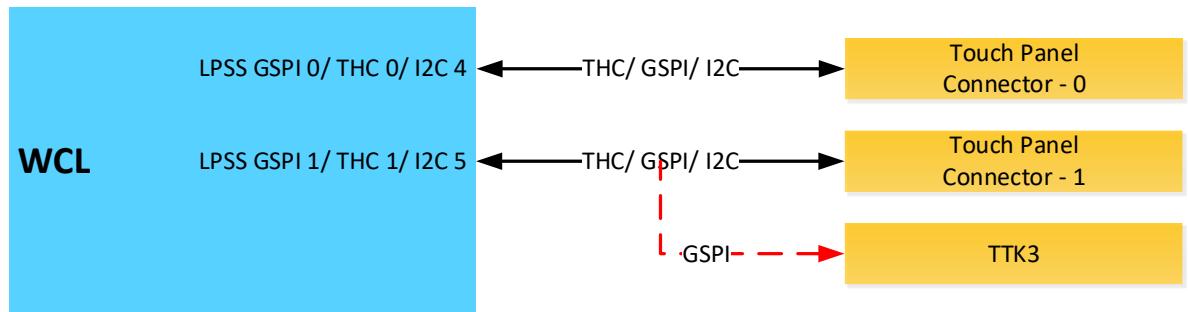
Table 49: UART Device details

Bus	Device Mapping
UART 0	Serial Debug Port /TTK3
UART 1/ ISH UART 1A/ I2C 3	Track PAD/ Audio/PSS/ Power meter/TTK3/EDP
UART 2/ CNVi	M.2 BT module CNVi and non CNVi

**Figure 50: LPSS UART Block Diagram**

16.3 GSPI

The SOC implements 2 GSPI interfaces to support devices that uses serial protocol for transferring data. Each interface consists of a clock (CLK), 2 chip selects (CS) and 2 data lines (MOSI and MISO). The device map for the LPSS-GSPI interfaces on WCL are as shown below.

**Figure 51: LPSS GSPI High level Block Diagram**

17 Integrated Sensor Hub (ISH)

17.1 ISH Sensors

Following sensors are selected for validation on WCL and will be hosted on the MoSAIC Gen 2 card. The details of ISH and MoSAIC Gen 2 card are discussed in subsequent sections.

Note: BOM1 BOM2 Sensors are not finalized for WCL. The 3PE teams need to provide the data.

Table 50: List of Sensors on WCL RVP (Not Final)

Generation	ISH 6.0	
Platforms	BOM1	BOM2
3-axis Accelerometer	<i>Bosch BMI323</i>	STMicro LSM6DSV16
3-axis Magnetometer	Memsic MMC5603NJ	AKM AK9919C
3-axis Gyroscope	<i>Bosch BMI323</i>	STMicro LSM6DSV16
Barometer/Altimeter		STMicro LPS22DF
ALS	Vishay VCNL4030	ST VD6283
RGB/XYZ		ST VD6283
SAR - Proximity	Semtech SX9331	Semtech SX9331
IR		ST VD6283
UV		
2nd Accelerometer	<i>Bosch BMA422</i>	STMicro LIS2DW12
Humidity		
Shock		ST LSM6DSV32
Temperature		STMicro HTS221
HAL switch	Rohm BU52072GWZ	Rohm BU52072GWZ
Heart rate/Sp02		
ECG		
Human Presence	ST VL53L7	<i>Infineon BGT60TR13C</i>
User temperature		

Note:

- Samtec Cable: HQCD-030-12.00-TBL-SBR-1
- Extender Cable: 10-pin 2x5 Socket-Socket 1.27mm IDC (SWD) Cable (<https://www.adafruit.com/product/1675>)
- **Blue** indicates changes from ADL MoSAIC Kits
- * Supported by 3rd party vendor.

17.2

Integrated Sensor Hub

The Integrated Sensor Hub (ISH) is a Soft IP that serves primarily as the connection point for the sensors on a platform. ISH is designed for the “Always-On, Always-Sensing” goal. WCL supports Integrated Sensor Hub (ISH 6.0). It contains the following interface to the sensors namely: I2C, I3C, SPI, UART, GPIO. It provides the following functions to support this goal.

- Acquisition / sampling of sensor data in all platform states including Sx and S0.
- Ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS/Applications.
- Low power operation through clock and power gating of the ISH blocks, including SRAMs, together with the ability to manage the power state of the external sensors.
- The ability to operate independently when the host platform is in a low power state.
- Compatibility with various operating systems,
- Ability to provide sensor-related data to other subsystems within the SOC, such as the CSME, Camera subsystem, Audio subsystem, etc.

ISH contains the following interface to the sensors namely: I2C, I3C, SPI, UART, GPIO.

- **ISH I2C:** ISH contains up to 3 I2C Ports capable of High-Speed Mode up to 1 Mbps.
- **ISH I3C:** ISH contains up to 2 I3C Port with HDR/DDR up to 24Mbps.
- **ISH SPI:** ISH contains 2 SPI port supporting speed up to 25 Mbps.
- **ISH UART:** ISH supports 2 UART ports capable of supporting operating speeds up to 4 Mbps.
- **ISH GPIOs:** ISH GPIOs are typically used for enabling the power to the sensor, detecting the interrupts from sensors etc. External pull ups will be provided for ISH GPIOs.

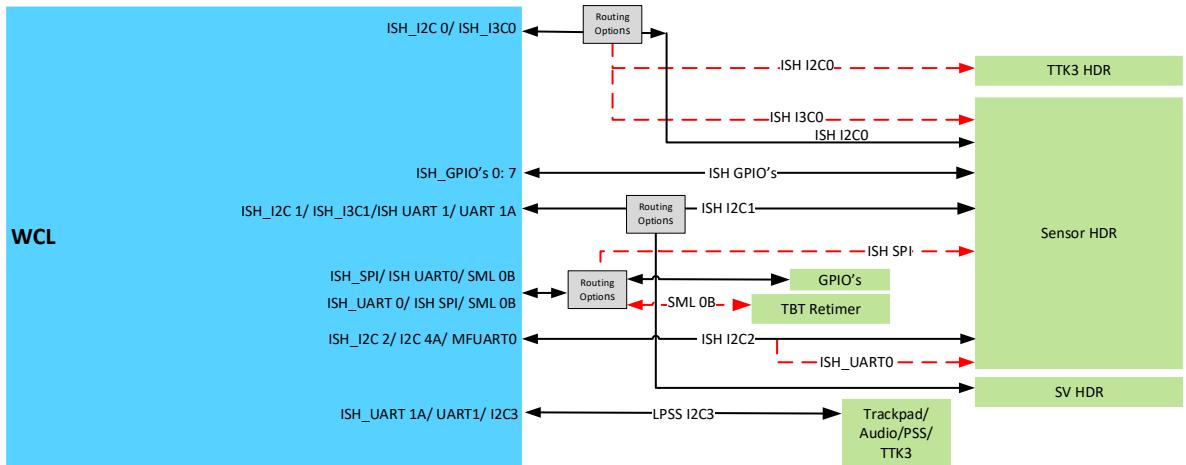


Figure 52: ISH Sensor Header high level block diagram

17.2.1 ISH I2C/I3C

The ISH supports three I2C controllers capable of operating at speeds up to 1 Mbps each. The I2C controllers are completely independent of each other: they do not share any pins, memory or interrupts.

The ISH's I2C host controllers also share the same general I2C port specifications:

- Master Mode Only (all peripherals must be slave devices)
- Support for the following operating speeds:
 - Standard mode: 100kbps
 - Fast Mode: 400kbps
 - Fast Mode Plus: 1Mbps
- Support 7-bit addressing formats on the I2C bus
- FIFO of 64 bytes with programmable watermarks/thresholds

ISH I3C signal is muxed with ISH I2C.

Table 51: ISH I2C device mapping

Bus	Device Mapping
ISH_I2C 0/ ISH_I3C0	Sensor HDR as ISH I2C 0/ I3C 0
ISH_I2C 1/ISH_I3C1/ ISH UART 1/ UART 1A	Sensor HDR as ISH I2C 1 / SV HDR as ISH I2C1
ISH_I2C 2/ I2C 4A/ MFUART0	SNSR HDR as ISH I2C2

17.2.2 ISH UART

ISH supports 2 UART ports capable of supporting operating speeds up to 4 Mbps. ISH UARTs is used to generally connect the sensors related to GNSS (Global Navigation Satellite Systems) Ex: GPS. All the signals are routed to the sensor header.

Table 52: ISH UART device mapping

Bus	Device Mapping
ISH_UART 0/ ISH SPI/ SML 0B	Sensor HDR/MECC as ISH UART0/ Re-timer as SML0B
ISH_UART 1/ ISH I2C 1/ UART 1A	Sensor HDR as ISH I2C1/SV HDR as ISH I2C1
ISH_UART 1A/ UART1/ I2C3	Track PAD/ Audio/ PSS/ TTK3/ MECC AIC as I2C3

17.2.3 ISH SPI

The ISH supports one SPI controller comprises of four-wired interface connecting the ISH to external sensor devices and port is routed to sensor header.

The SPI controller includes:

- Master Mode Only
- Single Chip Select
- Half Duplex Operation only
- Programmable SPI clock frequency range with maximum rate of 24 Mbps
- FIFO of 64 bytes with programmable threshold.

Table 53: ISH SPI device mapping

Bus	Device Mapping
ISH_SPI/ ISH UART0/ SML 0B	Sensor HDR as ISH SPI / GPIO's

17.2.4 ISH GPIOs

ISH GPIO's are typically used for enabling the power to the sensor, detecting the interrupts from sensors etc. External pull ups will be provided for ISH GPIOs. Up to 11 dedicated GPIOs can be used from ISH.

17.2.5 ISH Header

WCL will use the MoSAIC Gen2 board. Modular Sensor Add-In-Card (MoSAIC) Gen 2 is an add-in card to enabling connecting different sensors to sensor-enabled platforms. Its main purpose is to connect sensors to ISH (Integrated Sensor Hub aka ISS, Intel Sensors Solution), but it can be used with other sensor solutions as well. MoSAIC Gen2 is a carrier card which means that no sensors are installed on MoSAIC itself. Instead, the MoSAIC Gen 2 card provides 15 DIP sockets, into each a 1-sensor card with one or more sensors can be plugged. Several switches soldered on the MoSAIC Gen2 board are used to route the sensor signals (I2C/SPI/UART/GPIO) to relevant platform (ISH) pins.

Table 54: ISH Header Connector Pinout

Pin name	Pin No	Pin No	Pin name
V3.3A_1.8A_SNSR_HDR	1	2	V3.3A_SNSR_HDR
V3.3A_1.8A_SNSR_HDR	3	4	V3.3A_SNSR_HDR
GND	5	6	V3.3A_SNSR_HDR
GSPI2_CS1_N_SNSR_HDR	7	8	GND
ISH_GP_7_SNSR_HDR	9	10	ISH_I2C1_SDA_SNSR_HDR
NC	11	12	ISH_I2C1_SCL_SNSR_HDR
GND	13	14	GND
NC	15	16	ISH_GP_1_SNSR_HDR
NC	17	18	ISH_GP_0_SNSR_HDR
GND	19	20	ISH_GP_6_SNSR_HDR
ISH_GP_3_SNSR_HDR	21	22	NC
ISH_I2C2_SCL_SNSR_HDR	23	24	NC
ISH_I2C2_SDA_SNSR_HDR	25	26	GND
GND	27	28	GND
GND	29	30	GND
NC	31	32	NC
NC	33	34	SAR_NIRQ_R
NC	35	36	ISH_GP_5_SNSR_HDR
V3.3A_WWAN_SAR	37	38	ISH_SPI_CS_N_SNSR_HDR
GND	39	40	NC
ISH_SPI_MOSI	41	42	ISH_GP_4_SNSR_HDR
ISH_SPI_MISO	43	44	ISH_SPI_CLK_SNSR_HDR
GND	45	46	HDD_PROT
NC	47	48	NC
GND	49	50	NC
NC	51	52	NC
NC	53	54	ISH_UART0 RTS_N
ISH_I2CO_SCL_SNSR_HDR	55	56	ISH_UART0 CTS_N
ISH_I2CO_SDA_SNSR_HDR	57	58	ISH_UART0 TXD
ISH_GP_2_SNSR_HDR	59	60	ISH_UART0 RXD

18 *Touchscreen & Touchpad*

18.1 Touchscreen

WCL RVP will support 2 touch panels (1 per port) to support two 1x20 Headers on board that are not backward compatible to ADL RVP. These panel will support dual screen in as you can connect two screens to one RVP and have touch and pen work for both panels.

WCL RVP shall support 1 I2C based touch screen by default (Touch Panel Connector - 1) and 1 THC-SPI based touch screen by default (Touch Panel Connector - 2). The configuration above is the desire BKC Default, which shall be configured in BIOS. Starting in MTL/ARL, there will be an internal Muxing of the PCH to switch between I2C/GSPI/THC on the HID Port. Therefore, the ability to switch these ports shall be supported in BIOS and configuration can be changed by user preference.

NOTE: Maximum on-board THC-SPI trace length < 8"

The default power gating option is not provided for the POR touch panel as idle power requirement is on the low.

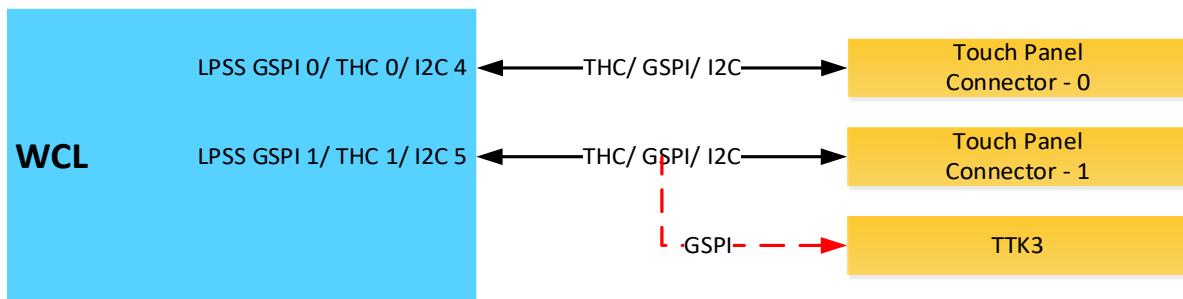


Figure 53 : Touch Panel high level block diagram

18.1.1 Touchscreen SPI / I2C header

The Pinout Details for the Touchscreen Header are provided below. Touch panel connector is different from ADL-P RVP Touch Panel connector.

Table 55: Touch Screen Header Pin-Out Details

Pin No	Functionality	Pin Description
1	THC SPI IO0	SPI MOSI
2	I2C SCL	I2C based touch panel - I2C clock
3	THC SPI IO1	SPI MISO
4	I2C SDA	I2C based touch panel - I2C data
5	THC SPI INT_N/I2C INT	Interrupt
6	THC SPI RST_N/I2C RST	Reset

7	GND	
8	THC SPI CLK	
9	THC SPI CS	
10	THC SPI IO2	
11	THC SPI IO3	
12	THC VDD PWR EN GPIO in	Loop back for RVP usage. Other usage is VISA
13	THC VDD PWR EN GPIO out	
14	VDD_3.3V	VDD - Power input to Touch controller
15	GND	
16	VDDSPI_1.8V	VDDSPI - SPI Power input to Touch Controller
17	Touch Pause Scan	
18	RESERVE	
19	I2C SPI MODE SEL	
20	HOOK[0] (CLTAP_PWRGOOD)	RSMRSTB

Note: Touch panel power header (1x4) will be removed from the RVP. This is because, 1.8V pins are allocated in the touch panel connector itself. So, switching between 3.3V and 1.8V power is no longer required.

18.1.2 Touchscreen Interrupt & Reset Mapping

For POR the default interface is 1.8V SPI interface and following signals from SOC/PCH are used as reset and interrupt.

Table 56: Pin map for Reset & Interrupt for Integrated Touch Panel

PCH GPIO	Function	Description	Voltage
TCH_PNL_RESET	Reset	HIGH: Out of Reset LOW: In Reset	PCH I/O voltage (No board level shifting)
TCH_PNL_INT	Interrupt	HIGH: No interrupt LOW: Interrupt	PCH I/O voltage (No board level shifting)

18.2

TouchPad

WCL RVP provides a 1x12 pin header to interface the THAT based click pad. The Touchpad is interfaced to LPSS I2C-1 at 3.3V through the level shifter on board.

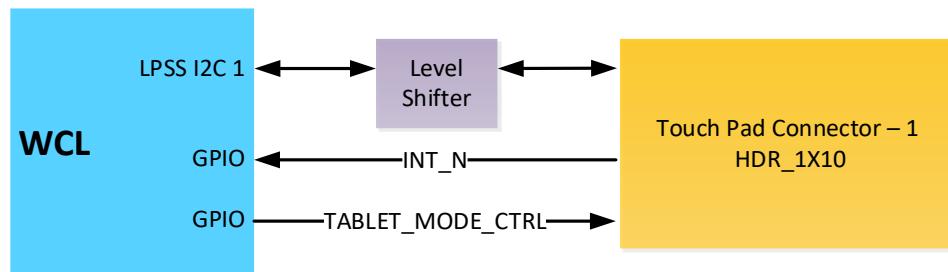


Figure 54: Touchpad high level block diagram

18.2.1

Touchpad I2C Header

Table 57: 1x12 Header Pinout for Touchpad Interface

Pin No	Signal Name
1	+3.3V
2	+3.3V
3	+1.8V
4	I2C_SDA
5	TABLET_MODE_CTRL
6	I2C_SCL
7	GND
8	+5V
9	+5V
10	GND
11	GND
12	INT_N

Note : The 5V will be removed from Touchpad connector. This is no longer used in latest touch pad. So pin 8 and 9 will NC in WCL

19 Security

Trusted Platform Module (TPM) is a Trusted Computing Group (TCG) low cost security solution to increase confidence on system security. The TPM is a device that resides on the motherboard and is connected to SOC/PCH using Serial Peripheral Interface (SPI) bus to communicate with the rest of the platform.

The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPM's are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a TPM provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions, and communication more trustworthy.

The WCL RVP supports only SPI based TPM AIC. It doesn't support eSPI based TPM as no such device exists. LPC based TPM as LPC interface is no longer supported.

19.1 SPI based TPM

The WCL RVP supports the discrete SPI TPM AIC over the primary SPIO interface that connects the SOC/PCH and the BIOS flash memory.

The SPI based TPM AIC should be plugged into the traditional 20pin BIOS flash header. The IPN of the 2x10 header is G25403-002 with pin definition given in below table.

Table 58: Pinout Details for SPI based TPM

Signal Name	Pin No	Pin No	Signal Name
KEYING	1	2	CHIP_SELECT_0
RSMRST	3	4	CHIP_SELECT_1
GND	5	6	+3.3A OR +1.8A
SPI_CLK	7	8	DQ2
DQ3	9	10	SPI_MISO
HOLD	11	12	SPI_MOSI
CHIP_SELECT_2	13	14	GND
WRITE_PROTECT	15	16	TP_SERIAL_IRQ
SPI TPM INT_N	17	18	+3.3A OR +1.8A
PLTRST	19	20	RSVD

SPI TPM AIC hosts the SLB9670Tx chip from Infineon. It supports an SPI interface with a transfer rate of up to 43MHz. Its power management is handled internally; no explicit power-down or standby mode is required. The device automatically enters a low-power state after each successful command/response transaction. If a transaction is started on the SPI bus from the host platform, the device will wake immediately and will return to the low-power mode after the transaction has been finished.

20 PSS

PSS is Processor Secured Storage interface that is primarily intended for tracking the platform specific information in a factory like environment. The PSS interface enables platform specific information to be stored on the On-board memory (EEPROM) and access the stored information by either I2C or RFID reader. The information can be uploaded to a Central Database which will then be accessible by internal labs for the purpose of tracking and proactively reviewing current hardware and software status. Information like reworks implemented on the specific platform can be stored in the PSS EEPROM chip.

PSS interface design is a standard implementation on all Intel RVP boards and WCL RVP shall follow the same circuit and design as its predecessors.

The PSS chip should be able to be read by an external reader at a distance greater than 1 meter from the Platform that contains the PSS chip in an open environment.

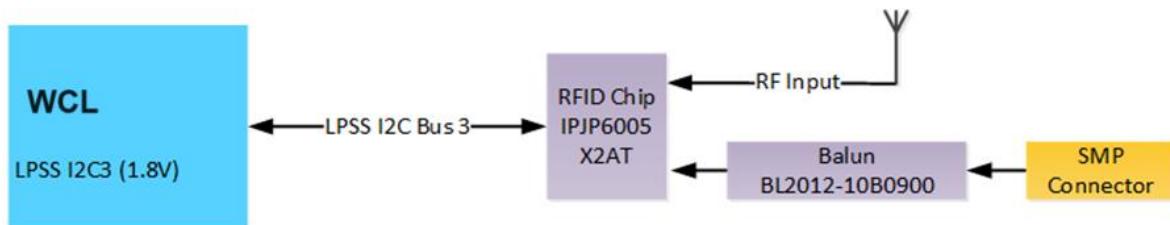


Figure 55: PSS Circuit high level block diagram

The WCL RVP supports 8K memory size RFID chip with options for I2C connection from SOC.

The RVP supports both on board PCB Dipole antenna as well as the external Antenna options. The external antenna path will have the on board BL2012 series Balun chip from ACX. The PSS shall have the properties mentioned in the table below.

Table 59: PSS Properties on WCL RVP

Description	Value
Memory Size	8kbit
Memory Configuration	12 x 128 NVM / OTP
I2C Interface	Device Driver-OS
Reader Communication	Gen2 RFID Commands
Antenna Bandwidth	900MHz
Antenna Type	Dipole, Monopole

21 ***GPIOs***

The SOC General Purpose Input/output (GPIO) signals are grouped into multiple groups (such as GPP_A, GPP_B, and so on) and are powered by the SOC/PCH Primary well. Many GPIO signals are multiplexed with other native functions.

The high-level features of GPIO:

- **Support 1.8V GPIO only**
- GPIO Serial Expansion (GSX) bus mux on existing GPIO pins
- All GP Input are capable of generating an IRQ interrupt based on software configured level or edge-triggered event.
- All GP Input are capable of generating SCI.
- All GP Input are capable of generating wake event.
- Selective GP Input are capable of generating NMI or SMI#.
- GPIO supports glitch free during power sequencing, and when switching mode of operation (see GPIO spreadsheet for pins with exception).
- Supports software configured GP Input polarity.
- Supports GPIO mode input sensing (Rx) disable.
- Supports GPIO mode internal weak pull configured for pullup, pulldown or none.
- Support RCOMP for all GPIO pins (LP).
- Support Virtual GPIO for internal on-die connection between CNVi and LPSS, ACE, PCIe CLKREQ, and OC Virtual wire support.

Table 60: GPIO Power group mapping

Power Group	Number of Pins	Remarks
GPP_A	16	
GPP_B	26	
GPP_C	24	
GPP_D	26	
GPP_E	21	
GPP_F	23	
GPP_H	21	
GPP_S	8	
GPP_V	18	

The **GPIO allocation yet to be updated.**

All the SOC/PCH GPIO pins will be routed though resistor which will help in debugging.

21.1 RCOMPs

RCOMP's in WCL platform are listed below.

Table 61: RCOMP Resistor Values

Pin Name	Description	Termination
DDI_RCOMP	eDP PHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
SOC_REFRCOMP_ISCLK	Connected to an external precision resistor for XCLK bias voltage generation	180 ohms 1%
TYPEC_RCOMP		200 ohms 1%
PCIE4A_RCOMP	analog connection point for an external bias resistor to ground	200 ohms 1%
PCIE4B_RCOMP	analog connection point for an external bias resistor to ground	200 ohms 1%
USB3_RCOMP	USB3 MPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
USB2A_RCOMP	USB Resistor Bias, analog connection points for an external resistor to ground.	200 ohms 1%
USB2B_RCOMP	USB Resistor Bias, analog connection points for an external resistor to ground.	200 ohms 1%
CNV_RCOMP	WiFi DPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
SNDW_RCOMP	SoundWire buffer RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
UFS_RCOMP	UFS MPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
DDR_RCOMP		100 ohms 1%

22 On board Hardware Straps

The WCL RVP takes care of the default hardware strap configuration for both CPU and PCH to ensure normal functionality. WCL RVP will provide on-board Pull-up/Pull-down resistor stuffing options for each strap. The strap configuration options along with default setting is given in below tables.

22.1 SOC Hardware Straps

SOC straps are mentioned in the table below.

Table 62: PCH Hardware Strap Options

GPIO #	When Sampled	Termination	HVM Strap	Pin Strap Usage	Polarity
xxgpp_b_4	PCH_PWROK	20K PD	No	No Reboot	No reboot if sampled high
xxgpp_b_14	PCH_PWROK	20K PD	No	Top swap override	Top Swap is enabled if sampled high
xxgpp_b_23	RSMRSTB	20K PD	No	"RTC" PLL (POR) or XTAL	Default RTC PLL distribution source 1 = 38.4MHz XTAL (Survivability usage only) 0 = "RTC" PLL @76.8MHz. This is the POR, and the default. *This pin strap is for survivability usage only, and expected to be further qualified with the "Personality Strap" aka "A0 only Strap" outside of GPIO prior to being used by iSclk.
xxgpp_c_2	RSMRSTB	20K PD	No	TLS Confidentiality Enable	TLS conf enabled if sampled high
xxgpp_c_5	RSMRSTB	20K PD	No	eSPI Disabled (previously called "EC-less Platform")	eSPI is disabled if sampled high
xxgpp_c_15	RSMRSTB	20K PD	No	XTAL Input Mode[0]	XTAL input mode 0: XTAL attached - default 1: Single-ended crystal input HVM/BI testing to pull-up this strap to select Single-Ended
xxgpp_d_12	PCH_PWROK	20K PD	No	Flash descriptor security override	Security measures defined in the Flash Descriptor is overriden if sampled high
xxgpp_e_6	RSMRSTB	20K PU	No	JTAG ODT Disable	JTAG ODT is disabled if sampled low
xxgpp_e_9	RSMRSTB	None	Yes	RTCPPLL Pre Divider Enable (HVM use only)	RTCPPLL Pre Divider Enable 0 – Bypass pre-divider (functional; 32.768kHz input) 1 – Enable /125 pre-divider (HVM; 4MHz input) *This strap is qualified by DFXTESTMODE

xxgpp_e_10	RSMRSTB	None	Yes	XTAL Input Frequency *HVM/BI mode only	Single-ended reference clock divider select 0 – Divider Bypass (functional) - default 1 – Divide by 4 (100MHz HVM mode) *This strap is qualified by DFXTESTMODE
xxgpp_f_2	RSMRSTB	20K PU	No	M.2 CNV modes / Integrated CNV Enable/Disable	M.2 CNV modes 0 = Integrated CNV enable 1 = Integrated CNV disable
xxgpp_f_19	RSMRSTB	20K PD	No	Skip RTC Clock Stabilization Delay (IOTG Boot Time Reduction)	Skip RTC Clock Stabilization Delay (IOTG Boot Time Reduction) 0 = No bypass (default) 1= Bypass/Skip 95ms RTC clock stabilization delay
xxgpp_h_0	RSMRSTB	20K PD	No	eSPI Flash Sharing Mode	Master attached flash sharing (MAFS) if sampled low, else slave attached flash sharing (SAFS)
xxgpp_h_1	RSMRSTB	20K PD	No	Enable/Disable SPI Flash Descriptor Recovery	Flash Descriptor Recovery for NIST SP800-193 0 - Flash descriptor recovery disable - default 1 - Flash descriptor recovery enable
xxgpp_h_2	RSMRSTB	20K PD	No	SPI Flash Descriptor Recovery Source - Internal/External	Flash Descriptor Recovery Source for NIST SP800-193 0 - Flash descriptor recovery internal source - default 1 - Flash descriptor recovery external source
xxspi0_io_2	RSMRSTB	20K PU	No	Consent Strap	Consent strap is enabled if sampled low
xxspi0_io_3	RSMRSTB	20K PU	No	Personality Strap (A0 only, disabled by RevID)	Personality strap is enabled if sampled low
xxdbg_pmode	RSMRSTB	20K PU	No	DFXTESTMODE active	Assert DFXTESTMODE to enable other straps to take effect if sampled low

22.2

CPU Hardware Straps

No NOA signals from WCL SOC.

23 Debug and Validation Hooks

A system could be debugged either via one of below methods:

- Open Chassis debug – this includes XDP, MIPI60 (LTB) with only one MIPI60 header on WCL RVP
- Closed chassis debug – USB debug (USB2/USB3/OOB/I3C)

This section of RVP HAS shall cover the overview of SoC debug architecture followed by debug interfaces of SoC that are supported in the RVP. It shall also list down various SoC validation hooks and cover all the validation interfaces that are supported in this WCL RVP for users to debug the Silicon.

23.1 SoC Debug architecture - Introduction

WCL SoC Architecture overview here.

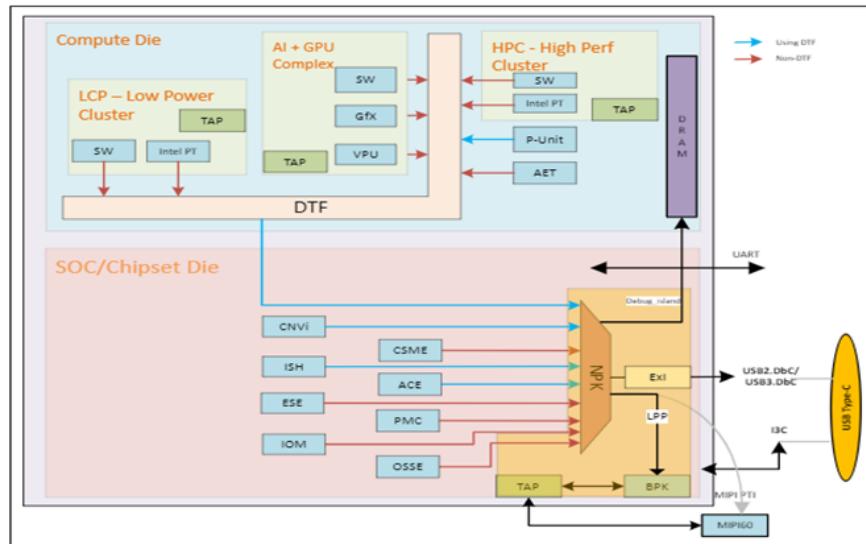


Figure 56: WCL Architectural overview

WCL has one High performance CPU, an Atom core cluster for efficient computing and an AI-GPU complex on the compute die. The VPU has been moved to the AI & GPU cluster.

The SoC/Chipset Die consists of NorthPeak (NPK) debug island and supports multiple debug interfaces like the USB/MIPI60/JTAG etc.

Debug Trace Fabric (DTF) is considered default bus to carry traces to NorthPeak (NPK). However, not all the trace sources support writing to DTF and their connection to NPK is shown in different colors.

23.2

Debug interfaces supported by SoC

Table 63 : SOC VISA MIPI60 Connector

Type	Interface Name	Supported in WCL RVP
Open Chassis	JTAG (over MIPI60)	Yes
	MIPI-PTI (over MIPI60)	Yes
Closed Chassis	USB2 DbC (over Type C)	Yes
	USB2 DbC (over USB2 port)	Yes
	OOB 2 wire (over Type C)	No
	I3C Debug (over Type C)	Yes
	USB3 DbC (over Type C/Std-A)	Yes (Type-A & Type-C)

23.2.1 SMP Mapping of Validation Hooks

Validation signals on single SMP connector List:

Only one signal at a time can be connected to SMP connector after resistor stuffing rework.

Table 64 : Validation Hooks on SMP

SMP - 1	SMP - 2
TBD	OBS0MON_ISCLK
JTAG_PCD_MBPB_2	GCD_VIEW_DIG_OUT_1
VIEWPWR_1	
SMP - 3	SMP - 4
TBD	OBS1MON_ISCLK
VIEWPWR_0	GCD_HVM_CLK
GCD_VIEW_DIG_OUT_2	USB2_ID
SMP - 5	SMP - 6
XTAL_IN	DDR_VIEW[0]
XTAL_OUT	JTAG_PCD_MBPB_0
SMP - 7	SMP - 8
DDR_VIEW[1]	DDR_ANA_VIEW
JTAG_PCD_MBPB_1	DLVR_PDMONO
	HVMBCLK
SMP - 9	SMP - 10
GCD_VIEW_DIG_OUT_0	VTARGET_0

JTAG_PCD_MBPB_3	VIEWCLK_1
DLVR_PDMON1	
SMP - 11	-
VIEWCLK_0	-
VTARGET_1	

23.3 Generic RVP debug features

23.3.1 Open Chassis Debug

Debug used for interfaces that are not placed inside a closed system is referred to as Open Chassis Debug.

Types of Open Chassis:

- MIPI PTI
- JTAG

The MIPI PTI & JTAG signals are over the MIPI 60 Connector.



Figure 57: MIPI60 Debug Port (Samtec QSH-030-01 series)

The MIPI 60 Debug Port Interface enables communication between the Target System and Debug Tools. The MIPI 60 connector has power pins, JTAG, UART, I2C clock & data signals and different active low signals like POWER_BUTTON_N, CPU_EARLY_BREAK_N, PLATFORM_BOOT_STALL_N, Single RESET_N, RESET_BUTTON_N to initiate a target system cold boot, to stall the CPU boot sequence at the earliest CPU stall point to perform pre-boot configurations to Intel CPU's, to stall the platform boot sequence at the earliest stall point to perform pre-boot configurations to Intel PCH's and SoC's, to determine various Reset and Power states on the Target System, to initiate a Target System warm-reset without cycling power cycles respectively.

23.3.1.1 MIPI60 Debug Connector

WCL supports 4 channel VISA debug capability. Channel 3 & 4 VISA signals will be routed to MIPI 60 connector. Whereas Channel 1 & 2 VISA signals are muxed with Touch signals & will be routed to new Touch connector.

WCL RVP will support a single MIPI 60 connector for debug. WCL does not have NOA signals.

The WCL RVPs will have support for MIPI 60 debug port with optional SOC/PCH –VISA only signals routed to a MIPI 60 connector & Touch connector.

Note- SOC/PCH JTAG will be routed to MIPI-60 Debug connector.

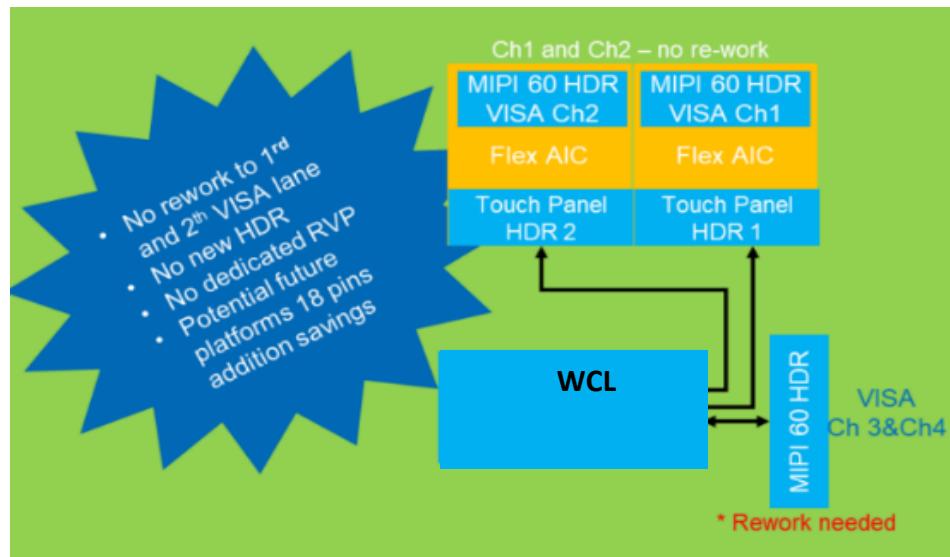


Figure 58: MIPI60 Debug Connector

Table 65: SoC VISA MIPI60 Connector Pinout

PIN	Intel MIPI60 Signal Name	Target System Signal Name	Device	PIN	Intel MIPI60 Signal Name	Target System Signal Name	Device
1	VREF_DEBUG	No Connect	NA	2	TMS	No Connect	NA
3	TCK0	No Connect	NA	4	TDO	No Connect	NA
5	TDI	No Connect	NA	6	HOOK[7]/nReset	No Connect	NA
7	Hook[6]	No Connect	NA	8	TRST_PD	10KΩ to GND	NA
9	TRST_N	No Connect	NA	10	PREQ_N	No Connect	NA
11	PRDY_N	No Connect	NA	12	VREF_TRACE	VREF_TRACE	System
13	PTI_0_CLK	PTI/VISA_0_CLK	CPU	14	PTI_1_CLK	GND	NA
15	POD_PRESENT1_N	GND	GND	16	GND	GND	NA
17	POD_PRESENT2_N	GND	GND	18	PTI_1_DATA[0]	No Connect	NA
19	PTI_0_DATA[0]	PTI/VISA0_DATA[0]	PCH	20	PTI_1_DATA[1]	No Connect	NA

21	PTI_0_DATA[1]	PTI/VISA0_DATA[1]	PCH	22	PTI_1_DATA[2]	No Connect	NA
23	PTI_0_DATA[2]	PTI/VISA0_DATA[2]	PCH	24	PTI_1_DATA[3]	No Connect	NA
25	PTI_0_DATA[3]	PTI/VISA0_DATA[3]	PCH	26	PTI_1_DATA[4]/ PTI_2_DATA[0]	No Connect	NA
27	PTI_0_DATA[4]	PTI/VISA0_DATA[4]	PCH	28	PTI_1_DATA[5]/ PTI_2_DATA[1]	No Connect	NA
29	PTI_0_DATA[5]	PTI/VISA0_DATA[5]	PCH	30	PTI_1_DATA[6]/ PTI_2_DATA[2]	No Connect	NA
31	PTI_0_DATA[6]	PTI/VISA0_DATA[6]	PCH	32	PTI_1_DATA[7]/ PTI_2_DATA[3]	No Connect	NA
33	PTI_0_DATA[7]	PTI/VISA0_DATA[7]	PCH	34	RSVD1	No Connect	NA
35	PTI_0_DATA[8]/ PTI_3_DATA[0]	PTIO_DATA[8]/ PTI/VISA1_DATA[0]	PCH	36	HOOK[3]	No Connect	NA
37	PTI_0_DATA[9]/ PTI_3_DATA[1]	PTIO_DATA[9]/ PTI/VISA1_DATA[1]	PCH	38	HOOK[2]	No Connect	NA
39	PTI_0_DATA[10]/ PTI_3_DATA[2]	PTIO_DATA[10]/ PTI/VISA1_DATA[2]	PCH	40	HOOK[1]	No Connect	NA
41	PTI_0_DATA[11]/ PTI_3_DATA[3]	PTIO_DATA[11]/ PTI/VISA1_DATA[3]	PCH	42	HOOK[0]	VREF_TRACE_PWRGOOD	System
43	PTI_0_DATA[12]/ PTI_3_DATA[4]	PTIO_DATA[12]/ PTI/VISA1_DATA[4]	PCH	44	RSVD2	No Connect	NA
45	PTI_0_DATA[13]/ PTI_3_DATA[5]	PTIO_DATA[13]/ PTI/VISA1_DATA[5]	PCH	46	RSVD3	No Connect	NA
47	PTI_0_DATA[14]/ PTI_3_DATA[6]	PTIO_DATA[14]/ PTI/VISA1_DATA[6]	PCH	48	I2C_SCL	No Connect	NA
49	PTI_0_DATA[15]/ PTI_3_DATA[7]	PTIO_DATA[15]/ PTI/VISA1_DATA[7]	PCH	50	I2C_SDA	No Connect	NA
51	TCK1	No Connect	NA	52	RSVD4	No Connect	NA
53	HOOK[9]	No Connect	NA	54	DBG_UART_TX	No Connect	NA
55	HOOK[8]	No Connect	NA	56	DBG_UART_RX	No Connect	NA
57	GND	GND	NA	58	GND	GND	NA
59	PTI_3_CLK	PTI_VISA1_CLK	PCH	60	PTI_2_CLK	GND	NA

23.3.2 Closed Chassis Debug

Debug using functional connections available in the complete, closed, form-factor system is referred to as Closed Chassis Debug.

Types of Closed Chassis:

- Debug over USB 2.0
- Debug over USB 3.0
- Intel 2W DCI
- Debug for I3C

23.3.2.1 Debug over USB 2.0

The Debug Class over USB 2.0 is supported on all USB 2.0 ports and uses the native USB protocol to transmit. USB2.0 debug class does require the use of the TS functional xHCI controller.

USB2 DBC Port 1 has enhanced capabilities beyond other USB2 ports and should be connected to an easily accessible USB Type-C port so these new features can be utilized. These features are enabled because USB2 DBC Port 1 is in “Debug Island”. The features include:

- Able to connect very early in the boot sequence to support Connect First/Authorized Debug unlocks.

- Able to remain connected and active during low power events (Sx and S0iX).

- Connection does not affect device going to low power.

- Since the Intel Trace Hub is also instantiated in Debug Island, traces can seamlessly transition over power cycling events.

- Supports all other traditional connection and debug capability.

For the Debug Class over USB 2.0 to operate, the TS must have debug enabled and the TS USB port used must be in the UFP role. The Type C is configured to UFP role when the PD controller detects Debug Accessory Mode. DTS is in the DFP role and TS is in the UFP role. The Std-A port must have the USB2 port manually configured to the UFP role in the FW straps using the mFIT tool and can't be used as functional port when it's configured for debug.

23.3.2.2 Debug over USB 3.0

The Debug Class over USB 3 is supported on all of the USB 3 ports from the PCH and CPU and uses the native USB protocol to transmit. USB 3 Debug Class does require the use of the functional controller. The Debug Class over USB 3 works over both Type A and Type C. However, DFx is not supported on USB3 connection to the CPU. Only USB3.1 connection to the SOC supports DFx.

The Debug Class over USB 3 is only available during the S0 power state. Debug Class over USB 3.1 is first available after the platform reset de-assertion and when the CPU is running. The Debug Class over USB 3 does not survive through Sx power state transitions and across warm and cold resets. When the Debug Class over USB 3.1 is connected, the system will not be able to exit the S0 power state into lower states.

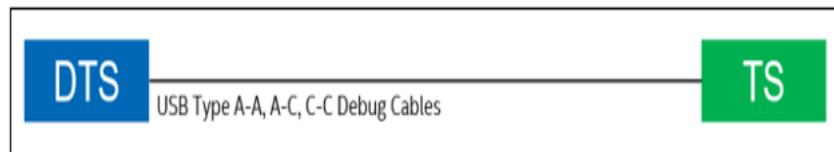


Figure 59: Illustrates the most basic connection between DTS and TS using just a USB Debug cable

23.3.2.3 Intel 2W DCI

Intel® DCI 2W DCI OOB uses the CCA adaptor combined with the “2W DCI OOB UART Adaptor” to convert USB signaling from the DTS to UART signaling to the TS. The Intel® 2W DCI OOB port is instantiated in the “Debug Island” power well which enables operation during early boot and through low power state transitions. 2W Intel® DCI OOB functions at low bandwidth, which supports Intel® JTAG Probe Mode like commands, Platform Boot Stall and run control but is too low for typical trace bandwidth. Intel® DCI 2W DCI OOB is a mature technology which is being replaced by the new platform debug connection called “Debug for I3C.”



Figure 60: 2W DCI OOB Connection

Figure 60 illustrates the connection between the DTS and TS using 2W DCI.OOB. The DTS connects with the CCA device which converts the USB transport signaling into proprietary OOB (out of band) signaling. The CCA device passes these proprietary signals through the 2W DCI.OOB UART Adaptor which level shifts them and multiplexes them onto the SBU pins for presenting to the Target System.

23.3.2.4 Debug for I3C

I3C is a new open standard protocol being used for inter-device communication. It extends traditional I2C by adding multi-mastering, higher speeds, and security protections. The MIPI I3C Debug Standard allows the I3C transport to send debug commands and have them intercepted and used to drive debug functionality. The primary use case is using a single I3C bus to interconnect all platform components to this debug transport. This allows a single connection to debug Intel’s SOC, Intel’s Discrete Graphic solution, and other compatible third-party devices. Since the MIPI I3C Debug Standard is public and scalable, third-party tool and device providers can freely use it to support platform debug.

A big advantage of using “Debug for I3C” is Hot Connect. The “Debug for I3C” port can reliably connect upon fail and extract some triage information. If **DAM** is preset, then the system can be unlocked by Intel and more extensive debug performed.

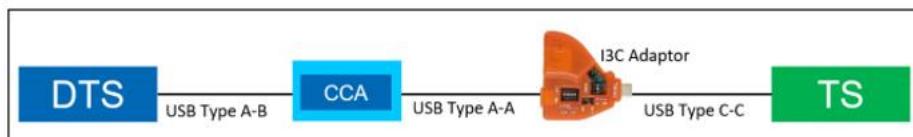


Figure 61: “Debug for I3C” Connection

Figure 61 illustrates the connection between the DTS and TS using the “Debug for I3C” transport. The DTS connects with the CCA device which converts the USB transport signaling into proprietary OOB (out of band) signaling. The CCA device passes these proprietary signals through the I3C Adaptor which converts them and multiplexes them onto the SBU pins for presenting to the Target System.

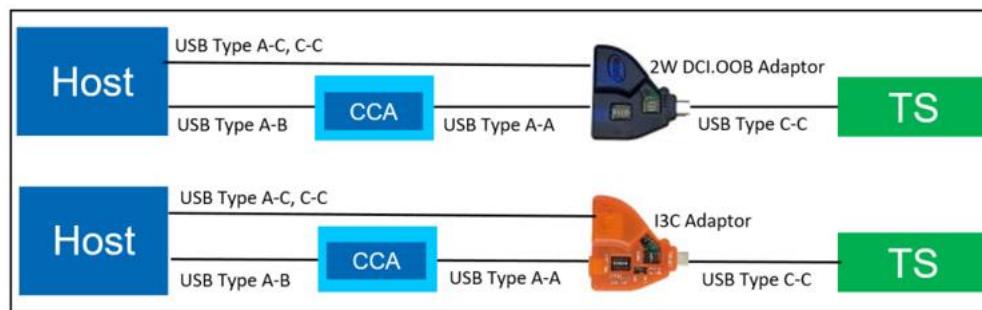


Figure 62: Extending 2W DCI.OOB and Debug for I3C with USB DbC

It is possible to multiplex USB3 DBC and USB2 DBC transports with either the 2W DCI.OOB or the “Debug for I3C” debug connections by routing a second USB port through the convertor. Figure 62 illustrates adding the additional connection. Caution, the TS USB port is set to Debug Accessory Mode, so the USB2 port is changed to an Upper Facing Port (UFP).

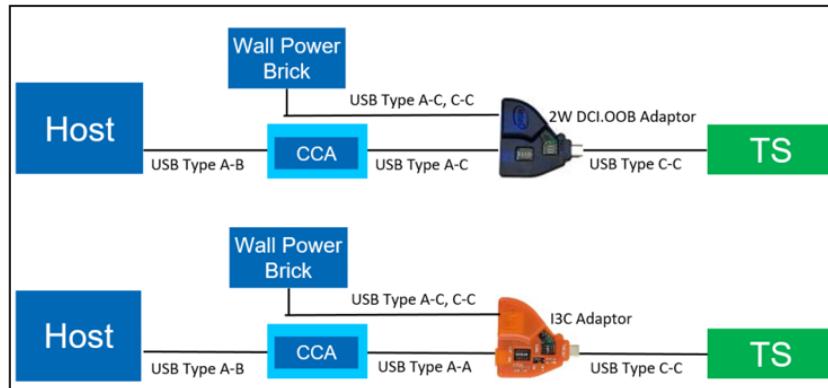


Figure 63: Charging the TS while Debugging using 2W DCI OOB or Debug for I3C

It is possible to power the USB port used for debug by plugging in a USB charging brick to the second port of the adaptors. Figure 63 shows some possible configurations.

23.3.3 Miscellaneous Debug headers in RVP

23.3.3.1 SINAII2/NEVO

SINAII2 is used for voltage & current sensing, current pump channels and GPIO manipulations. SINAII (believed to be the name of mountain where the Ten Commandments were given to Moses by God) is just an internal project name and does not have an acronym. The primary platform interface for SINAII2 is a 2x50, 100pin connector (IPN: D10221-001) for voltage margining and current sensing.

Sinai2 connectors has following types of pins:

1. GPIO: General purpose IOs. Can be configured as input or output and be configured as Open drain or CMOS.
2. GPIO-Fixed: IOs which should be routed to specific signals on the platform or stayed unconnected (if the feature is not needed). These have special topology which matches the relevant functionality.
3. DC3V3IO: General purpose IOs. Can be used to drive 3.3V signals. Good for stable signals (DC) like mux controls & straps. Currently only work as outputs.
4. ISNS [P/N]: Differential pair for sensing current through shunt resistors. Supports up to 160mV.
5. VSNS [P/N]: Differential pair for sensing voltage. Supports up to 3.2V in normal mode and 6.4V in extended mode.
6. IDRIV: Current pumps output for voltage margining. Can drive/sink up to 14mA.
7. SPCL: Special purpose pins, which are used for power/GND or other maintenance functions in Sinai2. They must be connected as stated in the pin map.

SINAI2 special pins:

1. GND – should be connected to reference GND of the platform.
2. VCCST – should be connected to VCCST plane (normally 1.05V) for reference of SVID bus)
3. VCCIO – should be connected to VCCIO plane (normally 0.95V) for reference of MBP and all other GPIOs.
4. Setup done (pin 100 in sideband) – indicates that Sinai2 configuration is done and that the GPIOs are in programmed state. A good practice would be to connect this indication to the power sequence of the platform to prevent race between Sinai2 and other devices. Normally this signal is asserted ~900mS before CPU_POWERGOOD (if powered from the same power supply)

The actual utilization of the Vsense, Isense, Idrive & GPIO channels of Sinai2 is platform dependent. The pinout and channel allocation of SINAI2 interface will be finalized after reviewing the requirements from VFT representative. Multiple options would be supported using optional resistors. Resistor based stuff/unstuff option must be included in any GPIO and Isense path to Nevo connector.

23.3.3.1.1 Current Sensing Signals

Sinai2 senses current for measurement through the Sideband connector. Like in voltage sensing, the accuracy required from Sinai2 is very high. Moreover, in current sensing, Sinai2 is actually sensing low voltage levels (0-160mV) on a shunt resistor and errors and bWCLy routed traces will result in wrong current reading. Max bus voltage is 3.2V (common mode voltage). P/N traces to be taken from phase sense resistor (P/N) similar to PnP HDR routing.

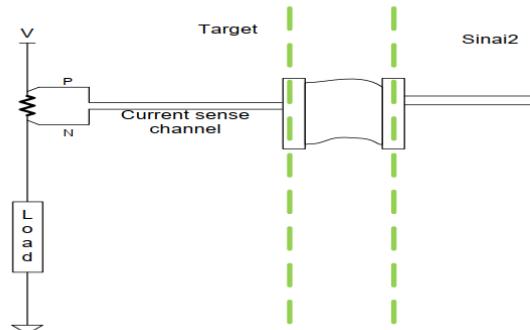


Figure 64: Current Sense Implementation

23.3.3.1.2 Sense resistor selection

It is important to note that the sense resistor selected for this circuitry should enable Sinai2 to measure the entire (or the desired) range of current to the load. For that, the voltage on that resistor in maximum current condition should not exceed 160mV. For example, if the maximum current expected from a plane is 15A, then a good practice would be to select a 10mΩ sense resistor (Vishay WSK2512-0.010-1%-R86E3 can be used for this purpose). A larger resistor will cause a cutoff in the range of sampling while a smaller resistor will cause degradation of the granularity and accuracy of the sampling.

23.3.3.1.3 Routing Guidelines for Sense Signals

Sinai2 senses voltage rails for measurement through AVMC connector. The accuracy required from Sinai2 sensing is very high (less than 1mV), thus, the routing of the sense traces should get special attention. The Routing of AVMC sense signals will follow below guidelines:

- The Voltage sense traces should be routed as differential pair on the platform from the sensing point to the AVMC connector.
- The traces differential impedance should be 80-100 Ω.
- If the negative trace (the *_N trace) is to be connected to GND, then it should be connected to the GND plane as close as possible to the sensing point (e.g. the CPU) and routed differential with the positive trace (*_P).
- It is preferred that the traces will be routed directly to the connector, but if there is a need to place series resistors on the voltage sense traces, the resistance of these resistors should not be bigger than 100 Ω.
- The traces should be routed in internal layers as far as possible from noisy parts (coils, oscillators, high frequency signals etc.)

23.3.3.1.4 SVID Signals to SINAI

SVID to SINAI2 connections are not part in any RVP SKUs of WCL since no team using SVID VR margining or validation over SINAI2 connector.

Table 66: SINA12 Connector pinout

Pin #	Pin Name (Option1 / Option2)	Type	Pin #	Pin Name (Option1 / Option2)	Type
1	VSENSE_P<0>	VSNSP	51	GPIO3	GPIO
2	VSENSE_P<1>	VSNSP	52	BCLKP	GPIO - FIXED
3	VSENSE_N<0>	VSNSN	53	GND	SPCL
4	VSENSE_N<1>	VSNSN	54	GND	SPCL
5	VSENSE_P<2>	VSNSP	55	ISense5N	ISNSN
6	VSENSE_P<3>	VSNSP	56	VSENSE_P<11> / I2C_Slave_SCL	VSNSP/GPIOFIX ED
7	VSENSE_N<2>	VSNSN	57	ISense5P	ISNSP
8	VSENSE_N<>	VSNSN	58	VSENSE_N<11> / I2C_Slave_SDA	VSNSN/ GPIO - FIXED
9	VSENSE_P<4>	VSNSP	59	ISense6N	ISNSN
10	VSENSE_P<5>	VSNSP	60	VSENSE_P<12>	VSNSP
11	VSENSE_N<4>	VSNSN	61	ISense6P	ISNSP
12	VSENSE_N<5>	VSNSN	62	VSENSE_N<12>	VSNSN
13	GPIO0	GPIO	63	I2C_Master_SCL	GPIO - FIXED
14	GPIO1	GPIO	64	I2C_Master_SDA	GPIO - FIXED
15	GND	SPCL	65	GND	SPCL
16	GND	SPCL	66	GND	SPCL
17	VSENSE_P<6> / SPI-MISO	VSNSP/ GPIO - FIXED	67	ISense7N	ISNSN
18	VSENSE_P<7> / SPI-MOSI	VSNSP/ GPIO - FIXED	68	ISense8N	ISNSN
19	VSENSE_N<6> / SPI-CLK	VSNSN/ GPIO - FIXED	69	ISense7P	ISNSP
20	VSENSE_N<7> / SPI-CS	VSNSN/ GPIO - FIXED	70	ISense8P	ISNSP
21	VSENSE_P<8>	VSNSP	71	GPIO4	GPIO
22	ISense0N	ISNSN	72	GPIO5 / PECL_MUX_CTRL	GPIO - FIXED
23	VSENSE_N<8>	VSNSN	73	CPU_PWRGD	GPIO - FIXED
24	ISense0P	ISNSP	74	PLT_RESETN	GPIO - FIXED
25	VSENSE_P<9>	VSNSP	75	GPIO6	GPIO
26	ISense1N	ISNSN	76	PLT_RESTARTN	GPIO - FIXED
27	VSENSE_N<9>	VSNSN	77	GND	SPCL
28	ISense1P	ISNSP	78	GND	SPCL
29	VSENSE_P<10> / PMSYNC	VSNSP/ GPIO - FIXED	79	ISense9N	ISNSN

30	CPU_SVID_OUT	GPIO - FIXED	80	ISense10N	ISNSN
31	VSENSE_N<10> / PECI_MON	VSNSN/ GPIO - FIXED	81	ISense9P	ISNSP
32	CPU_SVID_CLK	GPIO - FIXED	82	ISense10P	ISNSP
33	GND	SPCL	83	PROCHOT(Drive)	GPIO - FIXED
34	GND	SPCL	84	VSENSE_P<13>	VSNSP
35	CATERR	GPIO - FIXED	85	VSENSE_N<13>	VSNSN
36	CPU_SVID_ALRT	GPIO - FIXED	86	VSENSE_P<14>	VSNSP
37	PROCHOT	GPIO - FIXED	87	VSENSE_N<14>	VSNSN
38	THERMTRIP	GPIO - FIXED	88	GPIO7	GPIO
39	ISense2N	ISNSN	89	VCCST	SPCL
40	VRM_SVID_OUT	GPIO - FIXED	90	VCCST	SPCL
41	ISense2P	ISNSP	91	GPIO8 / IDRIVE9	GPIO/IDRV
42	VRM_SVID_CLK	GPIO - FIXED	92	IDRIVE0	IDRV
43	ISense3N	ISNSN	93	IDRIVE1	IDRV
44	GND	SPCL	94	IDRIVE2	IDRV
45	ISense3P	ISNSP	95	IDRIVE3	IDRV
46	VRM_SVID_ALRT	GPIO - FIXED	96	IDRIVE4	IDRV
47	ISense4N	ISNSN	97	IDRIVE5	IDRV
48	PECI	GPIO - FIXED	98	IDRIVE6	IDRV
49	ISense4P	ISNSP	99	IDRIVE7	IDRV
50	BCLKN	GPIO - FIXED	100	IDRIVE8 / PLT_SETUP_DONE	IDRV/SPCL

23.3.3.2 INTEC Header

InTEC is Integrated Thermal Environment Controller used for PECI and thermal monitoring of CPU and PCH thru the external InTEC AIC. The platforms signals that enable the thermal control and monitoring are thermal DIODE signals and PECI signals from CPU and PCH. The platform connector part details are given in below table. Test points will be provided for PECI, FORCEPR# & THERMTRIP#, and CATERR# signals.

MFG	Mfg. Part Number	IPN
Molex	501190-3027	G94240-001
Molex	501190-3017	G24701-002

Figure 65: INTEC Connector PN

The RVP supports G94240-001 part by default. The design details are given below.

Table 67: Platform Design Recommendations for InTEC signals

pin#	InTEC signal name	RVP Signal Connection	Comments
1	THERMDA0_Sense	VAL_THERMDA0_S	Compute Die Thermal Diode 1
2	THERMDC0_Sense	VAL_THERMDC0_S	
3	THERMDC0_Force	VAL_THERMDC0_F	
4	THERMDA0_Force	VAL_THERMDA0_F	
5	PROCHOT0	PROCHOT_MONO_INTEC_N	PROCHOT Copy (LVTTL)
6	GND	GND	
7	THERMDA1_Sense	VAL_GCD_THERM_DA_S	GCD Die Thermal Diode 2
8	THERMDC1_Sense	VAL_GCD_THERM_DC_S	
9	THERMDC1_Force	VAL_GCD_THERM_DC_F	
10	THERMDA1_Force	VAL_GCD_THERM_DA_F	
11	PROCHOT1_PECI Trigger	NC	
12	GND	GND	
13	THERMDA2_Sense	VAL_SOC_THERM_DA_S	SOC Die Thermal Diode
14	THERMDC2_Sense	VAL_SOC_THERM_DC_S	
15	THERMDC2_Force	VAL_SOC_THERM_DC_F	
16	THERMDA2_Force	VAL_SOC_THERM_DA_F	
17	PROCHOT2	NC	
18	GND	GND	
19	THERMDA3_Sense	VAL_THERMDA1_S	Compute Die Thermal Diode 2
20	THERMDC3_Sense	VAL_THERMDC1_S	
21	THERMDC3_Force	VAL_THERMDC1_F	
22	THERMDA3_Force	VAL_THERMDA1_F	
23	PROCHOT3	NC	
24	GND	GND	
25	PECI0	CPU_PECI	PECI Interface
26	GND	GND	
27	VTTO	+VCCIO_TERM_V1P25_INTEC	
28	PECI0_Mux_Ctrl	*PECI Mux Ctrl	
29	PECI_Copy	**PECI PROBING	
30	GND	GND	

*PECI Mux Ctrl Logic:

- PECI_MUX_CTRL = 0 - InTEC connected to H_PECI (CPU), EC/PCH disconnected from H_PECI (CPU)
- PECI_MUX_CTRL = 1 - InTEC disconnected from H_PECI (CPU), EC/PCH connected to H_PECI (CPU)

**PECI Probing (Copy/Monitor):

- 3.3V copy of PECI signal

- Buffered output, for monitoring only (w/o option to drive from PECL connector side)

23.3.3.2.1 PECL Signal routing options

The default routing of PECL signal from CPU will be to EC and there will be resistor stuffing options to route to SOC/PCH or the 30 pin InTec Connector. The PECL interface to InTEC header will also have option to route to SINAII header but the default option will be to InTEC header while SINAII header path requires a resistor rework on the RVP.

23.3.3.3 PORT80 Display Output

The WCL RVP supports the 4 digit 7-Segment LED display for Port80 debug messages like all other previous generation RVPs. The Port80 LED driver will be SMBus based connected to the Embedded Controller (EC) on-board. The EC gets the port80 messages from PCH over the eSPI interface depending on the platform configuration.

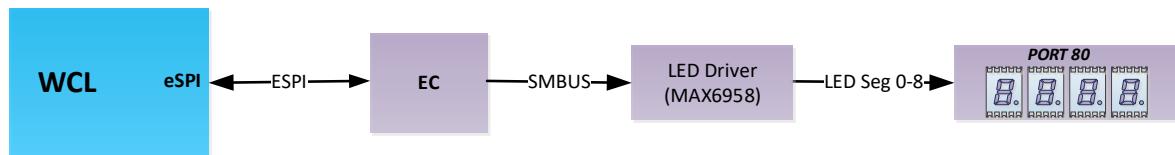


Figure 66: Port80 Functional Diagram

A 2x8 16-pin header 2.54mm pitch provided on the RVP design to bring the Port80 LED signals to front panel for validation purpose.

Table 68: SAS Header and Pinout

MFG	Mfg. Part Number	IPN Number
WIESON TECHNOLOGIES CO., LTD	AC2100-0009-005-HH	K92628-001

Signal Name	Pin #	Pin #	Signal Name
+V3.3A_3.3DSW_VAL	1	2	LED_SEG8
GND	3	4	LED_SEG7
NO PIN	5	6	LED_SEG6
NC	7	8	LED_SEG5
NC	9	10	LED_SEG4
NC	11	12	LED_SEG3
RSVD_LED_SEG9	13	14	LED_SEG2
LED_SEG0	15	16	LED_SEG1

23.3.3.4 Serial Debug Console

The WCL RVP supports Serial debug console over a micro-AB USB 2.0 receptacle port. The RVP uses CP2105 Dual USB UART / FIFO IC for UART to USB2.0 conversion. The RVP will have option for EC and

SOC/PCH connectivity for TX and RX signals while the CTS and RTS signals would be available from the SOC/PCH.

Debug UART signals from EC shall be connected to mECC AIC connector and TTK3 connector as option in the design.

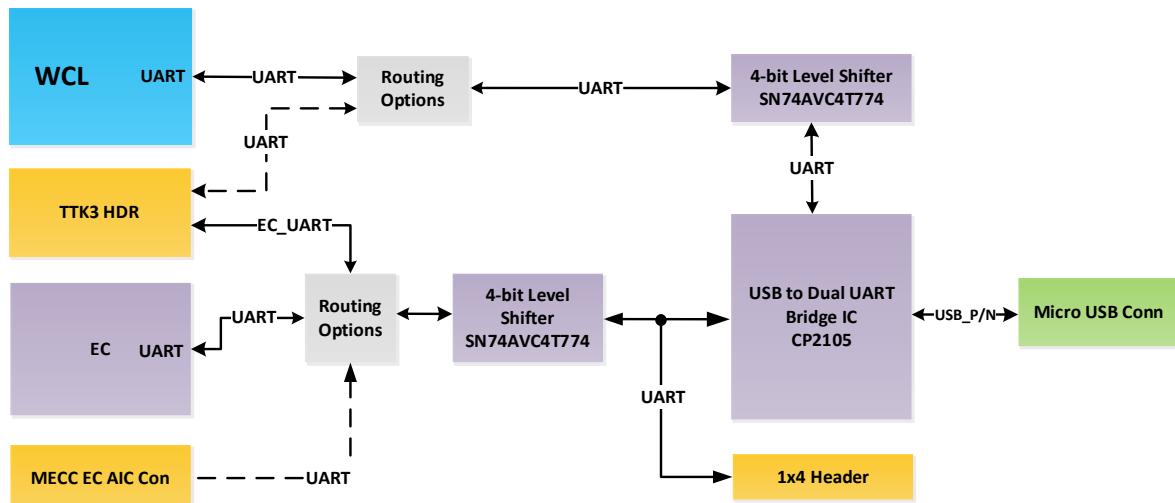


Figure 67: Serial debug console high level block diagram

Table 69: Micro USB connector and Pinout

MFG	Mfg. Part Number	IPN Number
Hirose	ZX62RD-AB-5P8(30)	E10610-003

Pin #	Signal Name
1	+V_VCC_USB_UART
2	USB_C_DEBUG_DM
3	USB_C_DEBUG_DP
4	NC
5	GND

23.3.3.5 LEDs

The WCL RVPs supports the following list of LEDs with their description given in below table.

Table 70: RVP LEDs & Function

LED Name	Functional Description	LED Color
CAPSLOCK	Driven by EC to indicate the CAPSLOCK condition	GREEN
NUMLOCK	Driven by EC to indicate the NUMLOCK condition	GREEN
SO_LED_DRV	Indicates system entering state - SO	GREEN

S3_LED_DRV	Indicates system entering state – S3	GREEN
S4_LED_DRV	Indicates system entering state – S4	GREEN
S5_LED_DRV	Indicates system entering state – S5	GREEN
SUS_LED_DRV	Indicates system sleep state	GREEN
ME_LED_DRV	When asserted, INTEL ME is off	GREEN
CATERR	On board LED to indicate catastrophic event driven by CPU.	RED
M.2_WLAN_LED1	Indicates WLAN Module availability	GREEN
M.2_WWAN_LED	Indicates WWAN Module availability	GREEN
M.2_BT_LED2	Indicates BT Module availability	GREEN
M2_SSD_DEVSLP_LED	Indicates Device sleep signal asserted connected on M.2	GREEN
SATA_DIRECT_DEVSLP_LED	Indicates SATA direct connect device sleep signal asserted	GREEN
PCH_SATA_LED	Indicates activating SATA	GREEN
PM_PWRBTN_LED	Driven by EC	GREEN
CHGR_LED_GATE_LED2	Driven By EC – Charging status	YELLOW
HGR_LED_GATE_LED1	Driven By EC – Charging status	GREEN
CS_INDICATE_LED	Indicates whether system is in Connected Standby(CS)	GREEN
C10_GATE_LED	Indicated C10	GREEN
PCIE_LINK_DOWN	Indicates PCIe link down and will be routed to LED and to header	AMBER

Table 71: WCL RVPs support following press buttons on board

Button	Function
Volume UP	Volume increase input to EC (Provided over header)
Volume DOWN	Volume decrease input to EC (Provided over header)
Power	External Power button input to the PCH and EC
Reset	External Reset button input to the PCH

Power and Reset signals will be routed to Front Panel Header and PM Side band header.

In general, for debug connectors, Refdes and pin numbering will be provided. Silkscreen for signal names can't be supported. Also, default power on from G3 state (i.e., no need to press power button) will be supported.

Table 72: Table depicting different debug features supported in WCL

Debug Features	Supported in WCL
SINAI2	Yes
InTEC	Yes
Port80 Display Output	Yes
Serial Debug Console	Yes
LED	Yes
Box Stress Test	Yes

23.4

Programming capabilities:

Devices programmable in RVP

- BIOS SPI Flash
- EEPROMs
- PD AIC
- Retimer Flash
- TTK3
- EC Flash
- Dediprog

23.5 Details of debug tools

The following tables provide the Manufacturer Part number supported on “Platform Name”.

23.5.1 Box Stress Tool

BST is an AIO integrated solution used for Voltage measurements, Voltage drive/margining, GPIO's manipulations, I2C master controller and Thermal Diodes measurements capabilities.

NTB FAB B (Nevo to BST Adapter)

BST hooks on to RVP 100pin Nevo connector with use of NTB adapter for ADC, DAC,GPIO's,ISENSE and I2C Controller functions.

For SoC Thermal Diodes measurements and BST onboard VR's auxiliary use case, dedicated cables are available as part of BST Kit.



Figure 68: Nevo to BST Adapter

Note: Users who want to use Nevo will need an Adapter card and extension cable.

Cable and extension adapter are part of Nevo demand call catalog which open every Quarter, kindly look at info below.

J34397-100	Nevo Extender Adapter	\$20
H82412-001	Nevo Extension cable	\$135

Nevo Extender Adapter – J34397-100



Extension cable – H82412-001



Figure 69: Nevo Extension Cable

23.5.1.1.1 Interface

BST hooks on to RVP 100pin Nevo connector with use of NTB adapter for ADC, DAC, GPIO's and I2C Master functions.

For SoC Thermal Diodes measurements and BST onboard VR's auxiliary use case, dedicated cables will be available as part of BST Kit.

23.5.1.1.2 Power Supply

For standard operation of ADC, DAC, GPIO's, I2C Master and Thermal diodes measurements the BST is powered from an USB Type-A to mUSB (5V from Host PC to BST).

For BST auxiliary use case a standard ATX with 12V/5V connector is required.

24 Power Delivery & Sequencing

In this section, all the WCL power delivery implementation details (with respect to energy management, rest of the platform power delivery, IMVP9.3, power sequencing, power measurement, voltage margining, power accumulator and PnP requirement) would be covered. High level SoC Power scheme for WCL is shown below, Figure 70 shows the pin map for MSU15W silicons sku, this MSU15W sku can be validated on RVP board.

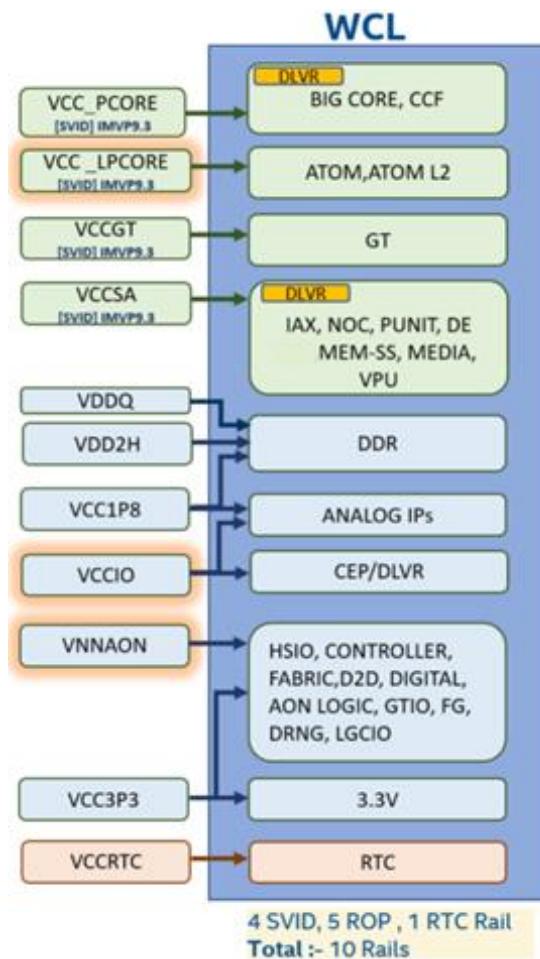


Figure 70: WCL High Level SoC Power Scheme

24.1 Power Sources

WCL can be powered through a standard AC adapter, a Type C power Adapter, or a Battery pack.

24.1.1 Standard AC adapter

A 230W adapter is being selected for the WCL RVP and is one of the three power sources which can be used for powering the RVP.

Standard AC adapter IPN: J82210-001

Description: AC/DC ADAPTER, 100V-240V Input, 50-60HZ, 19.5V/11.8A Output

24.1.2 Type C Adapter

There are two USB-C ports supported on WCL RVP, all ports are USB-C PD 3.1 compatible and can be used for plugging in the Type C adapter. EPR chargers more than 20V are **NOT** supported.

In the client segment, the market is shifting towards Type C adapter instead of AC adapter due to EU mandate common charger directive. Changing the EC-FW charging policy will deviate from guidelines given to customers through white paper and creates confusion. In order to support this initiative, WCL RVP design will incorporate a jumper solution which will allow higher priority to be assigned to Type C power in case both AC Barrel and Type C power is connected. This POC will be implemented on RVP2 LP5x T3 SKU.

Note: For dead battery boot with type-c adapter, minimum 45W adapter is required to boot the WCL RVP.

24.1.3 Battery Pack

A 3S1P battery pack is being selected for WCL RVP with maximum capacity of 61.5Whr.

3S1P battery pack **IPN:** M77304-001

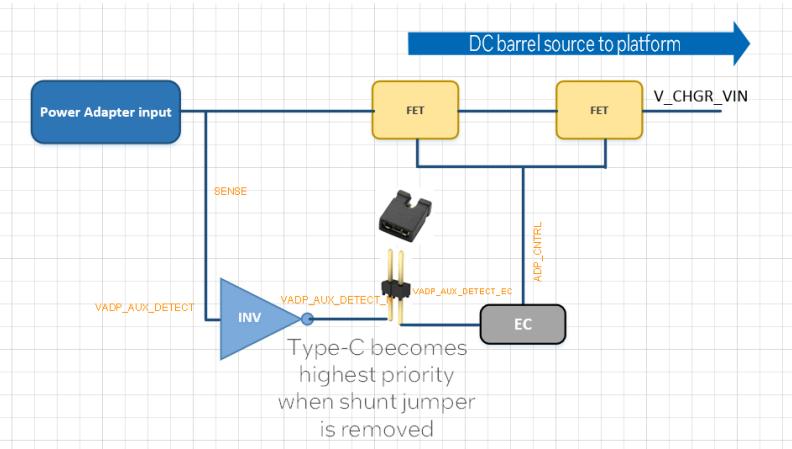
Recommendation: For all the validation except Performance, the recommendation is to use standard AC adapter. Use Type C adapter or battery pack on need basis.

Table 73: Power Sources & Priority on WCL RVP

Available Sources	Priority Given To
Standard AC Adapter + Battery Pack	Standard AC Adapter
Standard AC Adapter + Type C Adapter	Standard AC Adapter
Standard AC Adapter + Type C Adapter	Type C Adapter*
Standard AC Adapter + Type C Adapter + Battery Pack	Standard AC Adapter*
Type-C Adapter + Battery Pack	Type-C Adapter

Note: Smooth/seamless transition from Type-C adapter to AC adapter and vice versa is not supported if battery is not connected.

*WCL RVP design will incorporate a jumper solution which will allow higher priority to be assigned to Type C power in case both AC Barrel and Type C power is connected. This POC will be implemented on RVP2 LP5x T3 SKU.

**Figure 71: WCL RVP2 Jumper Solution to Set Type C as Higher Priority**

24.2 Key Power Delivery Subsystems

The platform power delivery has three key sub-systems which are Energy management, Rest of the platform (RoP) power delivery and CPU power Delivery (including IMVP9.3).

24.2.1 Energy Management Sub-System

Battery charger and USB power delivery comes under the energy management sub-system. A buck-Boost NVDC charger is used to charge the battery pack and to power the system with the input voltages from standard AC adapter and Type-C adapters. Battery charger PROCHOT# signal is connected to the SOC PROCHOT signal.

24.2.2

Rest of the Platform Power Delivery

Discrete voltage regulators are required for powering the CPU (non SVID), PCH and platform components, power sequencing and load switches form the RoP power delivery sub-system. The RoP power delivery circuitry is down on the mother board.

24.2.3

IMVP9.3 Sub-system

WCL CPU requires four different SVID rails (VCC_PCIE, VCCGT, VCCSA and VCC_LP_ECORE). VCC_LP_ECORE is new VR compared to MTL-U/P/H. An IMVP9.3 compliant controller is used for generating these rails.

Note: The power delivery sub-systems are on the motherboard.

WCL RVP will be designed for MSU15W to support the silicon.

For tuning load line other than POR targets, reworks on board or IMVP FW change or both may be required depending on the selected IMVP9.3 controller IC.

Table 74: Processor Line Vs. Phase Count

Processor Line	Phase Count Required (VCCPCORE+VCCGT+VCCSA+VCCLP_ECORE)
Processor Base Power – MSU15W	Baseline and Performance PD: 1+1+1+1

Iccmax, TDC and load line targets for different processor line is shown in Table 75.

Table 75: Processor Line Power Specifications

	MSU15W (2P+0E+4e)		
Rail Name	Icc_max/Iccmax.app	I_PL2/I_TDC	LL (mΩ)
VCC_PCIE	43.5A/30.5A	27A/23A	5.2
VCCGT	25A/17.5A	15A/--	6.6
VCC_LP_ECORE	35A/24.5A	21.7A/11A	8.0
VCCSA	35A/24.5A	15.4A/--	8.0

24.3

Critical Rails and Default Voltage Levels

The below table for all the critical rails and the default regulated voltages.

Table 76: Critical Voltage Rails with default regulated voltage

Voltage Regulator	Default Voltage	Comments
+VCC_PCORE	0V (Boot Voltage) 0.52-1.52V	CPU adjusts the output voltage through SVID.
+VCCGT	0V (Boot Voltage) 0.52V-1.26V	CPU adjusts the output voltage through SVID.
+VCCSA	0V (Boot Voltage) 0.52V-1.23V	CPU adjusts the output voltage through SVID.
+VCC_LP_ECORE	0V (Boot Voltage) 0.52V-1.52V	CPU adjusts the output voltage through SVID.
+VNNAON	0.77V	
+VCCST	0.77V	MB PG From VNNAON
+VDD2H	1.065V (LP5x Mem Down)	Shared rail (LP5x memory + CPU) in LP5x SKU
	1.1V (DDR5)	SoC Only (DDR5)
+VDDQ	0.52V(LP5x Mem Down)	Shared rail (LP5x memory + CPU) in LP5x SKU
	1.1V Tied with +VDD2H	SoC Only (DDR5)
+VDD2L	0.92V	Applicable for only LP5x memory (For DVFS support)
+VDD1	1.8V (LP5x Mem Down)	LP5x Only
+VCCIO	1.25V	
+V3.3A	3.3V	
+V5A	5.0V	
+V1.8A	1.8V	
DDR5 rail	5V	DRAM module only

Table 77: Typical Voltage rail for different Memory technologies

Memory Type	Supporting voltages on memory modules by RVP PD			
	VDD2H	VDD2L	VDD1	VDDQ
LPDDR5x	1.065V → SoC + LP5x	0.92V	1.8 V	0.52 V
DDR5	1.1V → SoC 5V → DRAM Module	NA	NA	NA

24.4

Power Map for WCL

Updated WCL power map would be placed in [LINK](#)

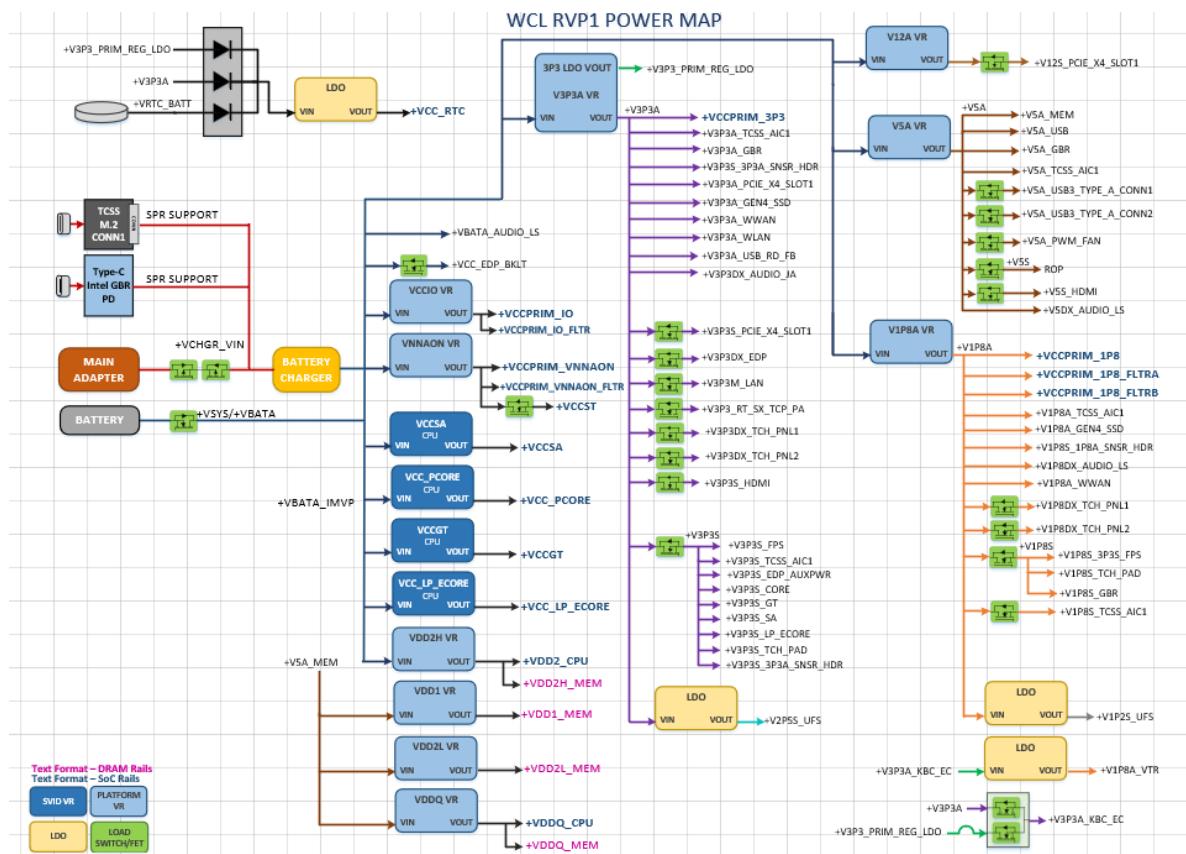


Figure 72: WCL RVP1 Power flow diagram

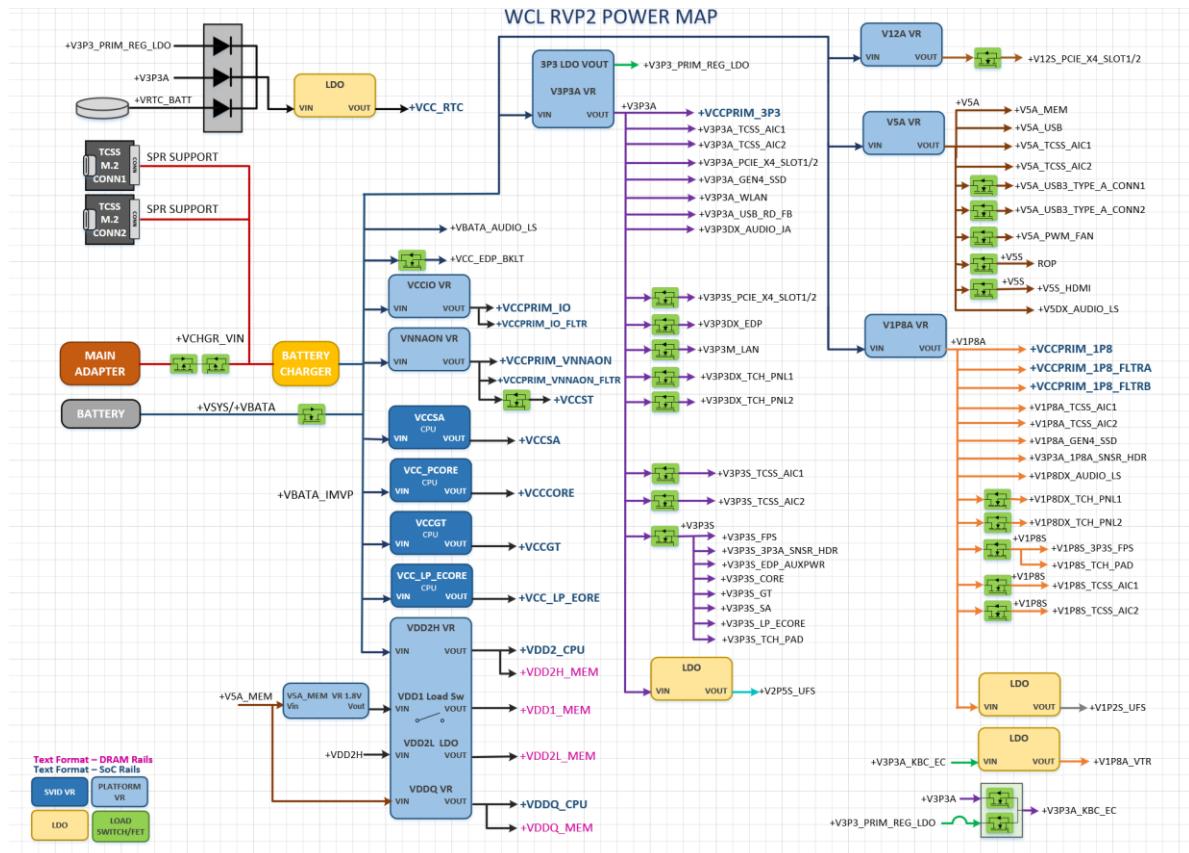


Figure 73: WCL RVP2 Power flow diagram

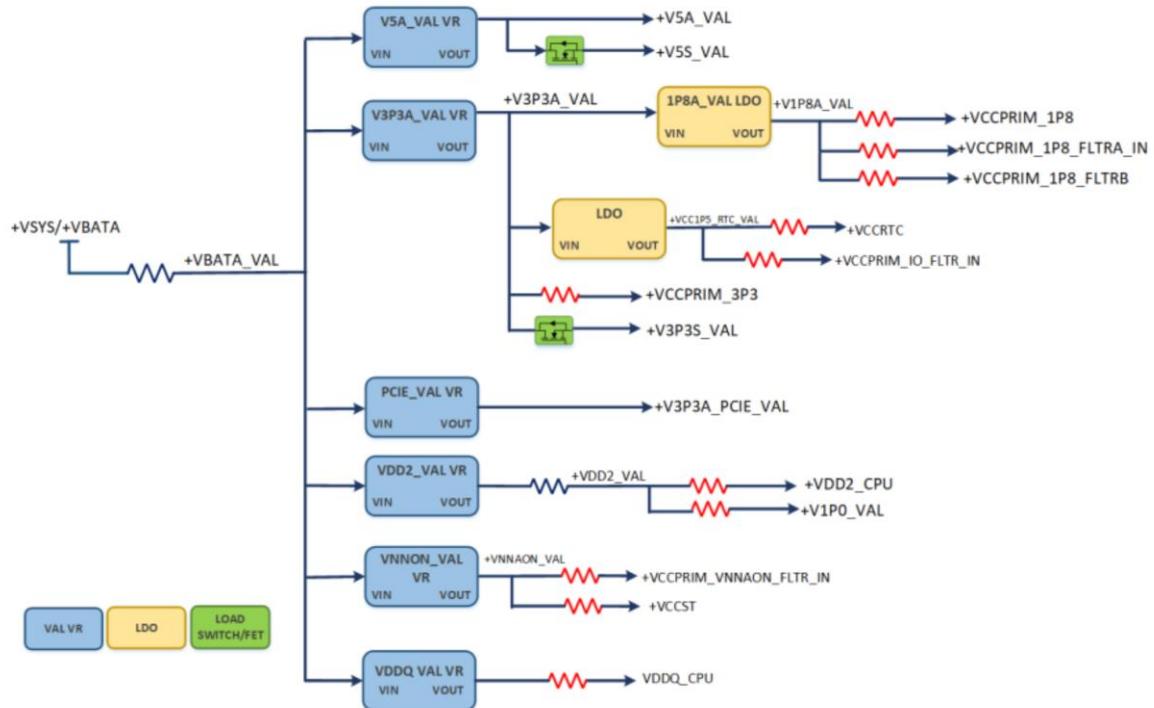


Figure 74: WCL VAL rails Power flow diagram

24.5 Power Sequencing

- WCL requires Four IMVP9.3 rails.
- IMVP9.3 voltage regulators are enabled by ALL_SYS_PWRGD signal which indicates all the platform rails are stable.
- VCC_PCORE, VCCGT, VCCSA and VCC_LP_ECORE IMVP9.3 VRs have Zero boot voltage requirement.
- SVID communication is required to change the voltage of IMVP9.3 VRs.
- WCL platform supports Pseudo G3 state.

WCL RVP Power sequencing diagram is available at [LINK](#)

25 Power n Performance

25.1 PRD from PnP for power measurements

RVP team will follow all the requirements which are mentioned in WCL Power and Performance requirements document ([Link](#)) . RVP also follows PnP PMR [BKM](#) to select the resistors MPNs.

25.2 Voltage margining

For the power and performance validation, margining is supported through Sinai Nevo connector and range of voltages supported are tabulated below. For SoC/PCH a separate +V3.3A _VAL is provided to support extensive range of margining than +V3.3A_VR.

Table 78: Voltage Margining support on WCL RVP

VR	VR controller		Nominal Voltage	Voltage range support by VR	Iccmax	Margining Support
	DDR5	LP5x				
+V3.3A	RT6585AGQW	RT6585AGQW	3.3	2.97V to 3.63V	0.1A	Yes
+V5A			5V	4.5V to 5.5V	2.5	No
+V1.8A	RT6220A	RT6220A	1.8V	0.6V to 5.0V	1.0A	Yes
+VNNNAON	RT8237KZQW	RT8237KZQW	0.77V	0.7to3.3V	11A	Yes
+VCCIO	RT6338AGQUF	RT6338AGQUF	1.25V	0.6 to5.5V	1.8A	Yes
+VDD1	RT5795AGQW	RT6300	1.8V	1.8V Fixed	0.25A	TBD
+VDD2H	RT8231AGQW		1.065V	1.065V Fixed	6.5A	TBD
+VDD2L	RT5795AGQW		0.92V	0.92V Fixed	2.9A	TBD
VDDQ	RT5795AGQW		0.52V	0.52V/0.32V (fixed)	1.8A	TBD
+VCC1P5_RTC	AP7354D-15FS4-7	AP7354D-15FS4-7	1.5V	1.1 to 4.5V	2mA	Yes

25.3 Additional Current support (for stress tests)

The IMVP VCC_PCORE, VCCGT, VCCSA and VCC_LP_ECORE VRs support additional +20% currents to POR PL2 currents to support stress tests on SoC.

The teams doing stress tests (that draw higher currents than POR) are expected to have external cooling (may be an external cooling fan) for VRs. Thermal solution on board does not support cooling requirements during stress tests for higher currents.

25.4

PnP PMR resistor

2x7 headers are provided on board which brings out voltage and current sense points from the board that can be used for Power and Performance measurement of different power rails for both PCH and CPU and different on-board interfaces. Few of 2x7 connection pairs are left spare, provision to wire for additional measurements on board.

SoC/PCH and CPU current sense lines from Power Measurement Resistor (PMR) are connected to dedicate 2x7 headers. 2x7 HDRs mapping to PMR resistors is available in [LINK](#). CPU and PCH rails assigned/grouped to 2x7 HDRs to optimize the cable connections to NI DAQ.

Special attention from PnP (CPU, SoC/ PCH & ROP PnP) team is required on type of the PMRs used in WCL RVP. Previous programs use the PMRs only from Vishay, WCL program follows different approach to enable PMRs from the multiple vendors includes Vishay. Approach in WCL is to select the PMRs from the different vendors with the criteria provided in the BKM below:

[**PMR BKM Link**](#)

25.5

Power Accumulator

Six power Accumulators (PAC1954T) provided for measure power in following rails. Each power accumulator has 4 channels, Per Channel 48-Bit Power Accumulators Capture 17 Minutes of Data at 1024sps. Also has per Channel 12-Bit Voltage Registers. The data can be read through PCH SM bus.

Power meter mapping for WCL RVPs is captured in following Table 79.

Table 79: WCL RVP1/RVP2

S.No .	Power meter PAC1954	C H	Rails	Domain	SMBus Address	ADDRESL_RES (ohm)	I2C Bus Number
1			1 +VCCCCORE	CPU			
2		1	2 +VCCGT	CPU			
3			3 +VCCSA	CPU			
4			4 +VCC_LP_CORE	CPU			
5			1 +VNNAON	CPU			
6		2	2 +VCCIO	CPU			
7			3 +VCC_3P3	CPU			
8			4 +VCC1P8	CPU			
9			1 +VCC1P5_RTC	CPU			
10		3	2 +VCCST	CPU			
11			3 +VDD2H_CPU	CPU			
12			4 +VDDQ_CPU	CPU			
13			1 +VDD2H_MEM	DRAM			
14		4	2 +VDD2L_MEM	DRAM			
15			3 +VDDQ_MEM	DRAM			
16			4 +VDD1_MEM	DRAM			
17			1 +VCC_EDP_BKLTX1	Display			
18			2 +V3P3DX_EDPX1	Display			
19		5	+V3P3A_WLAN (Default) +V3P3A_WWW(non-POR)	Connectivity			
20			4 +V3P3DX_SSD1	Storage			
21			1 +VBATA_CORE	System VBATA			
22		6	2 +VBATA	System VBATA			
23			3 TBD				
24			4 TBD				
25	Power meter PAC1952	C H	CPU SENSE	Domain	SMBus Address	ADDRESL_RES (ohm)	TBD
26							
27		1	1 SENSE_VCC_CORE	VCCCCORE PKG SENSE			
28			2 SENSE_VCCGT	VCCGT PKG SENSE			
29			1 SENSE_VCCSA	VCCSA PKG SENSE			
30		2	2 SENSE_VCC_LP_ECORE	VCC_LP_ECORE PKG SENSE			

26 PPV (Processor/Product Platform Validation)

WCL RVP is used in PPV environment for silicon screening.

26.1

PPV support on WCL RVP

WCL shall support the necessary mechanical and PPV specific socket KOZs required for PPV environment without deviating from POR platform requirements. IO Assignment is covered in the respective IO section. That should be referred to know the exact mapping.

PPV SKUs key board level interface requirements :

1. Side band header – for key control signals
 - a. Pins 35/37/39 go to the FRU ROM after the "isolation" jumpers, so we can remove jumpers and FRU connects ONLY to STHI, not to MB SMBUS
 - b. +VRTC_BATT is exactly that' the RTC Coin Cell battery.
 - c. There are 4 EDM pins, connect to DUT as appropriate: for U Package for example, 2 to CPU, 1 to EDRAM, with stuffing option for second PCH if applicable, and one to primary PCH.
 - d. Pins 4/6 are the SMBUS connected to the Port80 PLD
2. InTEC header – for thermal connection
3. SINAI2 header – for analog voltage and current sense and a couple DIOs
4. SPI TPM header – For BIOS emulator / programming with stuffing option to allow disconnecting SPI down to have emulator ONLY
5. Debug log capability using either DB9 connector or via uUSB
6. PPV socket specific PDBOM implementation.
7. Header for I2C CLK/DATA connecting to on board FRU EEPROM.
8. PCIe x1 slot – One PCI-E x1 slot on the board to cable PCI-E to host system to connect other PCIe devices down-stream from a bridge.
9. PPV BOM ID should retain same as RVP BOM ID.

PPV SKUs custom BRD requirements :

1. CPU pad must have Solder Resist Opening (SRO) 25um radius / 50um diameter larger than the pad, example 250um pad would need 300um SRO. This is to optimize socket alignment.
2. No silk-screen under socket zero height KOZ area, to avoid silk screen lifting socket slightly off board, impacting socket reliability.
3. NiPdAu plating (aka ENEPiG) with Nickel, Palladium, and Gold on surface for the PPV specific builds PCB to make more durable for use in factory.
4. Must review DFx (DFM/DFT) with SIMS team to enable smooth transfer of PPV builds to SIMS to support future builds past PRQ.
5. Mechanical & Socket KOZ / KIZ

27 Mechanical

27.1 Form Factor

The WCL RVP will follow LNL-Mx RVP Form Factor → Board size: 7.35" x 11.1". RVP will provide mounting holes such that it aligns to EPS as well as PPV chassis. Each of the holes will follow the standard ATX Mounting Hole specification (Diameter-156mils) & KOZ.

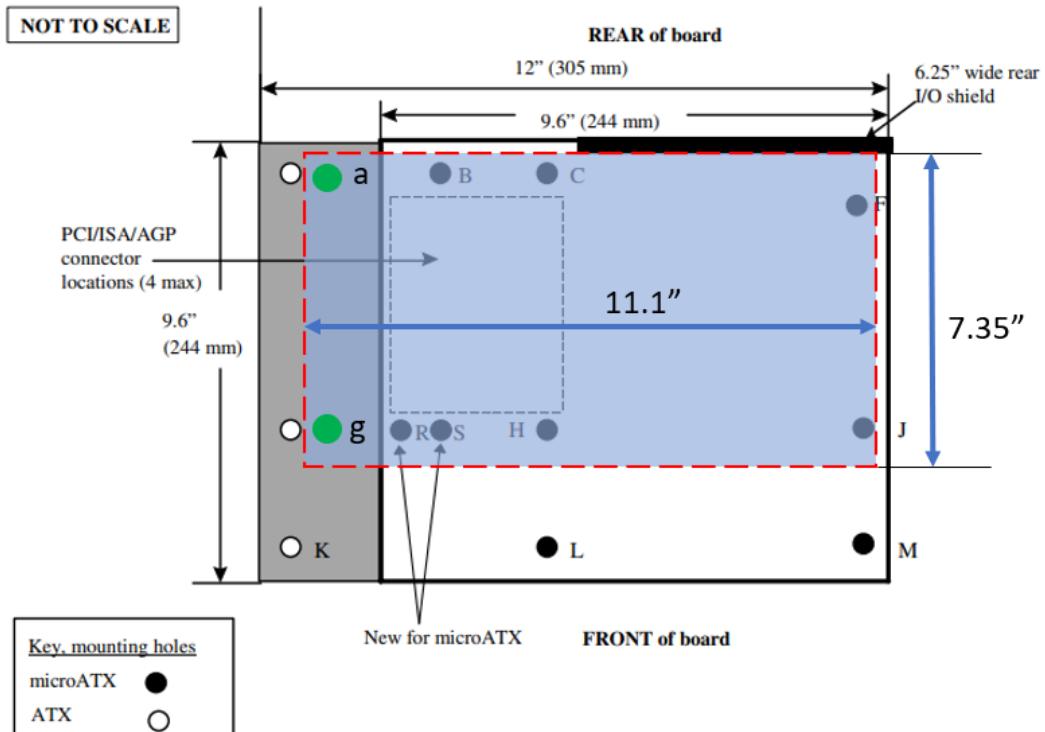


Figure 75: WCL RVP Form factor details

28 Chrome Requirements

Chrome architecture varies a little from Windows architecture and Chrome teams need a mechanism to validate delta hardware requirements on the WCL RVP. Delta subsystems include,

- Chrome EC
- Audio
- Chrome security chip (H1)
- Chrome debug header SERVO
- TCSS Modular TCPC AIC

28.1 Chrome support on WCL RVP

WCL RVP supports chrome requirements using Microchip EC on-board. EC to support many other features – WOV, TCPM, Integrated Sensor hub for sensor attach, integrated TCPC ports (in few cases). These features are different from Windows EC.

RVP includes the Chrome EC part MEC1727N-B0-I/SZ-CHRO on-board with some BoM changes for Chrome requirement. No support for Chrome EC AIC on the MECC connector in WCL RVP.

H1 security IC and Servo debug header will be supported using a new H1-Servo AIC. Dauntless (H1D3) GSC (Google Security chip) AIC to be supported on Chrome SKU using H1 AIC and TTK3 header. H1 AIC supports SMBUS based controller to support chrome keyboard validation.

A dedicated Chrome BOM SKU will be supported in **LP5x (RVP2)** SKU of WCL RVP to enable these features by default. Configuration support model planned for Chrome on WCL RVP as follow:

- Config: onboard EC(Microchip) + H1-Servo AIC + WCL M.2 TCSS module on two TCP ports.

Note: Chrome requirements have slight changes and are yet to be confirmed. This section might have some modifications once confirmed from Chrome team.

High level block diagram for Chrome from RVP side is shown below.

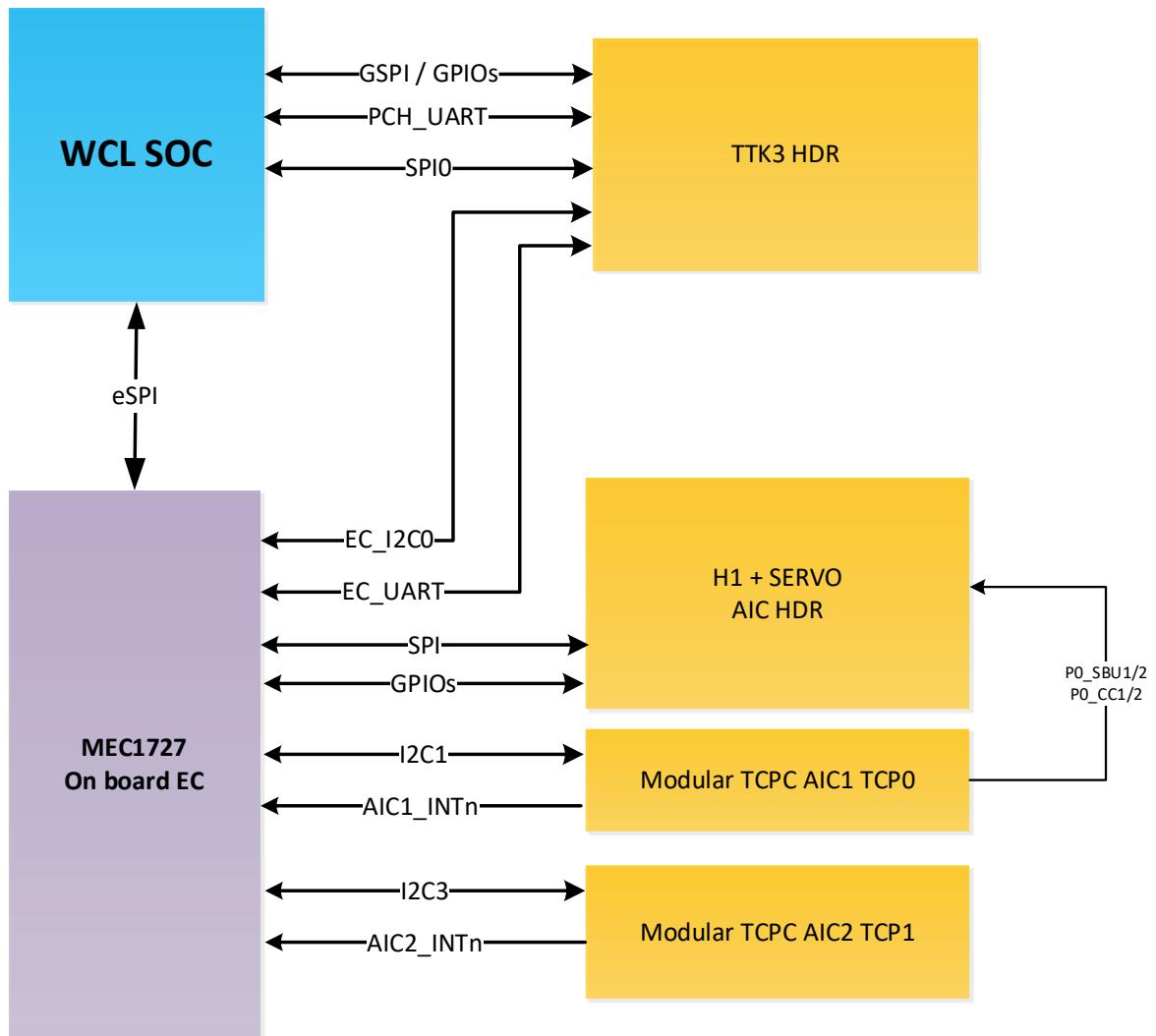


Figure 76 : Chrome support High Level block diagram with on-board Chrome EC

28.2 H1-Servo AIC

H1-Servo AIC is designed based on dauntless GSC security chip. This AIC includes,

- Chrome security chip: It communicates with EC & AP over SPI and does following features.
 - Reset functions
 - Closed case debugging
 - Verified boot
 - Security features
 - Battery cutoff
- Servo header:

- Access UARTs of EC, CPU, ISH, TPM, PD
- Flashing firmware like EC, Coreboot, PD, TPM
- Access device GPIOs like power button, cold reset, warm reset, volume buttons, keyboard pins, lid, etc
- SMBUS companion IC and keyboard connector to support chrome keyboard validation.

TTK3 & H1 connector pinout details are shared over [Link](#)

Table 80: TTK3 & H1 Connector

MFG	Mfg. Part Number	IPN Number
Samtec	ASP-203744-03	K18833-001
Samtec	ASP-159358-09	G25403-004

28.3

Chrome USB-C support

WCL Chrome planned to support M.2 Modular TCPC AIC on two ports. TCSS module details are provided in link <https://goto/tcssmodule>

Chrome USB-C modular AIC includes single port TCPC and PPC. USB-C connector and the retimer are available on the module. SBU mux shall be added on this AIC for considering SBU signals for DP/debug alternate modes. This AIC follows the latest 2.04 spec PD AIC pinouts. I3C debug over TCP0 is supported. Two different I2C ports from EC are provided for individual TCP port modules.

To support CCD debug, SBU and CC signals connected to H1 AIC connector. An external 3:1 SBU mux shall be provided to select between retimer or H1 SBU path.

Below block diagram shows the WCL USB-C TCPC Chrome support.

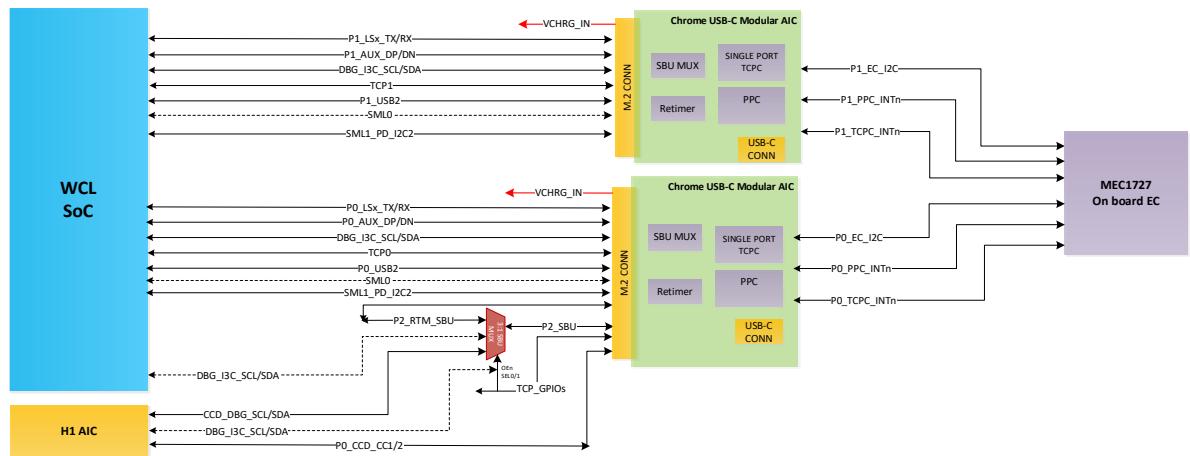


Figure 77 : WCL Chrome CCD support

29

Regulatory & Product Ecology

The following items must be satisfied to meet regulatory and ecology requirements for the WCL RVP.

- An unauthorized device label needs to be attached/tied to the RVP board at the factory. Intel part number K21553-003 (or later) should be used.
- A safety flyer must be shipped with the RVP board. Intel part number J10643-003 should be used and the flyer should be included in the packaging box of RVP board.
- Review batteries (including coin cell) being shipped/used with the RVP for proper shipping and safety compliance. The following certificates should be obtained in cooperation with SSC (MSO): UN38.3/MSDS/1.2m drop, CSTCG (Dangerous good), CB (IEC62133), UL1642, REACH SVHC, and EU battery directive. Please refer to DocLocator document "Battery Selection and Approval Procedure" [DL-0002566](#) (legacy SNAP 227-0029), for details.
- Review power supply being shipped/used with the RVP for safety and energy efficiency compliance in the region it is being shipped. For previous RVPs, power supplies with NRTL certification and US Dept. of Energy Level VI efficiency rating have been used. Please refer to DocLocator document "Mains Connected Power Supply Selection and Approval Procedure" [DL-0002565](#) (legacy SNAP 227-0028), for details.
- Intel Pre-lease Loan Agreement (IPLA) "One Pager" must be shipped with the RVP board. It communicates the important legal information about the DV to customer. Intel part number M21973 should be used and included in the packaging box of RVP board.
- When shipping with a battery, there needs to be a battery warning label on the packaging. Li Metal Battery Warning Label (including coin cell if shipped from China): IPN: J72126-004 and/or Li Ion Battery Warning Label: IPN: J72128-004.
- The RVP BOM needs to be reviewed and undergo a risk assessment by a Product Ecology Engineer and given a ship approval. The results will be documented in the product regulatory plan.
- Ecology labeling needs to be attached to the packaging to show compliance to CA perchlorate requirements. Perchlorate label, (sample IPN: D85237-001), needs to be affixed to the packaging of the board containing coin cell battery shipping to CA. Please refer to DocLocator document [DL-0002372](#) "Environmental Product Content Specification for Suppliers & Outsourced Manufacturers" (legacy SNAP 18-1201), 3.5 for details.
- Review components containing laser emitters for eye safety compliance before usage. shall follow distribution requirements outlined in the Laser Regulatory and Product Safety Requirements [DL-0002555](#) (legacy SNAP 227-0009).
- Review radio (Wi-Fi, WiGig, cellular, BT, NFC, etc.) components for regulatory staging and carrier access compliance in the regions it will be used in.
- Complete radiated emissions (EMI) scans to the limits of the regions it will be shipped to ensure no harmful interference (shall be performed with assistance from the PRE). A schematic and layout review for EMC and RF by PRE is recommended.
- Undergo a Safety Review by a qualified Product Regulations Engineer (PRE) or 3rd party certified safety testing organization and found to be "reasonably safe" as defined in the Intel Corporation "Product Regulations Methodology Specification", [DL-0002650](#) (legacy SNAP 227-GS0021). The criteria used for the safety review are based on the current version of

“Information Technology Equipment - Safety”, IEC 62368 or other relevant product specific safety standard.

DocLocator documents can be found here:

<https://doclocator.intel.com/>

30 RVP Health DAC

30.1 RVP Health DAC: A novel way to access remote hardware & accelerate debug

The product development life cycle is accelerating at fast pace and platform design complexity continues to increase exponentially. The platforms continue to evolve rapidly, to address aggressive schedules and products time to market goals. A reduced overall silicon development cycle warrants a faster and efficient validation environment. But root-causing platform failures in these circumstances becomes a huge challenge. Accessing and debugging remote deployed systems, becomes a big herculean task. In this challenging ecosystem, it's extremely important to innovate efficient mechanisms for faster debug, to enable high quality validation and bug fixes.

RVP Health DAC (Debug Acceleration card) is a novel approach that facilitates faster remote debug monitoring & root cause of platform issues. It gives a completely new dimension to diagnostics, remote platform access and validation. It's a pluggable kit solution, which reduces main platform design dependency. Thoughtfully designed as a scalable/reusable solution across big & small core products.

30.2 RVP DAC (Debug Acceleration Card) Goal is to enable “Remote debug and accessibility” of deployed RVP to validation customers.

RVP Health DAC is based on Intel Altera based MAX10 FPGA (Field programmable gate array) for probing and processing of debug signals. Main goal of DAC (Debug Acceleration card) is to facilitate faster remote debug, monitoring, and root cause of issues. All these features are enabled via user friendly GUI (Graphical user interface).

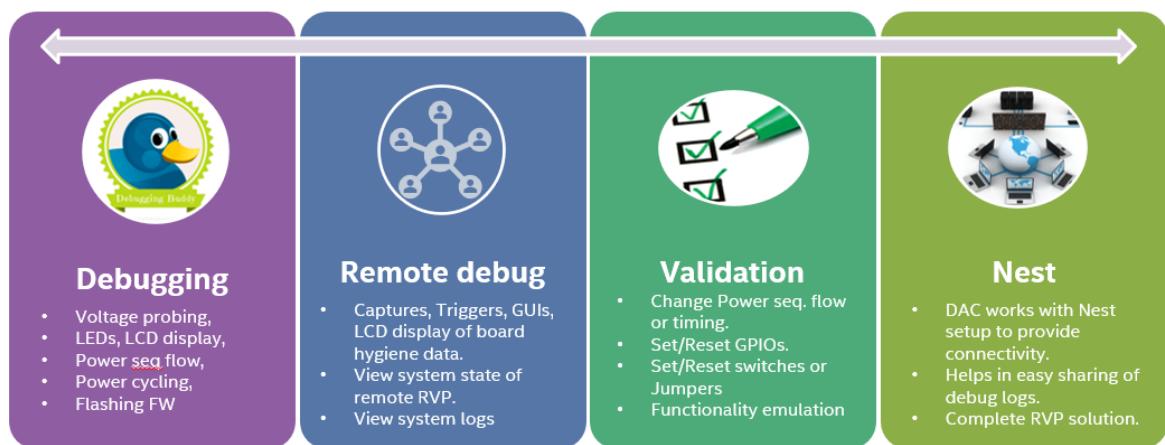


Figure 78 : Strategy for debug acceleration card

30.3 The RVP Health DAC solution can be divided into two parts:

30.3.1 Hardware Interface

The DAC (Debug acceleration card) does not need any special header to connect on RVPs.

The overhead is avoided by using existing headers to tap the signals from RVP to provide all the features. This salient unique feature of DAC makes it scalable across all the RVP segments of S, P, M and atom segment N too. There is a single custom designed 100-pin cable on DAC side for ease of connectivity. The HW unit is assembled and shipped in a chassis and a 100-Pin cable, AC-Brick adaptor is included in packaging box. All the soft collaterals and list of key contact are available at <https://goto.intel.com/rvpdac>.

The detailed block diagram of RVP Health DAC is as given below:

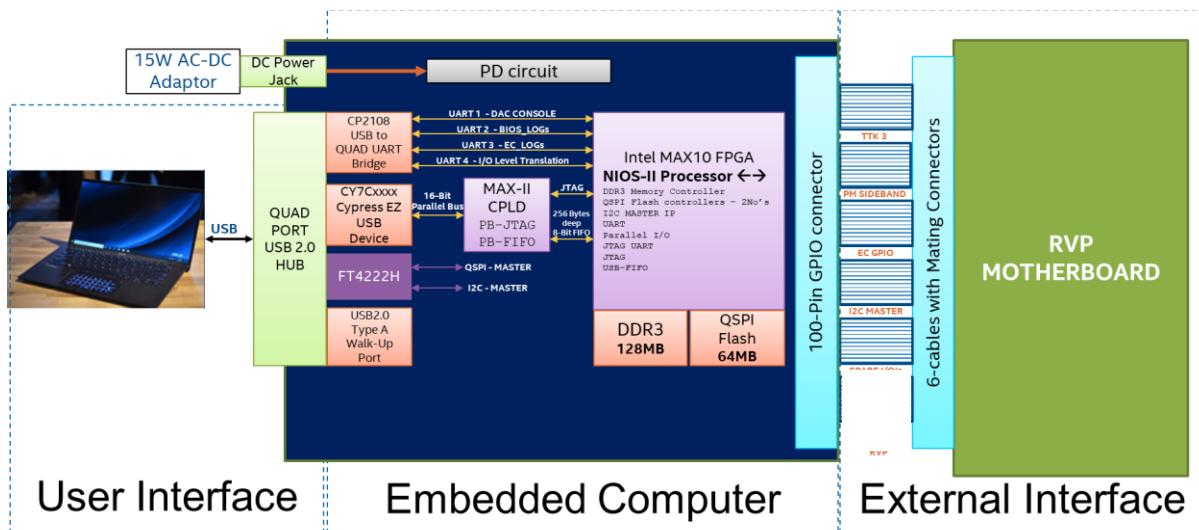


Figure 79 : RVP DAC Block Diagram

The RVP Health DAC snapshot is as given below:

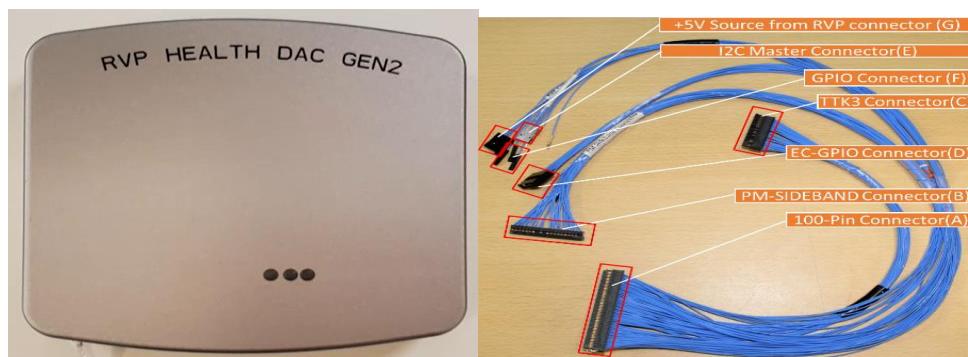


Figure 80 : Snapshot of RVP DAC with Cable

30.3.2 Software interface

For the ease of debug for validation customers, instead of console command-based interface, DAC has been designed with simple, light weight Python based windows GUI application. Below picture of DAC GUI depicts the post code displayed in red, on right side. The console down shows the status of RVP boot and COM port detection. The power monitor shows the status of signals on RVP on successful DAC connection.

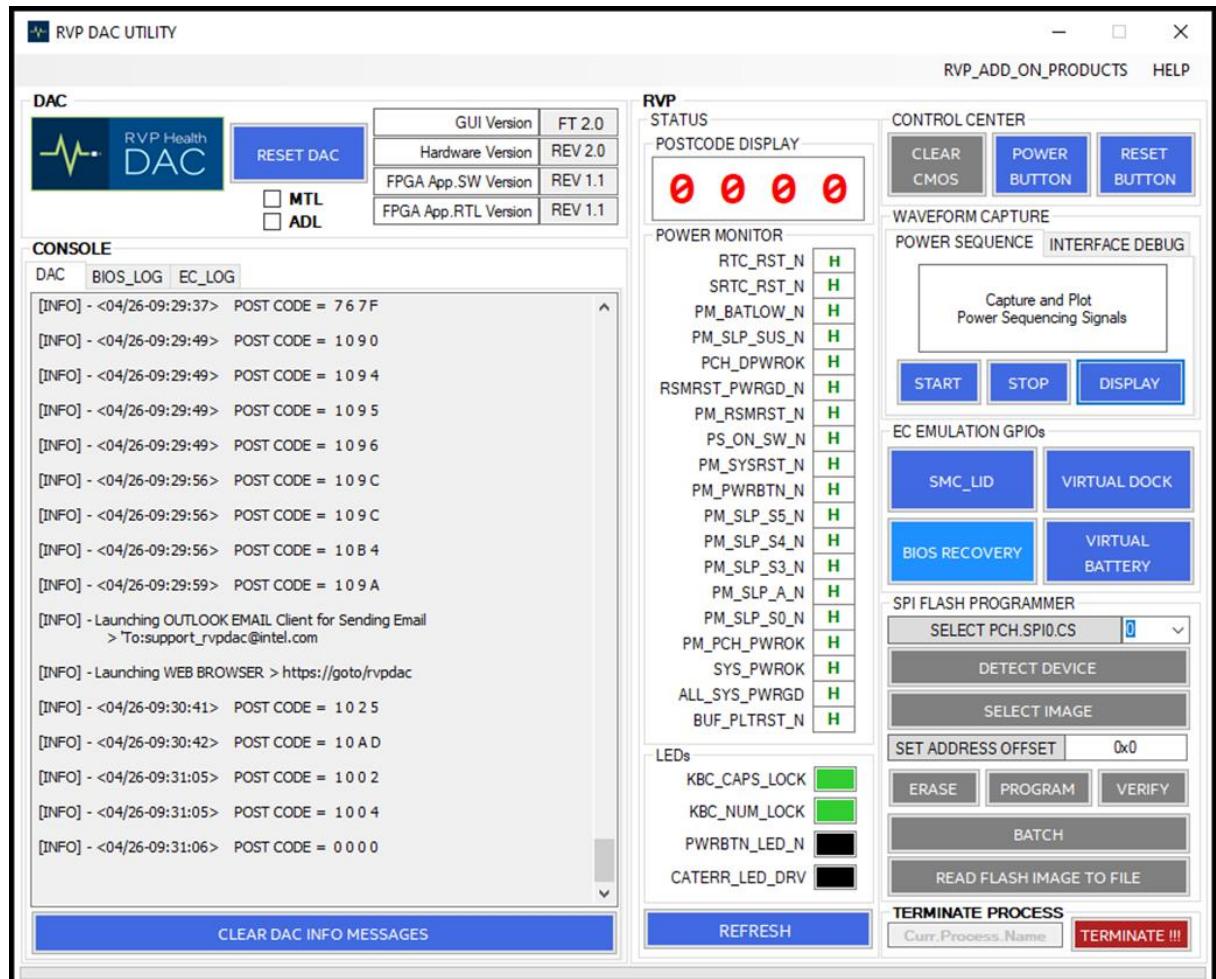


Figure 81 : Debug acceleration graphical user interface and features

Here are the main features that DAC supports -

- 1) **Communication between HOST and RVP DAC over USB-UART**
- 2) **Reset the RVP DAC from HOST**
- 3) **Configure RVP DAC from HOST**
- 4) **Control RVP power-button & reset-button**
- 5) **Interface RVP DAC to Target motherboard**
 - 1) **Clear CMOS operation**
 - 2) **Sniff and Display**
 - POST Codes over PORT 80

- Num-Lock LED
- Caps-Lock LED
- CAT_ERR_LED
- PWR_BTN_LED

3) Control EC Emulating GPIOs

- Lid Close/Open
- Battery Charger Connect/Disconnect
- Dock Connect/Disconnect
- Set BIOS Recovery Mode ON/OFF

4) Read and Plot

- Power Monitoring signals
- Interface debug signals

5) SPI FLASH Programming

6) Read or Program PSS data <WIP>

7) Capture and save debug Logs over

- BIOS UART
- EC UART

For more info on RVP Health DAC, please refer below links:

Link to Intro video	: DAC_Introduction.mp4
Link to User Guide	: RVP_DAC_UG_Gen2_REV1p0.docx
Link to I/O connector details	: M37690-001.xlsx

31 UCP-SQUID

31.1 Low cost, Multi-Protocol and Remote programming solution

Intel RVP motherboard is the primary validation hardware for Intel CPUs and these motherboards host various ROM devices that store the firmware required. During debug and validation there is frequent need for updating these components and validation engineers need to identify the programming dongle for the ROM device, install the software utilities and drivers, identify where and how to connect the external programming dongle to the motherboard and then proceed for programming.

Traditionally, updating firmware on to each programmable components on Intel RVP motherboard users require different external programming hardware based on the communication protocol supported by the component like SPI NOR Flash for BIOS, I2C EEPROMs for Retimer, PD-Controllers, Firmware Records Unit, Programmable Voltage Regulator Controllers etc., on motherboard and these hardware modules when left attached to motherboard they gate systems from boot.

UCP SQUID is one tool supporting programming over SPI, I2C, SWD and JTAG. It also has GPIOs that connect to Front Panel HDR of RVP and help to get or set the system states. UCP SQUID also has tiny paddle boards and cables designed for needs of Intel RVPs as part of Hardware KIT. The paddle boards host FET devices which enable for systems to boot with UCP SQUID programmer connected to the platform, thus enabling the remote programming hardware tool for Validation teams.

A GUI software package to be installed on HOST PC that can identify the Intel RVP model name, List the reference designators of programming headers, and allows users to program each component individually or all devices in a single click of button. It also allows seamless integration to automation setups through APIs developed in Python, C#, and C++.

With UCP-SQUID **cost savings of about 75%** can be achieved by replacing the multiple programming hardware tools with single hardware module and GUI software significantly reduces time and effort of the users in identifying the ref.des of programming headers on motherboard, identifying the right programming dongle and Installation of each tool's software and drivers.

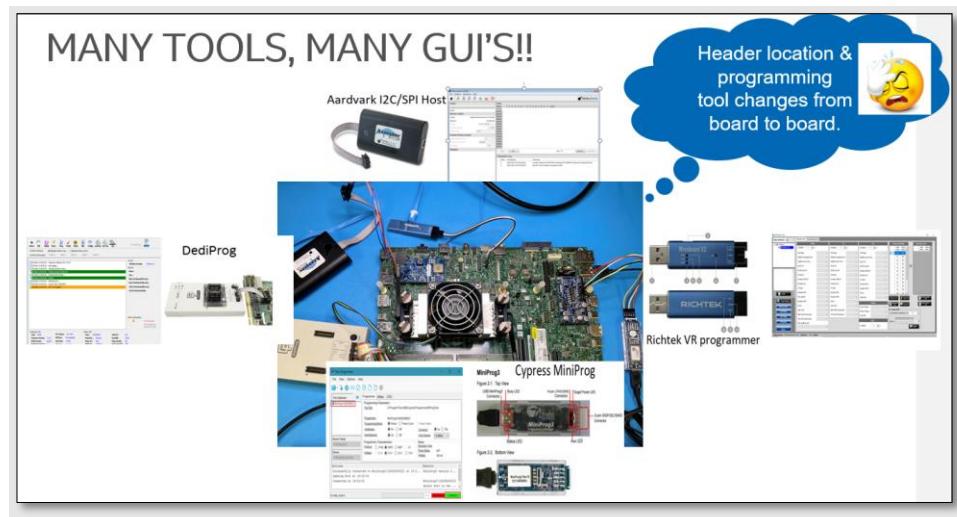


Figure 82 : RVP Eco System: UCP SQUID

Current day changes to work models such as Hybrid / Remote increase the need for remote access to hardware and the current day third party programming tools limit this functionality as they are not system state aware and gate the SUT to proceed for boot. This problem is partially address by In-System programming approach by software, but they are dependent on functional status of hardware.

31.2 Solution

UCP (Universal Configurable Programmer) is the vision of Platform and Systems Engineering RVP (CCG-CPS-CPE-PSE-RVP) Team to address the problem statement and is realized using the SQUID Hardware developed by Intelligent Validation Tools Engineering Team(iVE-IDC).

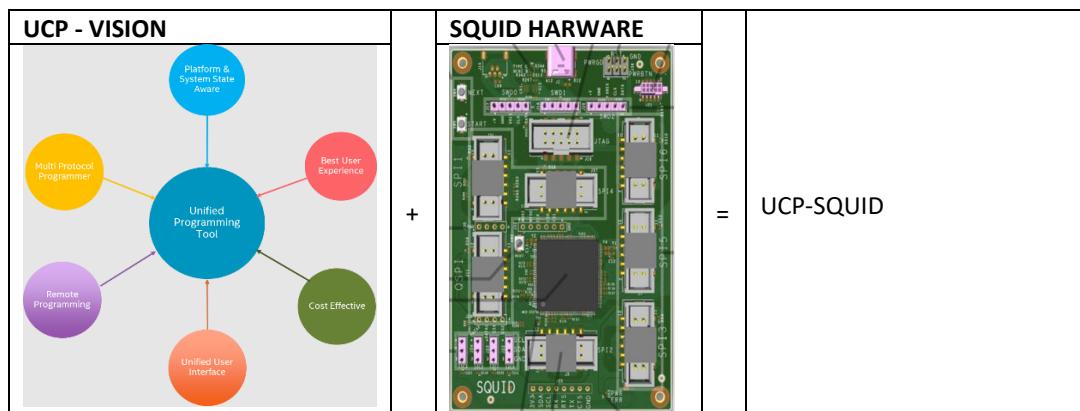


Figure 83 : UCP-Solution

31.2.1 Hardware

UCP-SQUID is a Micro-Controller based hardware that can support programming of up to 7-SPI Devices, 4 – I2C Devices, 3 – SWD Devices and 1 JTAG Interface port. It is connected to HOST as a USB device and the device and using the cables specifically developed for the requirement are used to connect to programming headers on the DUT. For the solution to system state aware a 2x3 pin header is provided on the hardware which can be cabled to Front Panel of the RVP to control the power button, reset button, and get the system power status. The Paddle boards mentioned in the Kit items host a FET isolation circuit that will allow to disconnect the programming cable connection load on to the RVP traces when not in use. Thus, enabling true remote programming operation for the system under test.

31.2.1.1 Block Diagram

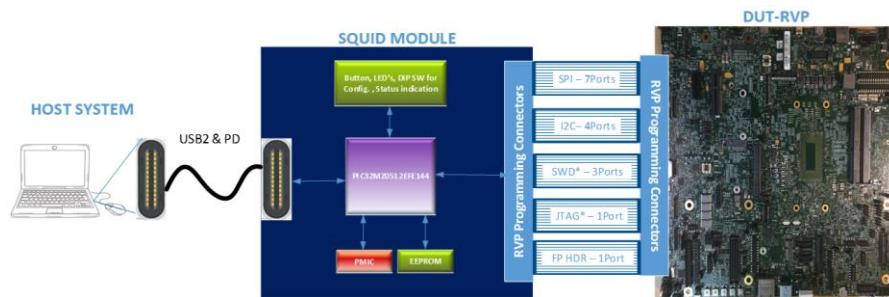


Figure 84 : UCP-Block diagram

31.2.1.2 Kit-Items

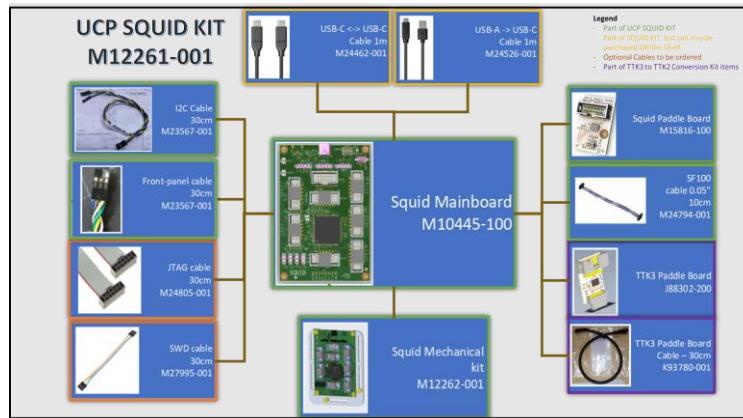


Figure 85 : UCP-Kit item

31.2.2 Software

UCP-SQUID can be accessed through HOST PC either in API mode or GUI utility. The GUI utility automates scan for SQUID USB devices connected at launch and upon successful detection proceeds to identify the RVP Motherboard model by accessing the RFID/I2C Tag EEPROM chip on the motherboard. Once the detection is successful it lists all the programmable ref.des header on the platform from which user can

select choice of device then select the firmware image to programmed or request to readback content of the ROM device to file

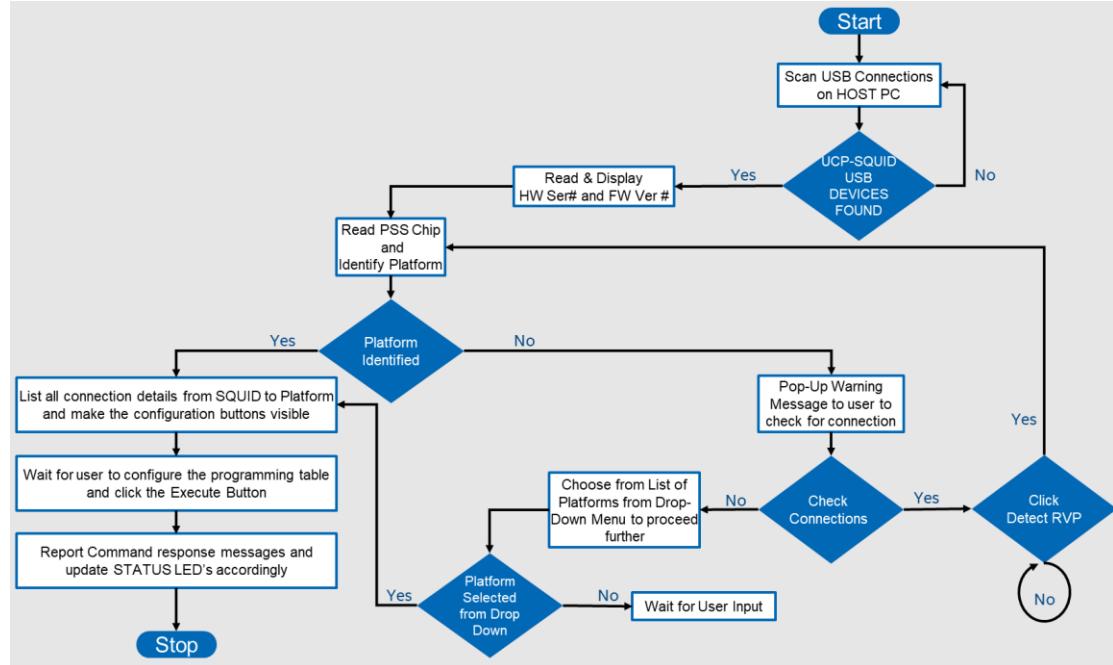


Figure 86 : UCP-SW flow

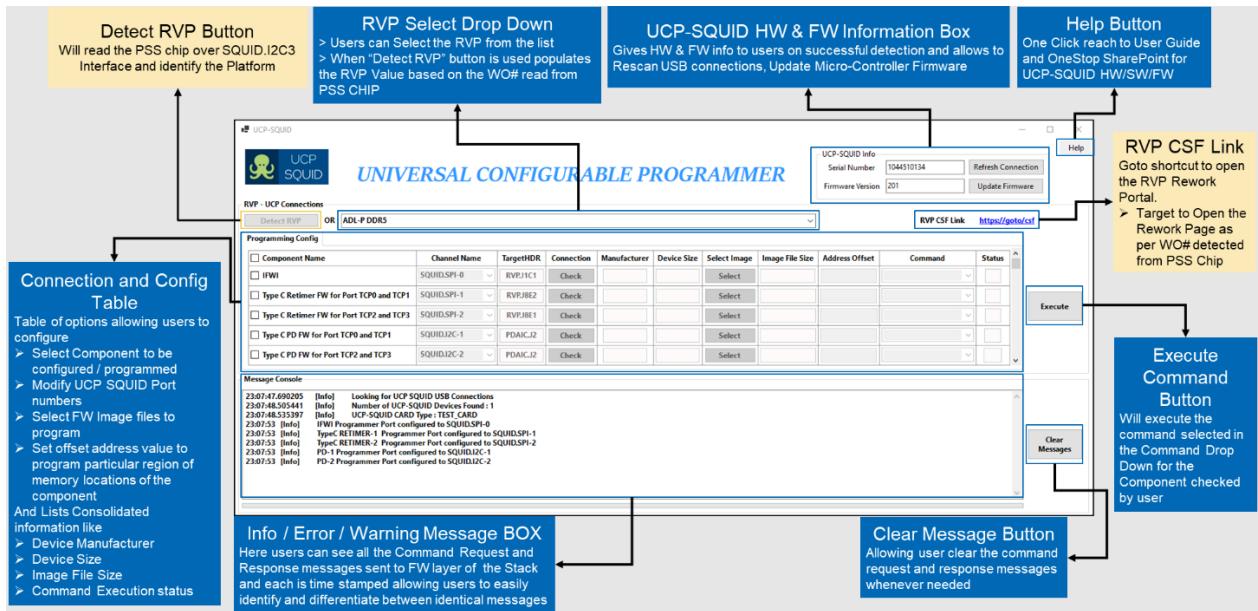


Figure 87 : UCP-GUI

31.3

Cost of Solution

Today the solution is priced at \$ 250 including all required ingredients. However, we are working on a “low-cost” reduced version of SQUID. The final price should be defined soon.

More details about UCP SQUID can be accessed at below link:

* [UCP SQUID Abstract Demo.pptx](#)

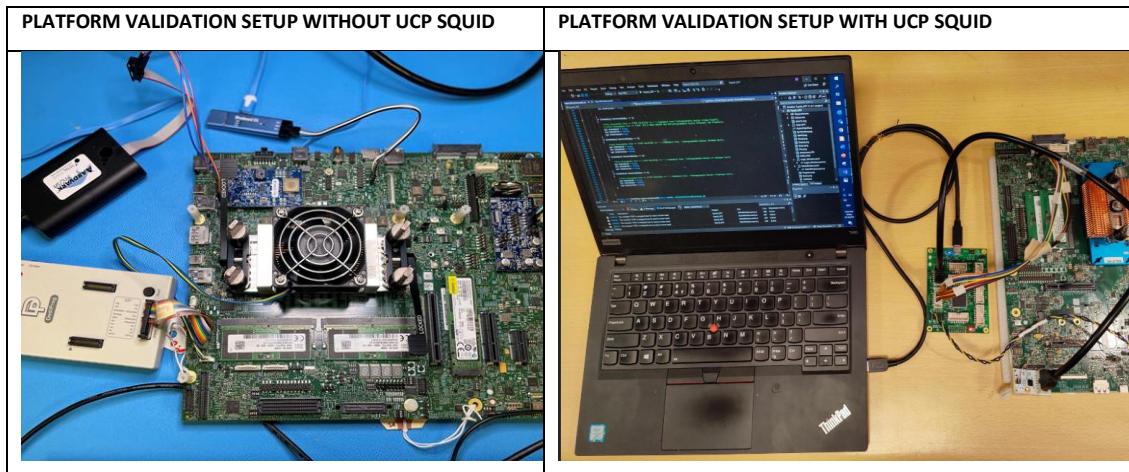


Figure 88 : SNAPSHOT OF UCP SQUID SETUP

32 RVP NEST

32.1 Introduction

RVP NEST is a remote access farm hosted and maintained by RVP Team. Goal of RVP NEST is to enable early access to platform for the RVP users. RVP NEST gives the in-lab user experience and allows to remotely control the RVP by logging-in through Host PC.

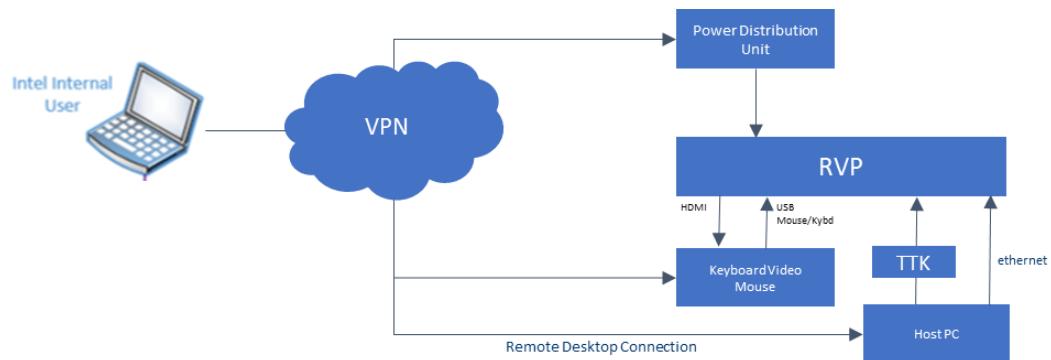


Figure 89 : RVP NEST Connection diagram

By default, each setup has dedicated host in which KVM, IFWI flashing tool (e.g. TTK3 or DAC or UCP), BIOS serial cable, G3 Cycling support through IP PDU connected to RVP. On need basis, we shall support

- Setups can be made fully loaded GC or DC configs
- ITP-XDP debug tools shall be connected
- Flexible to any OS (Ubuntu/Centos/SVOS) on SUT
- Peripherals/3PE shall be connected
- Debug Acceleration Card (DAC) can be connected to platform, UCP, CBS
- Support post PRQ
- Optional/Feature Reworks will be supported

For more details on the RVP Nest User Guide, please visit the below wiki link:

<https://goto.intel.com/rvpnestwiki>