



# PTL-UH RVP Hardware Architecture Specification

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***Revision 1.1***

***December 2024***

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## Revision History

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Revision Number	Description	Date
0.5	Initial document for review	May, 2023
0.7	RVP HAS updated based on feedback received from RVP LZ Rev0p7, PRD and stakeholder feedback.	August, 2023
1.0	Updated the design document based on RVP LZ Rev1p0	February, 2024
1.1	Updated the HAS based on RVP LZ Rev1p2 and CCB in RVP2 to intercept LPCAMM E1 spec and DP2.1 MUX between GPU (iGfx/dGfx) and Barlow Ridge	December, 2024

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## Reference Documents/ Links

- i. PTL-UH RVP PDT SharePoint [link](#)
- ii. PTL-UH Platform Architecture [link](#)
- iii. PTL platform SAS documents [link](#)
- iv. USB-C PD Add-In-Card, USBC PD Add-In-Card Specification Rev1\_1\_r2.docx, [link](#)
- v. Type-C USB Switching AIC - Cswitch Rev4.0, [link](#) and Cswitch 2.0 [link](#)
- vi. PTL Platform CCB link (TBD)

## Document Conventions

The terms PTL-UH, processor and SoC are used interchangeably in the document.

Small letter ‘b’ stands for bits, e.g. Mbps stands for Megabits per second. Capital letter ‘B’ stands for Bytes, e.g. MB stands for Megabytes.

All binary numbers will have a suffix ‘b’ at the end of the number, e.g. 00110b. Hexadecimal numbers will be mentioned with a prefix ‘0x’, e.g. 0x11FD. Decimal numbers will not have any suffix or prefix.

Capital letter ‘HDR’ stands for Header in the figures.

Items mentioned as **TBD** are open and yet to be closed from the design perspective.

## Acronyms

Acronym	Description
PTL	Panther Lake
MTL	Meteor Lake
ARL	Arrow Lake
ADL	Alder Lake
AIC	Add-In Card
ALS	Active Level Shifter
BOM	Bill of Material
BP	Back Panel
BSSB	Boundary Scan Sideband
CC	Configuration channel
CRLS	Cost Reduced Level Shifter
DCI-OOB	Direct Connect Interface Out of Band
DDR	Double Data Rate
DnX	Download and execute
DP	Display port
DPC	DIMMs Per Channel
EC	Embedded controller
FP	Front Panel
GND	Ground return
HDMI	High-Definition Multimedia Interface
I3C	Improved Inter Integrated Circuit also known as Sense Wire
IIC or I2C	Inter-Integrated Circuit
KoZ	Keep-out Zone

LSPCON	Level Shifter Protocol Converter
MR	Maple Ridge
NOA	Node Observation Architecture
PCH	Platform Controller Hub
PD	Power Delivery
PD	Power Down
POR	Plan of record
PSS	Processor Secured Storage
RVP	Reference Validation Platform
SBU	Sideband use
SKU	Stock Keeping Unit
SML/SMB	System management link/Bus
SODIMM	Single Outline Dual Inline Memory Module
SPI	Serial Peripheral Interface
TBT	Thunderbolt
TCPC	Type-C port controller
TCPs	Type-C ports
TCSS	Type-C sub system
THC	Touch Host Controller
UFP / DFP	Upstream/Downstream Facing Port
USB	Universal Serial Bus
VBUS	Bus power
VISA	Visualization of Internal Signals Architecture
WIP	Work In Progress
XDP	eXtended Debug Port

# 1 Introduction

---

The scope of this document is to cover the overall functional architecture for the PTL-UH RVPs including the debug and validation hooks. The document would describe the architecture and feature set of PTL-UH RVP's and the design in detail.

## 1.1 Design Team

The Key contacts for PTL-UH RVP are given in Table 1 below.

**Table 1: Key Contacts for PTL-U/H RVP design**

Role	Point of Contact
<b>RVP Program Manager, Systems PDT, Boards &amp; Kits</b>	Mani, Suresh; Korishettar, Aishwarya
<b>RVP Engineering Manager</b>	Agrawal, Archana
<b>RVP Architect</b>	N, Anilkumar Srighakollapu, N V S Kumar (PD Architect)
<b>RVP Design Lead</b>	Ismail Sherif, Khader Shareef
<b>RVP Design Engineers</b>	C M, Aparna Dixit, Mayank George, Priyan Jadhav, Aniket K, Vishnu M K, Muhammed Naseef Prabha, Abhijith Rao, Archana Sahu, Shubham Kumar Usha Vidaya, Divya
<b>RVP Power Delivery Lead</b>	P, Manas
<b>RVP PCB Layout Lead</b>	V, Singaravelan J, Diana Kumari Selvaraj, Balaji Elayaraj, David
<b>Mechanical Team</b>	Kadadevaramath, Akarsha
<b>Validation Lead &amp; CSF</b>	V, Manjunatha Jha, Nisha Kumari (Chrome)

## 1.2

### RVP design SKUs

The PTL-UH will have the SKUs as listed in Table 2. There will not be a different PI / PnP Board SKUs rather all the boards will have same implementation from PI / PnP perspective. All RVP boards will have PnP HDR place holders; however, only PnP BOM SKU RVPs will be stuffed with 2x7 HDRs.

There would be other design options provided on each board which are explained in the respective interface functional specification section of the document.

**Table 2: PTL-UH RVP Design SKUs**

PTL-UH RVP SKU List (with SKW - SKU Key Word)							Board SKU Is TO SKU	
Compute Die: Intel 18A (1278.3) ; PCD-P (UP) & PCD-H : N6 ; Gfx PiXe3 64EU (UH); P1276.4 ; Gfx PiXe3 192 EU (P) ; N3E	PTL-UH RVP Base SKU	Board SKU or BOM SKU	SKW	PTL-UH RVP SKU Name	Memory	PCB Type	Validation Config	Comments
PTL-UH LP5x T3	PTL-UH LP5x T3	Board SKU	UH-01	PTL-UH LP5x T3 Mem Skt	7400 1R/2R	T3 - 10+6 Layer	Golden Config	Memory Socketed, Limited to Memory validation teams, PO Vehicle
		BOM SKU	UH-02	PTL-UH LP5x T3 MemSD				Memory Soldered Down - 4x4GB (16GB), Volume SKU
		BOM SKU	UH-14	PTL-UH LP5x T3 MemSD 32GB EPS				Memory Soldered Down - 4x8GB (32GB)
		BOM SKU	UH-15	PTL-UH LP5x T3 MemSD MECC				Same as UH-02, but with MECC conn stuffed
		BOM SKU	UH-03	PTL-UH LP5x T3 MemSkt PnP				Memory Socketed, PnP SKU
		BOM SKU	UH-04a	PTL-UH LP5x T3 MemSkt Chrome				Chrome SKU, Memory Socketed - only for PrePO
		BOM SKU	UH-04	PTL-UH LP5x T3 MemSD Chrome				Memory Soldered Down, Chrome SKU, Plan for Mem Skt in PrePO
PTL-UH dTBTT3 LP5x CAMM	PTL-UH dTBTT3 LP5x CAMM	Board SKU	UH-05	PTL-UH LP5x CAMM dTBTT T3	7400 1R/2R (IPOR)	T3 - 10+6 8+10 Layer	Delta Config	dTBTT - Barlow Ridge with BOM for Internal Graphics on UHBR20 mode
		BOM SKU	UH-13	PTL-UH LP5x CAMM dTBTT T3 Ext Gfx				BOM SKU for external discrete Graphics on dTBTT
PTL-UH LP5x T4	PTL-UH LP5x T4	Board SKU	UH-06	PTL-UH LP5x T4 Mem Skt	8533 1R/2R & 9600	T4 2x2+, 10+6 Layer	Delta Config	Memory Socketed
		BOM SKU	UH-07	PTL-UH LP5x T4 MemSD				Memory Soldered Down - 4x8GB (32GB)
		BOM SKU	UH-08	PTL-UH LP5x T4 MemSkt PnP				Memory Socketed, PnP SKU and EVO SKU
		BOM SKU	UH-09a	PTL-UH LP5x T4 MemSkt PPV				PPV SKU for U & H 12Xe, Memory Socketed - only for PrePO
		BOM SKU	UH-09	PTL-UH LP5x T4 MemSD PPV				PPV SKU for U & H 12Xe
PTL-UH DDR5 T3	PTL-UH DDR5 T3	Board SKU	UH-10	PTL-UH DDR5 T3	SODIMM - 7200 1DPC	T3 - 8+6 8+10 Layer	Delta Config	Chrome SKU
		BOM SKU	UH-11	PTL-UH DDR5 T3 Chrome				PPV SKU for H 4Xe
		BOM SKU	UH-12	PTL-UH DDR5 T3 PPV				

## **2      Feature Set & HW-BOM**

---

### **2.1    RVP Landing Zone**

RVP landing zone can be viewed in SharePoint site for the PTL-UH RVP [here](#)

### **2.2    Platform HW BOM**

The platform HW BOM is being defined at this point and will be provided at the below HSD-ES links.

[PTL-U Platform HW BOM](#)

[PTL-H 12Xe Platform HW BOM](#)

[PTL-H 4Xe Platform HW BOM](#)

### **2.3    Platform Validation Configuration**

The platform validation configurations can be found in the below link.

PTL-UH Validation configuration [link](#)

3 General Architecture

### 3.1 Platform Block Diagram

The functional block diagram of the PTL-UH RVP system with all the interface routing and connectivity options are presented in Figure 1,

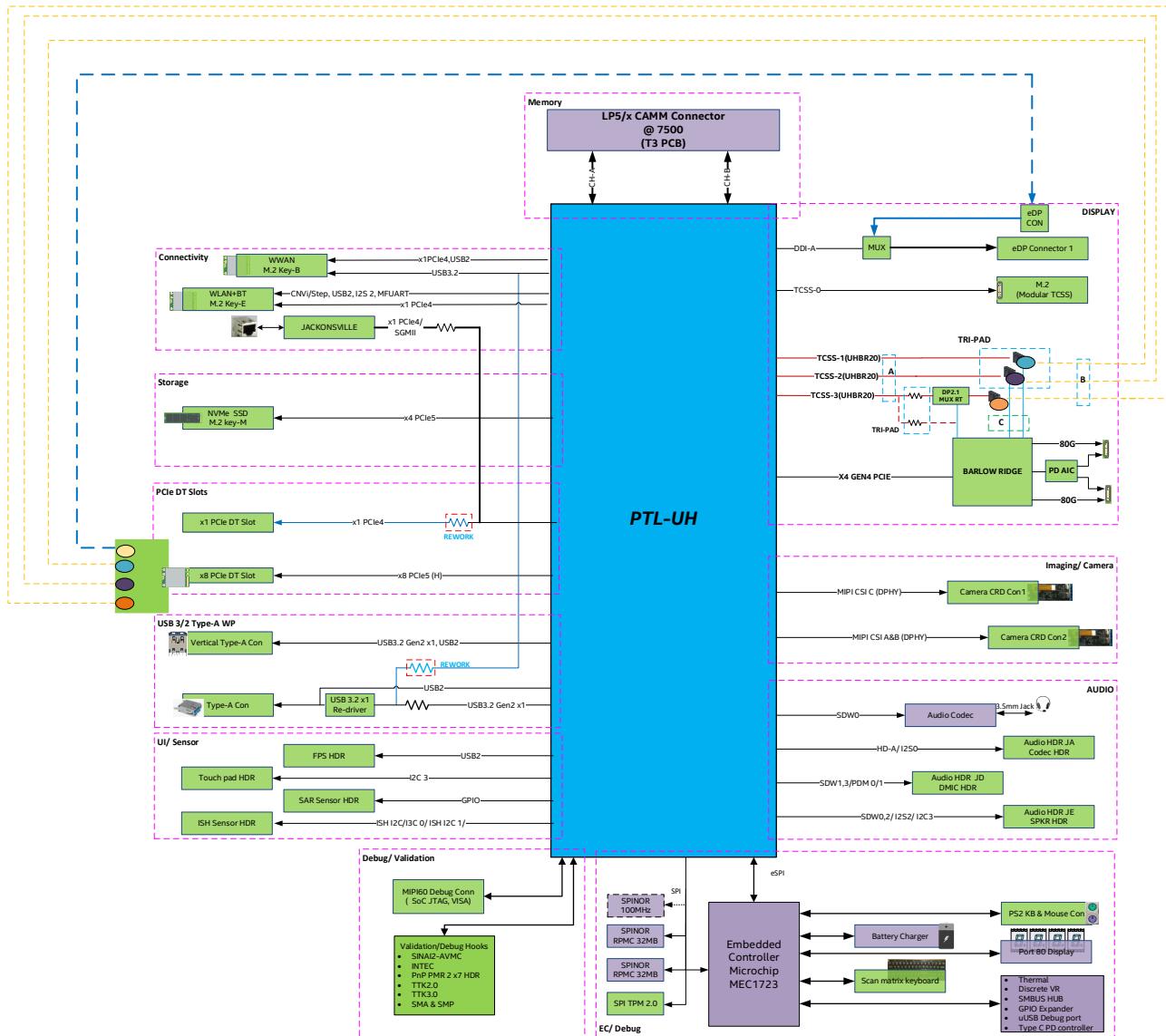


Figure 2, Figure 3 and Figure 4. All the major interface options are mentioned in the figure. The validation hooks are not illustrated in the figure but will be covered in the design. The details of the validation hooks provided are covered in the respective sections.

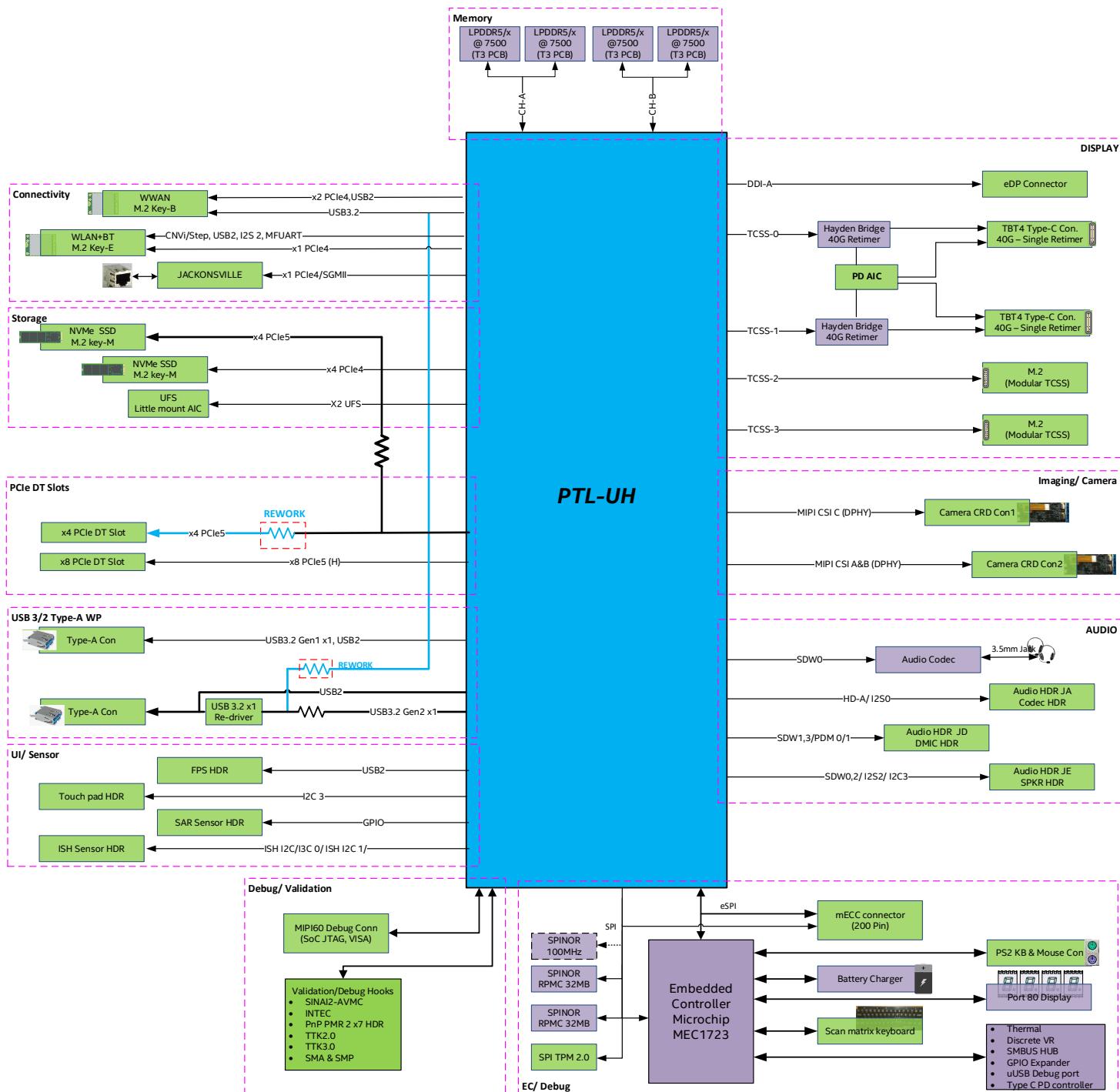


Figure 1: RVP1 PTL-UH T3 LP5x RVP Block Diagram

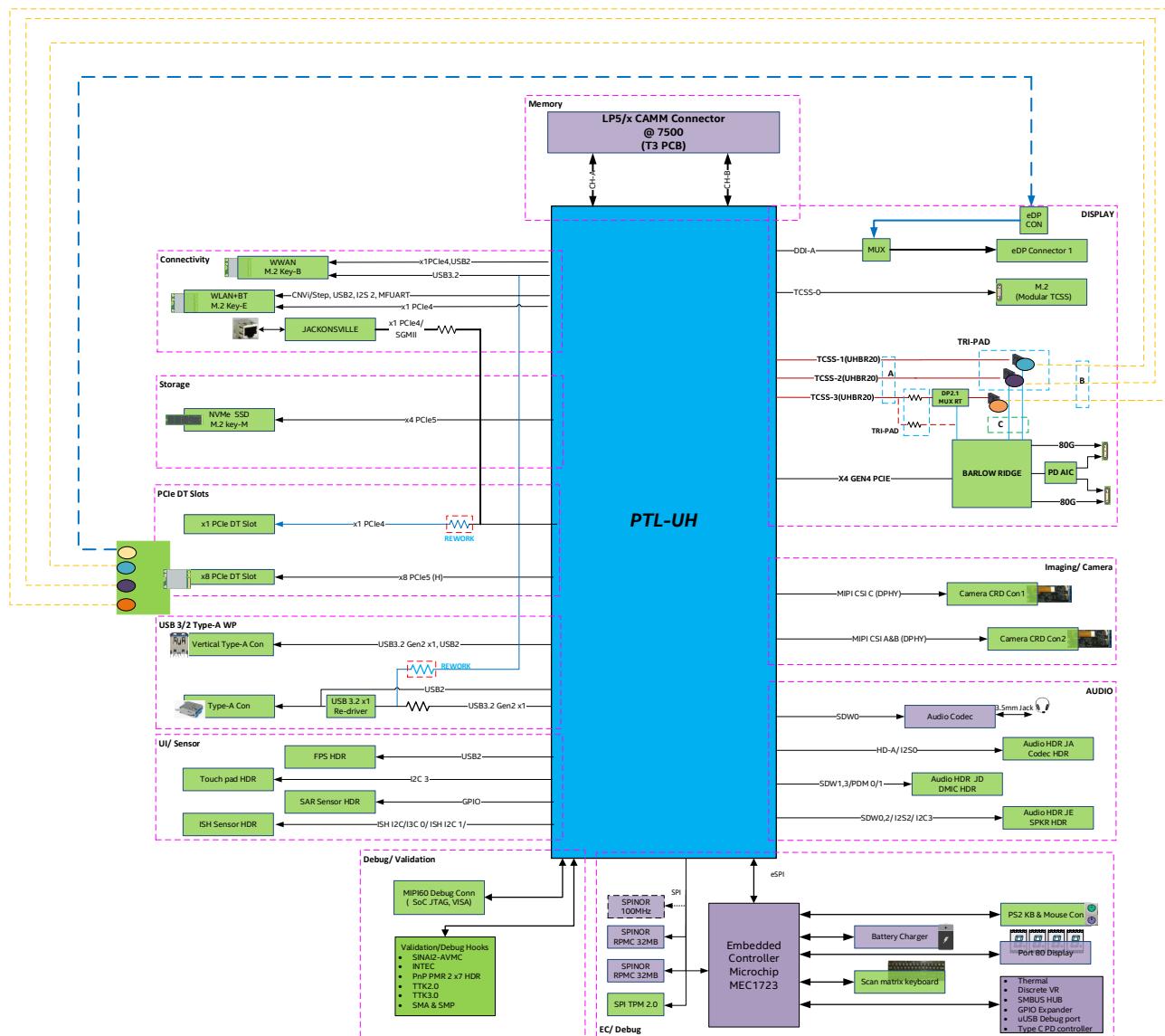


Figure 2: RVP2 PTL-UH T3 LP5x CAMM & dTBT RVP Block Diagram

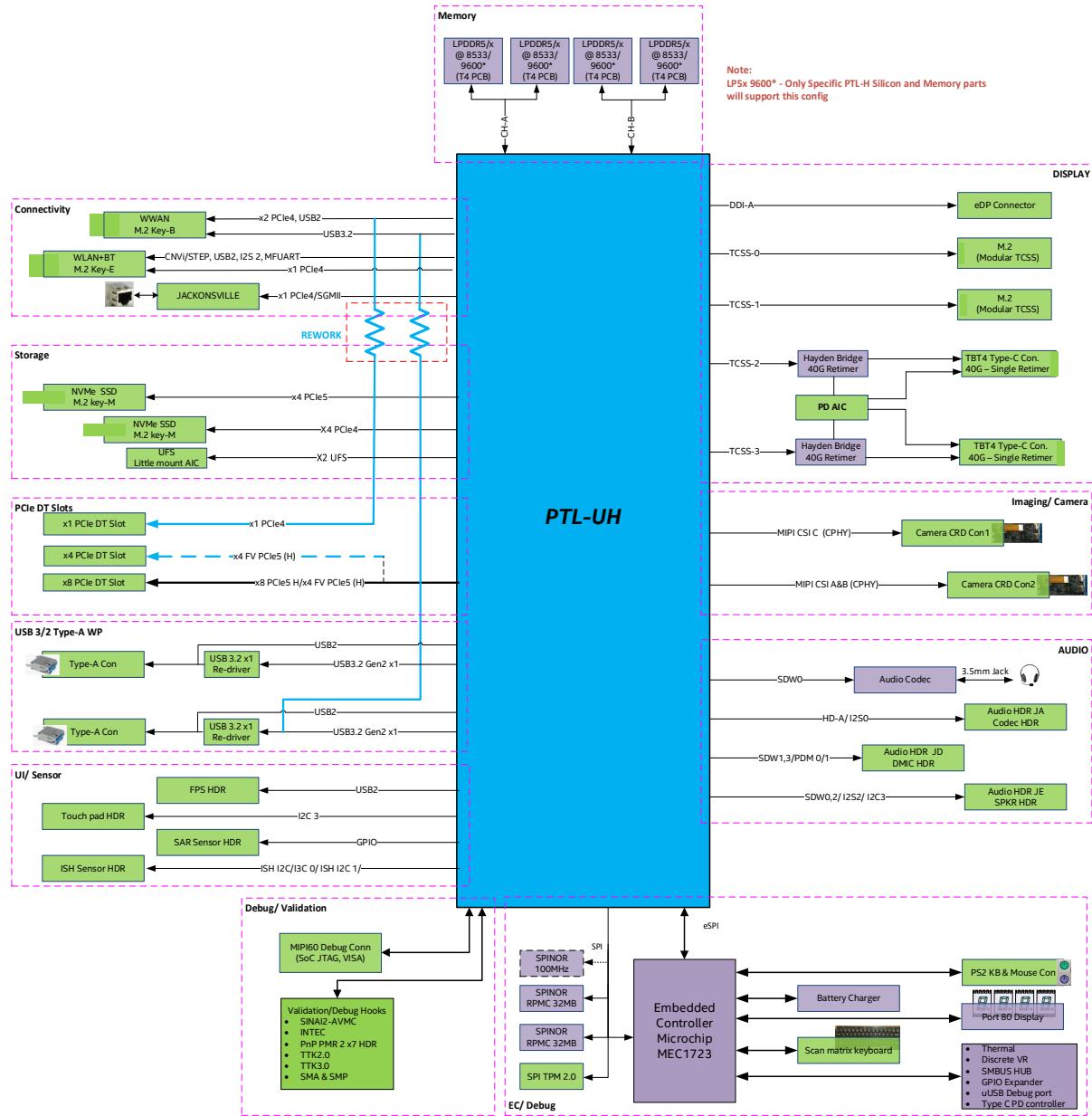


Figure 3: RVP3 PTL-UH T4 LP5x RVP Block Diagram

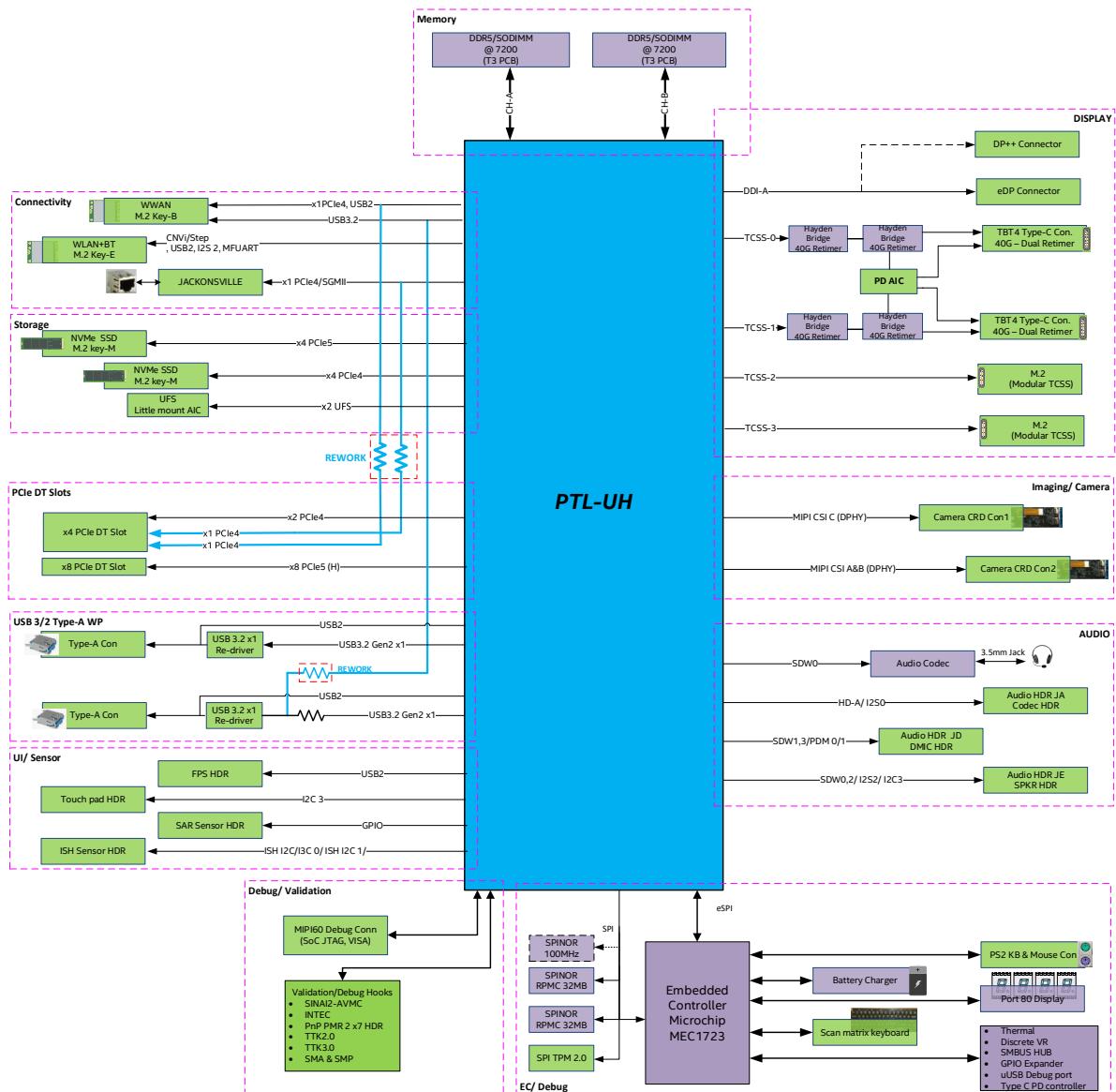


Figure 4: RVP4 PTL-UH DDR5 SODIMM RVP Block Diagram

### 3.2

## Panther Lake SoC overview

PTL-UH SoC is supporting die disaggregated strategy (Compute/Gfx/PCD). PCD stands for Peripheral Controller Die and it contains all the traditional client IPs. It does contain the Die to Die (D2D) links to connect to the other die to form the products.

PTL-UH have new core architecture (PCore: Cougar, ECore: Darkmount), new GFX XE3 Architecture, New VPU architecture and new efficient atom complex.

The new efficient atom complex consists of highly efficient Darkmont core that are off the ring, and they handle background task, so you don't have to wake up all the other higher power cores or more cores.

For more details, please refer [PTL SoC overview HAS](#) and [PTL Product Specification HAS](#)

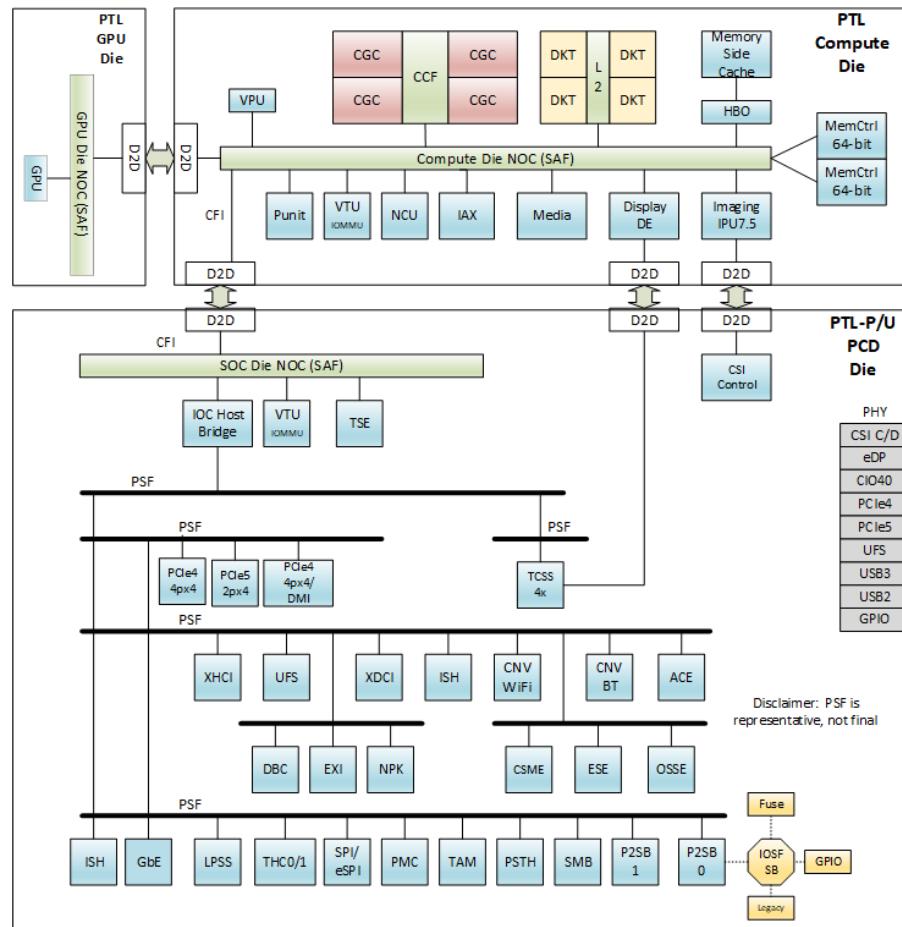


Figure 5 : PTL-UH SoC Block Diagram

### 3.3

## PTL-UH RVP platform SoC / Interface support overview

PTL-UH RVP supports PTL-H404, PTL-H 12Xe and PTL-H484 SoC socketed down on the board.

Table 3: PTL-UH RVP Supported CPU TDP Characteristics

Die Package	Product	TDP
PTL-H404 (PTL-U)	4+0+4+GT1	15W
PTL-H484 12Xe (PTL-P)	4+8+4+GT2	28W
PTL-H484 (PTL-H)	4+8+4+GT1	45W

The major platform interface supported on the PTL-UH RVP apart from debug, sideband and GPIO are listed below.

**Table 4: PTL-U/H SoC/ RVP platform interface support summary**

Interface	PTL-U/H RVP's
Memory	LP5x/LP5CAMM/DDR5 SODIMM
eDP/ DDI	1x4 eDP1.5b (DP++ support only on RVP4 DDR5 SKU through rework)
Concurrent Dual eDP Display	N/A (Optional with eDP/Type-C)
USB Type C	4 ports CIO40: USB4.0 + TBT4 + DP 2.1 + HDMI2.1
MIPI CSI	4 Total / 3 concurrent D-PHY 2.1 2.5Gbps
PCIe	12 total lanes in U; 20 total lanes in H x8 Gen5 (PEG IO – only in H) x4 Gen5 X8 Gen4
GbE (Muxed PCIe)	1x 1GbE Port (muxed with PCIe Gen4 port)
USB3.2 Gen2x1 10G	2 ports
UFS	1x2 UFS 3.1 Gear 4 ( <i>U Only, Not Supported in H</i> )
USB2	8 ports USB 2.0
CNV (WiFi / BT)	Scorpius, 2x2 Wi-Fi 7 R2, BT 6.x
SPI Interface	1 CSME SPI 2 THC SPI
Audio	1 HD-A 3 I2S 4 SoundWire 2 DMIC Interfaces
eSPI	eSPI with 4 chip select signals
LPSS	6 I2C Ports 2 I3C 2 GSPI/THC Ports 3 UART Ports
ISH	3 I2C Ports 1 SPI Bus 2 UART Ports 11 GPIOs
Thermal DIODE	PCH Thermal Diode
MLINK	1 Channel with CLK, DATA & RST
Integrated Clock Controller (ICC)	7 CLKREQ / CLKOUT [0:6] for CCG'S U/P/H 2 CLKREQ / CLKOUT [7:8] for CCG'S H only
SMBUS / SMLINK	2 SMLINK 1 SMBUS

### 3.4

### Form Factor

The PTL-UH RVP will follow a 9inch x 11inch form factor. Please refer to the Mechanical chapter for more details.

#### Generic Implementation Notes

- GND vias are spread across the board on both top and bottom sides, with clear marking on silk screen will be provided.
- All the socket caps will be specified in the schematics and can be removed in the customer version of the schematics or board.
- RVP design will follow the PDG for routing of all traces.
- All the LED will be placed on the TOP side and will be visible.

---

*Note: Text highlighted in yellow color will be updated in subsequent versions of this RVP HAS document*

---

## 4 Main Memory

---

### 4.1 Memory Controller

The PTL U/H memory subsystem supports DDR5/LPDDR5/LPDDR5x memory technologies. RVP SKU memory configuration support would be as follows.

**Table 5: Memory Support for various RVPs**

RVP SKU #	Config	Internal POR Transfer Rate (MT/s)	External POR Transfer Rate (MT/s)	Memory Device	Routing Topology	Supported Memory density		PCB Stack-Up / Routing Layer
						Min	Max	
RVP1 T3	LPDDR5/x Memory Down x32 315 BGA	2R 8533	2R 7467	DDP QDP ODP	Point to Point	16GB	64GB	T3/10L 3 Layers;
RVP2 T3	LPDDR5x CAMM2	2R 8533	2R 7467 (PTL H) 2R 6800 (PTL U)	LPCAMM2	Point to Point	16GB	64GB	T3/10L 2 Layers.
RVP3 T4	LPDDR5x Memory Down x32 315 BGA	2R 9600	2R 8533	DDP QDP ODP	Point to Point	16GB	64GB	T4/10L 4 Layers;
RVP4 T3	DDR5 SODIMM 1DPC	2R 7200	2R 7200	CSODIMM /SODIMM	B2B	16GB	96GB (24Gb, 2R x8) 128GB (32Gb, 2R x8)	T3/8L 3 Layers;

### 4.2 Memory Device BOM options

The following tables provide the Manufacturer Part number supported on PTL U/H. The below table is based on initial HAS release. Contact MIO Team for the latest memory parts validated on the platform.

Refer the below table for the initial memory parts considered for each SKUs. Please find the complete memory IPNs in this link: [MEMORY PART NUMBERS](#).

**Table 6: Preferred Part List - Memory**

Memory Type	Package	Manufacturer Part Number (Intel Part Number)	Speed (MT/s)	Module/DRAM density	Memory Config	Mfg
LPDDR5x	DDP 315b	H58G56BK8BX068	8533	4GB	1R x16 2ch	SK Hynix
LPDDR5x	DDP 315b	H58G56BK7BX068	7467	4GB	1R x16 2ch	SK Hynix
DDR5 SODIMM 262	CSODIMM 262	MTC4C10163S1SC	7200	8GB	1R x16	Micron
LPDDR5 CAMM	LPCAMM2	MTD8C10324N2FN026CY	7467	16GB	1Rx16	Micron

#### 4.3

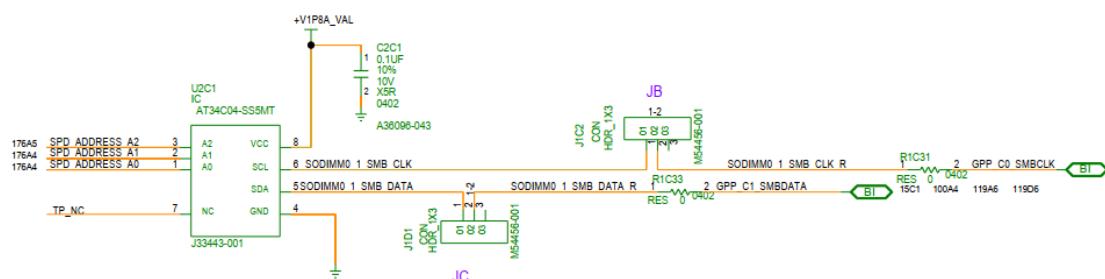
#### Memory SPD

Memory SPD [Serial presence detect] is a standardized way to automatically access information about a memory module or device. Refer Link of SPD Repository [SPD\\_Files - BIOS Group BKM - Intel Enterprise Wiki](#).

**Table 7: Memory SPD info**

RVP SKU #	Config	SPD
RVP1 T3	LPDDR5x Memory Down	BIOS Hard Coded/ SPD EEPROM ON RVP
RVP2 T3	LPDDR5x CAMM2	On the Module
RVP3 T4	LPDDR5x Memory Down	BIOS Hard Coded/ SPD EEPROM ON RVP
RVP4 T3	DDR5 CSODIMM, 1DIMM/Channel	On the Module

Example Schematics Snapshot for SPD EEPROM;

**Figure 6 : SPD EEPROM for LP5x MD Designs**

SPD present signal will be given on DIP switch instead on jumper for customer's convenience. The Level translator is optionally given in case VIL issue observed with SMBUS when interfacing with SPD EEPROM.

## 4.4

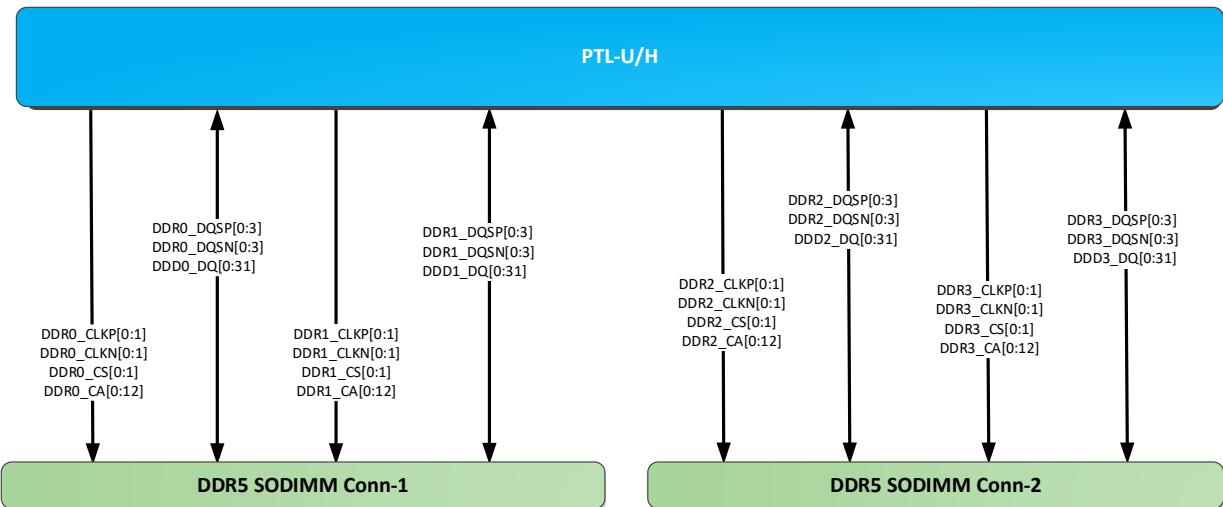
### Routing Topology

This section deals with the routing topology to be adopted for DRAM routing on PTL U/H RVP boards.

#### 4.4.1

##### Topology for DDR5

DDR5 SODIMM routing on PTL U/H will be point-to-point routing for all the DDR5 signals. DDR5 SODIMM RVP will be placed B2B (back-to-back). Two standard (8H & 4H) will be placed in a stacked format on RVP.



**Figure 7 : Memory DDR5 SODIMM Down Routing Topology for RVP**

##### Bit/Byte Swapping Rule:

- Bit swapping is allowed within each Byte for all memory technologies.
- DDR5: Byte Swapping is allowed within each x32 channel.
- ECC bits swap is allowed within ECC byte / nibble: DDR5 ECC [3..0].

#### 4.4.1.1

##### CSODIMM

Clocked SODIMMs are used for modules with target frequency more than 6400MT/s. RVP will be supporting CSODIMM and the traditional SODIMMs as well. Major differences for CSODIMM will be number of clock lines running from controller to DIMM will be reduced to one from four. There will be buffer chip in the CSODIMM module which will condition and buffer to DRAM chips. This helps to improve the jitter requirements and allowing to run the interface at higher speeds

comparing to traditional SODIMM. There won't be any hardware changes required to switch between CSODIMM to SODIMM.

#### 4.4.2 Topology for LPDDR5x MD Down

The Address & command signals are routed with point-to-point topology with Data and Strobe signals in LP5x topology. This x32 device is common for T3 and T4 RVPs, illustrated in the figures below.

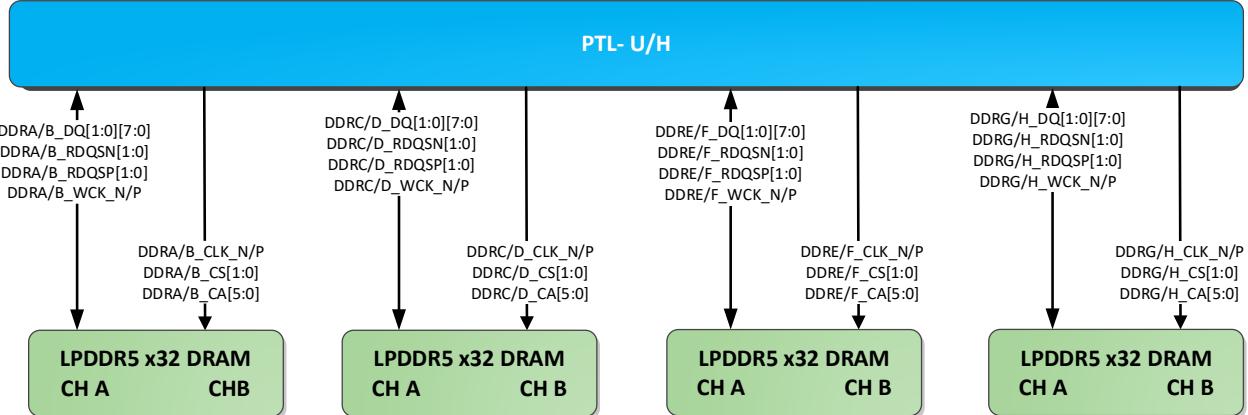


Figure 8 : Memory LP5x Device Down Routing Topology for RVP

#### Bit/Byte Swapping Rule:

- Bit swapping is allowed within each Byte for all memory technologies.
- Byte swapping is allowed within a 16-bit channel.
- LPDDR5: x16 sub-channels can be swizzled within their x64 MC.
- When swapping channel DQ, the CA/CS signals must be swapped as well.

#### 4.4.3 Topology for LPDDR5x CAMM2

The Address & command signals are routed with point-to-point topology with Data and Strobe signals for LPCAMM2. **PTL UH RVP** will be supporting both E0 and **E1 memory modules**. Additional VDDQ power rail and VDDQ\_DISABLE signal terminated to memory connector footprint to support later E1 modules. This is backward compatible with E0 modules.

Note: Additional 2 rows of pins added to LPCAMM2 footprint without shielding pins for the E1 module support.

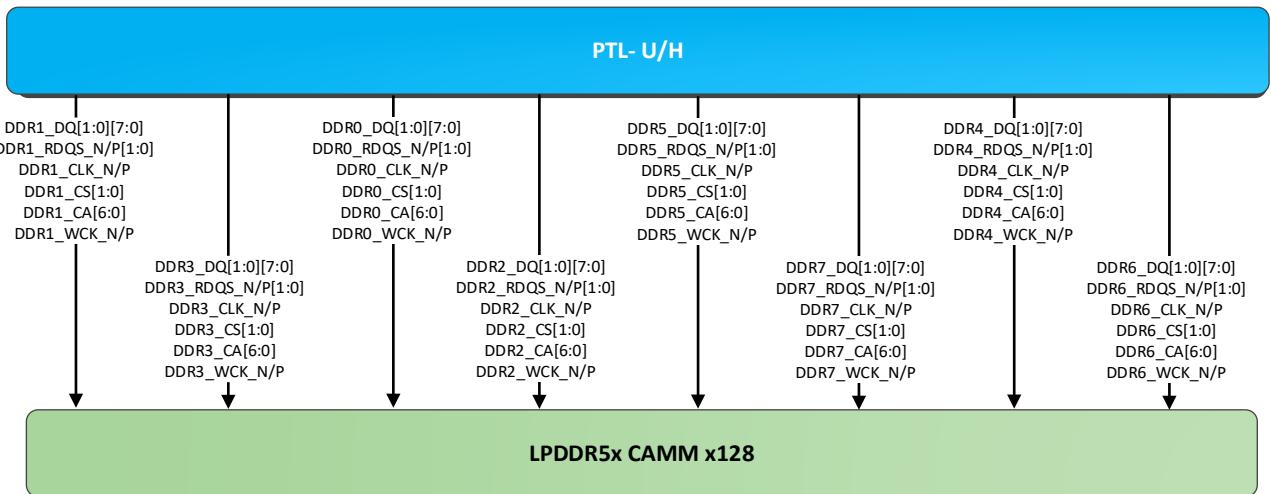


Figure 9 : Memory LPCAMM Routing Topology for RVP

#### Bit/Byte Swapping Rule:

- Bit swapping is allowed within each Byte for all memory technologies.
- Byte swapping is allowed within a 16-bit channel.
- LPDDR5: x16 sub-channels can be swizzled within their x64 MC.
- When swapping channel DQ, the CA/CS signals must be swapped as well.

## 5 Display

PTL supports two types of Display PHYs. The embedded display eDP C10 PHY and the secondary internal display panel will be over TCPO Type-C/eDP/DP Alt/HDMI C20 PHY. There is 1 dedicated EDP port and 4 Type-C ports on PCD-U/H. One of the Type-C (port-0) will support EDP-over-TypeC. The C20 PHY supports various external display connections. It supports DP2.1 (1, 2, or 4 lanes up to 20Gbps with Adaptive Sync), HDMI 2.1. One of the Type-C port will be a combo port, capable of the legacy Display-over-TypeC and the new eDP-over-TypeC. No native HDMI support in PTL-UH platform.

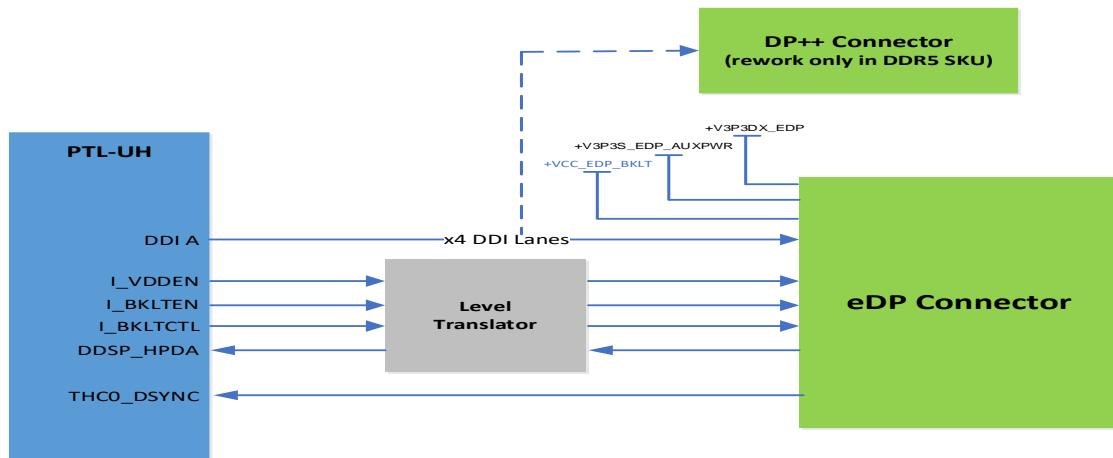
### 5.1 Display Topology

#### 5.1.1 PTL-U/H RVP Display Topology

Refer to below table and block diagrams for PTL-U/H RVP's eDP/DDI display port configuration.

**Table 8 : PTL-U/H RVP's eDP/ DDI port display configuration**

Silicon Interface	RVP 1: PTL U/H LP5 T3 RVP	RVP 2: PTL U/H – T3 LP5 CAMM RVP	RVP 3: PTL U/H – LP5 T4	RVP4: PTL U/H – DDR5 SODIMM
DDI-A	eDP Panel Conn	eDP Panel Conn (MUX with DG eDP)	eDP Panel conn	eDP Panel Conn (default) DP++ (rework)



**Figure 10 : PTL U/H – All SKUs except RVP2 dTBT Barlow LP5 CAMM block diagram**

PTL-U/H RVP2 SKU supports muxed display feature through eDP MUX provided on RVP. RVP supports DIODES INCORP's PI3WVR13612ZLEX (N34750-001) MUX on the RVP board itself.

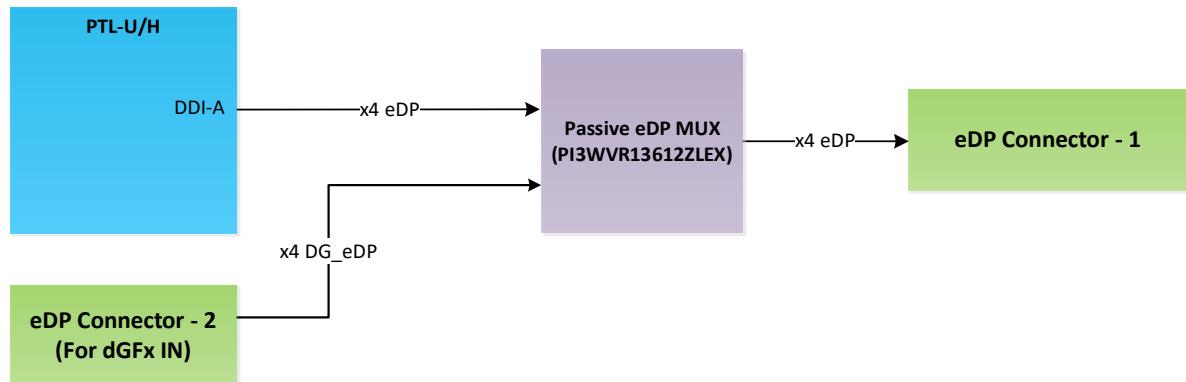


Figure 11 : PTL U/H – RVP2 dTBT Barlow – LP5 CAMM block diagram

### 5.1.2

### OLED Panel Support

OLED panels are supported using OLED PMIC AIC to provide the required power changes. A cable from eDP 60-pin connector on RVP to be connected to OLED PMIC AIC. The output from that AIC will be connected to the OLED panel using another eDP 60-pin cable.

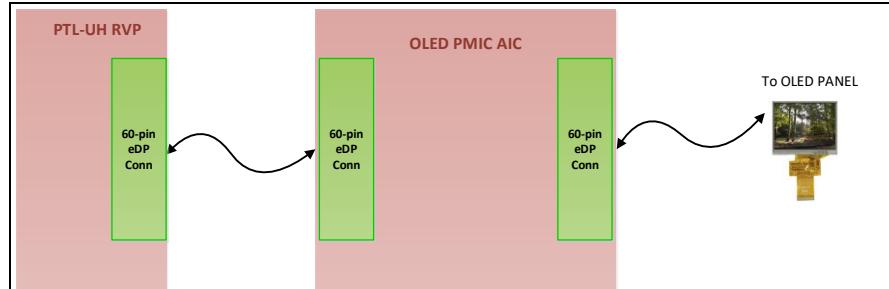


Figure 12 : OLED PMIC AIC support

## 5.2

### Display Topology from TCSS ports

Type-C PHY on PTL-U/H supports DP, HDMI, and TBT displays. Type-C PHY can be used as alternate mode for DP on a physical Type-C port or can be used as a dedicated eDP or HDMI port with an eDP or HDMI native connector. Refer to Type-C & Thunderbolt section for more details on the same.

Please refer to the Type-C section for the TCSS port mapping and block diagram for the various display topologies supported from TCSS ports.

## 5.3

### 3<sup>rd</sup> Party display re-timer/ re-driver support details

Below table shows the 3<sup>rd</sup> party display re-timer/ re-driver device support list in PTL-U/H RVP's.

**Table 9: Display 3<sup>rd</sup> party devices support list**

Device Name	MPN
HDMI 2.1 Linear Redriver (Used on TCSS module, not on RVP)	PS8219QFN46GTR-B0
HDMI 2.1 Retimer (Used on TCSS module, not on RVP)	PS8419QFN46GTR-A1
USB 3.2 Gen2 x1 Re-driver	PI3EQX1002E2

## 5.4

### DG Support

PTL-U/H RVP will be supporting 3<sup>rd</sup> party graphics card from Nvidia or AMD, and the Intel DG MRB AIC is not PoR.

#### 5.4.1

#### 3<sup>rd</sup> party Graphics card support on x8 PCIe slot

PTL-U/H RVP supports the CLKREQ muxing between pins B12 and B17 of the PCIe slots to enable the L1 sub-state for low power modes of the 3<sup>rd</sup> party PCIe AICs. The default routing of CLKREQ on PCIe 8 lane slot will be to pin B12 of the PCIe slot with a switch option provided on the board to change the connection to pin B17 of the slot.

Additional pins supported for external GFx cards are listed below.

**Table 10: Sideband signals for external GFx card support**

Pin	Signal Name	Description	I/O (PCIe slot)	Polarity (Default)
A19	DGPU_PWR_EN#	Used to control power enable for GPU. Set to 0 by default. <b>Option provided for having both logic low and logic high for this A19 pin through switch.</b>	I	Low
B30	DGPU_SEL	Used in conjunction with GPU_PWR_EN# to control power state transitions in GPU; 0 = dGPU select. 1 = dGPU deselect. B30 is an input at the PCIe slot and is Active Low.	I	LOW
B12	DGPU_CLK_REQ#	Allows dynamic control on CLKREQ to hit power saving features on new designs.	O	LOW
A11	DGPU_RST#	Discrete GFx Enable signal. Controlled by Switchable Graphics Driver and driven by PCH GPIO. Used to gate with Platform Reset to enable the Reset for dGPU. 0 = Keep dGPU in reset; 1 = Reset is released. This action taken 100ms after DGPU_PWROK to ensure clock is stable.	I	LOW

## 5.4.2

**3<sup>rd</sup> party Graphics card support on x4 PCIe slot limitations:**

- Double width dGFX card not supported, due to KOZ issues. But single width half size and full-size card supported.

## 5.4.3

**PCIe CEM connector pinout (DG)**

PTL-U/H RVP supports the x8 lane PCIe slot for 3<sup>rd</sup> party GFx cards with below pinout:

**Table 11: DG AIC connector pinout**

PEG pin	Pin Functionality	PEG Pin	Pin Functionality
B1	+V12S_PEG_SLOT	A1	PEG_SLOT_PRSNT1_N
B2	+V12S_PEG_SLOT	A2	+V12S_PEG_SLOT
B3	+V12S_PEG_SLOT	A3	+V12S_PEG_SLOT
B4	GND	A4	GND
B5	SMB_CLK_PEG_SLOT	A5	TP
B6	SMB_DATA_PEG_SLOT	A6	TP
B7	GND	A7	TP
B8	V3P3S_PEG_SLOT	A8	TP
B9	TP	A9	+V3P3S_PEG_SLOT
B10	+V3P3A_PCIEAUX	A10	+V3P3S_PEG_SLOT
B11	PEG_SLOT_WAKE_R_N	A11	PEG_SLOT1_RST_N
B12	CLKREQ#	A12	GND
B13	GND	A13	CLK_SRC_PEG_SLOT_DP
B14	EXP_A_TX_0_C_DP	A14	CLK_SRC_PEG_SLOT_DN
B15	EXP_A_TX_0_C_DN	A15	GND
B16	GND	A16	EXP_A_RX_0_DP
B17	DGPU_PRSNT#	A17	EXP_A_RX_0_DN
B18	GND	A18	GND
B19	EXP_A_TX_1_C_DP	A19	RTD3_COLD_OFF
B20	EXP_A_TX_1_C_DN	A20	GND
B21	GND	A21	EXP_A_RX_1_DP
B22	GND	A22	EXP_A_RX_1_DN
B23	EXP_A_TX_2_C_DP	A23	GND
B24	EXP_A_TX_2_C_DN	A24	GND
B25	GND	A25	EXP_A_RX_2_DP
B26	GND	A26	EXP_A_RX_2_DN
B27	EXP_A_TX_3_C_DP	A27	GND
B28	EXP_A_TX_3_C_DN	A28	GND
B29	GND	A29	EXP_A_RX_3_DP
B30	PROCHOT# (or) PEG_SLOT_DGPU_SEL_N	A30	EXP_A_RX_3_DN
B31	PEG_SLOT_PRSNT2_N	A31	GND
B32	GND	A32	PEG_SLOT_DGPU_PWR_OK

B33	EXP_A_TX_4_C_DP	A33	TP
B34	EXP_A_TX_4_C_DN	A34	GND
B35	GND	A35	EXP_A_RX_4_DP
B36	GND	A36	EXP_A_RX_4_DN
B37	EXP_A_TX_5_C_DP	A37	GND
B38	EXP_A_TX_5_C_DN	A38	GND
B39	GND	A39	EXP_A_RX_5_DP
B40	GND	A40	EXP_A_RX_5_DN
B41	EXP_A_TX_6_C_DP	A41	GND
B42	EXP_A_TX_6_C_DN	A42	GND
B43	GND	A43	EXP_A_RX_6_DP
B44	GND	A44	EXP_A_RX_6_DN
B45	EXP_A_TX_7_C_DP	A45	GND
B46	EXP_A_TX_7_C_DN	A46	GND
B47	GND	A47	EXP_A_RX_7_DP
B48	PEG_SLOT_PRSNT2_N	A48	EXP_A_RX_7_DN
B49	GND	A49	GND

## 6 Type-C & Thunderbolt

PTL-U/H supports integrated Type-C ports, supporting DP2.1, USB3.2, TBT3, TBT4 and USB4 protocols. The following figure shows functional block diagram of the Type-C ports on the PTL-U/H SoC. The block diagram is a super set implementation of RVP SKUs.

### 6.1 PTL-U/H RVP TCSS port configuration details

Refer to below table and block diagrams for the PTL-U/H RVP's TCSS Type-C and display port configuration.

Table 12 : PTL-U/H RVP's TCSS Type-C and display port configuration

Silicon Interface	Platform config requirement (all inputs)	RVP1: PTL U/H - T3PCB - LP5 MD	RVP2: PTL U/H – T3PCB - dTBT Barlow – LP5 CAMM	RVP3: PTL-U/H - T4PCB - LP5 MD	RVP4: PTL U/H - T3 PCB - DDR5 SODIMM
TCP0	1.Type-C TBT 40G with Single Re-timer (4 no's) 2.Type-C TBT 20G with Single Re-timer longer PDG length (1 no's) 3.Type-C TBT 40G with Dual Re-timer 4.Type-C with DP 1.4b +USB 3.2 Gen2 x2 20G Re-timer less 5.Cable topology TBT40G 6.Cable topology TBT20G 7.Cable topology DP1.4a / USB 3.2 Gen2 x2 20G Re-timer less 8.Type-A USB3.2 Gen2 x1 10G 9.Type-A USB3.2 Gen2 x1 10G with re driver 10.Native DP connector DP1.4a 11.Native HDMI 2.1 12 Gbps with linear re-driver 12.Native HDMI 2.1 10 Gbps with CRLS 13. Native HDMI 2.1 8 Gbps with CRLS 14.I3C debug port mux needed in one port 15.EV min, max, typical - length needed per topology at least one port in any board. 16. dTBT BR - Native DP 2.1 UHBR 20 retimerless FFC cable 17. M.2 modular TCSS AIC (TBT type-C / eDP / HDMI / USB type-A) 18. dTBT BR MD – Native DP 2.1 UHBR20 vertical DP connector <b>Topologies Zbb'ed</b> <b>1. Type-C TBT 40G with Re-driver + Re-timer</b> <b>2.1x Type-C with DP UHBR10+USB 3.2 Gen2 x2 20G Re-timer less</b> <b>3.1x Type-C with DP UHBR10+USB 3.2 Gen2 x2 20G with re-driver</b> <b>4. Native HDMI 5.94 Gbps with ALS</b> <b>5.Cable topology DP UHBR10/ USB 3.2 Gen2 x2 20G Re-timer less/ with re-driver</b> <b>4.Native DP connector UHBR10</b> <b>5.Native DP connector UHBR10 with re-driver</b>	Type C Con - TBT 40G Single Re-Timer	M.2 Modular TCSS: <b>USB-C</b> Retimer Module	M.2 Modular TCSS: <b>USB-C</b> Retimer Module	Type C Con - TBT 40G Dual Re-Timer
TCP1		Type C Con - TBT 40G Single Re-Timer	dTBT BR MD – Native DP 2.1 UHBR20 mDP connector	M.2 Modular TCSS: <b>HDMI</b> Redriver Module	Type C Con - TBT 40G Dual Re-Timer
TCP2		M.2 Modular TCSS: <b>USB-C</b> Retimer Module	dTBT BR MD – Native DP 2.1 UHBR20 mDP connector	Type C Con - TBT 40G Single Re-Timer	M.2 Modular TCSS: <b>USB-C</b> Retimer Module
TCP3		M.2 Modular TCSS: <b>HDMI</b> Redriver Module	dTBT BR MD – Native DP 2.1 UHBR20 mDP connector <b>(DP2.1 retimer supported)</b>	Type C Con - TBT 40G Single Re-Timer	M.2 Modular TCSS: <b>HDMI</b> Redriver Module

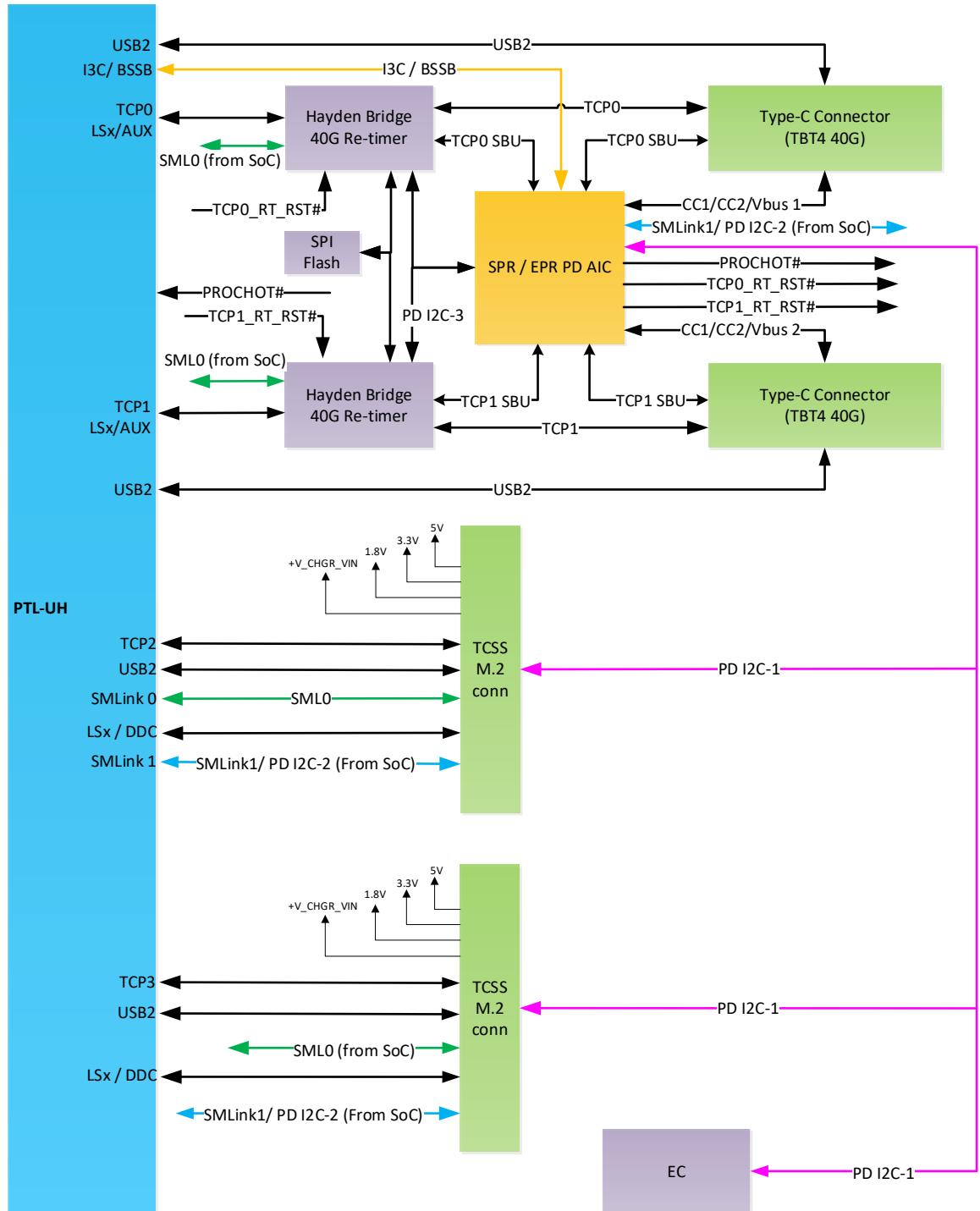
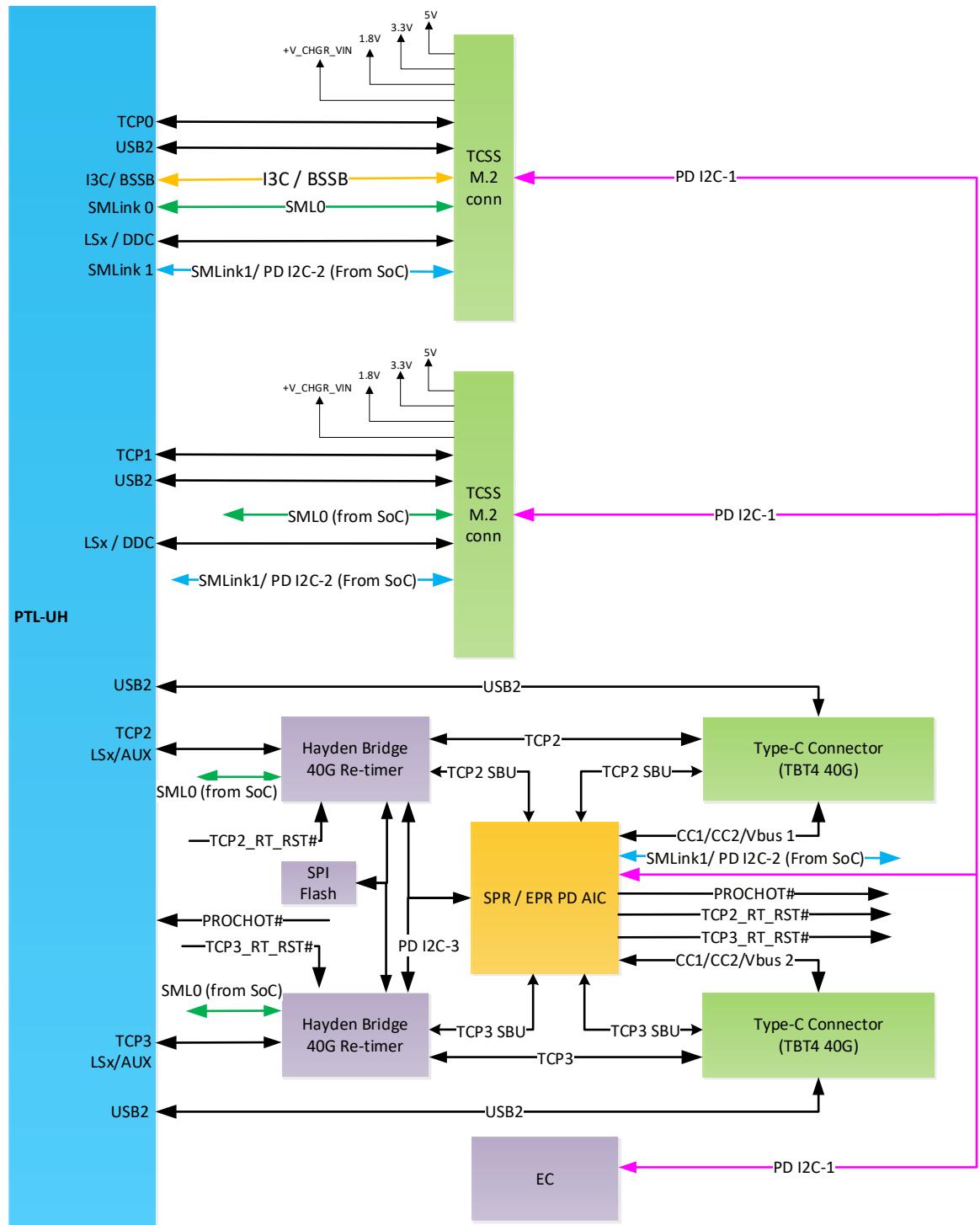


Figure 13: PTL-UH T3 LP5x RVP TCSS and display high level block diagram.



**Figure 14: PTL-UH T4 LP5x RVP TCSS and display high level block diagram**

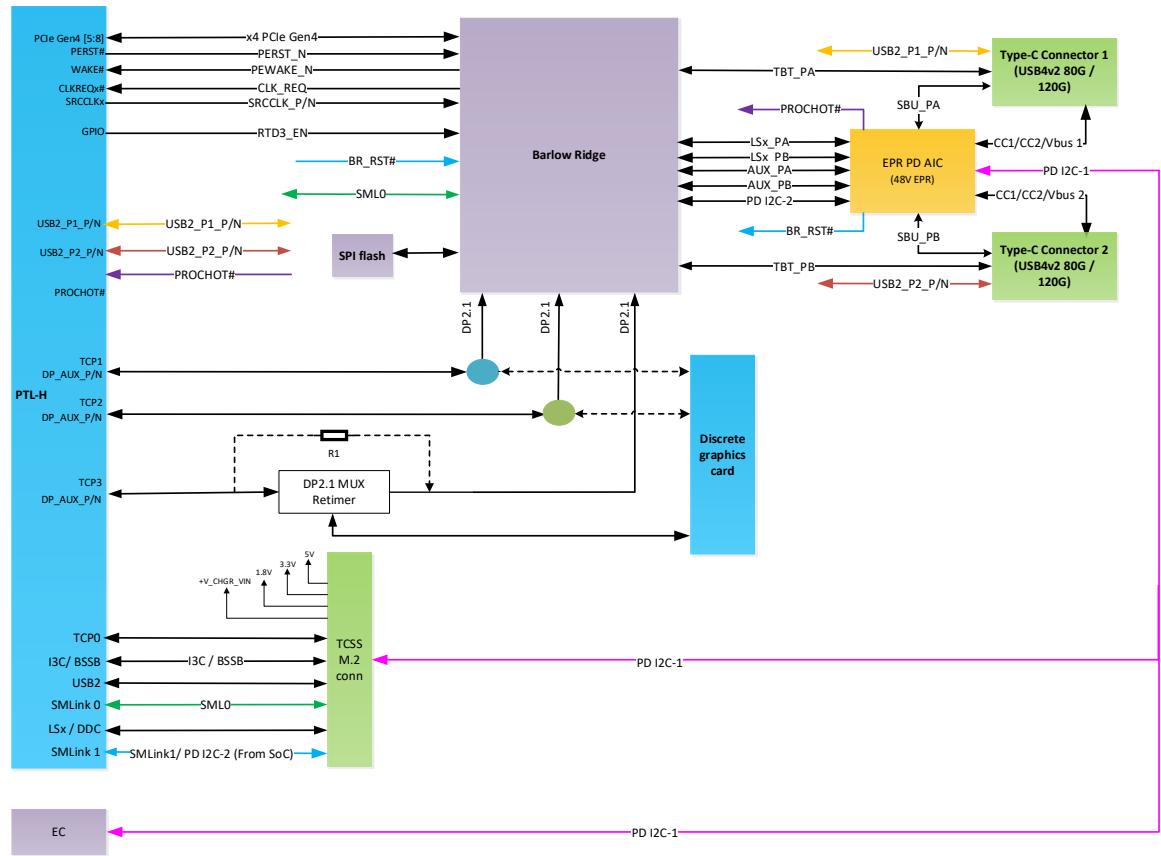


Figure 15 : PTL-UH LP5 CAMM dTBT Barlow T3 RVP display and TCSS high level block diagram

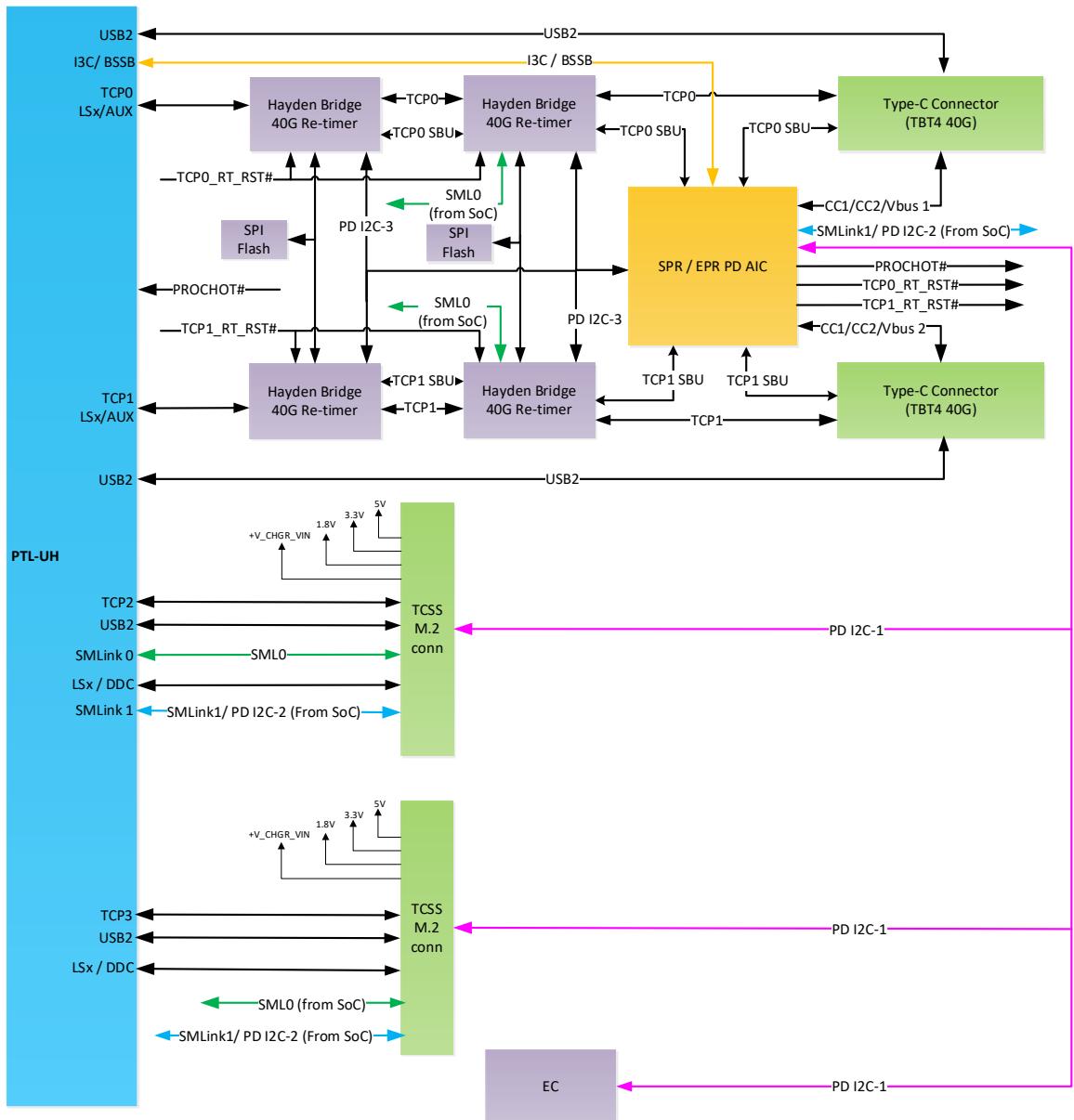


Figure 16 : PTL-U/H DDR5 SODIMM T3 RVP TCSS and display high level clock diagram

**Note:**

1. Both 28V and 48V EPR with common PD controller footprint will be supported on all the RVPs.
2. More EPR feature details on PTL-U/H are given in upcoming sections.
3. On PTL-U/H LP5 CAMM dTBT Barlow RVP, Barlow Ridge with USB4v2 support is soldered down.

## 6.2

### Modular TCSS AIC support

Type-C IO components are generally placed on the motherboard. For each variety of IO requirements based on the SKU, separate efforts in terms of electrical, mechanical and development and validation efforts are needed. RVP supporting these configuration needs to support nearly 20+ configuration as Type-C validation topologies. This results in multiple RVP construction and reworks for each configuration.

Modular approach tends to reduce these efforts significantly and reduce the number of RVP configurations needed. Modular TCSS AICs have been developed to validate different configurations of ports (Type-C / HDMI / DP / USB3 (Type A) / eDP) without the need for building dedicated RVPs to support these configs, thereby, reducing the number of RVPs required and save on integration and validation cost. One RVP can support all Type-C validation. Modular TCSS AIC is a new feature being intercepted on PTL-U/H platforms.

To enable modularity on RVP, the TBT /USB4 lanes from the SoC needs to be used as the data link for the different IO port requirements (TBT / USB-C / Type-A / DP / HDMI). The IO ports can be incorporated into a separate module which come in a specific formfactor (such as 30x30 mm here). With different modules, the system feature set can be varied according to the segment requirements. Based on IO requirements, different modules can be ordered and validated.

On PTL-U/H RVP, following table lists down the POR modules for different RVP SKUs.

**Table 13: Modular TCSS AICs support on PTL-U/H RVP SKUs**

TCP Ports	RVP SKUs			
	RVP1: PTL U/H - T3PCB - LP5 MD	RVP2: PTL U/H – T3PCB - dTBT Barlow – LP5 CAMM	RVP3: PTL-U/H - T4PCB - LP5 MD	RVP4: PTL U/H - T3 PCB - DDR5 SODIMM
TCP0	On board type-C port 1	M.2 Modular TCSS: USB-C Re-timer Module	M.2 Modular TCSS: USB-C Re-timer Module	On board type-C port 1
TCP1	On board type-C port 2	Barlow Ridge DP-In port 1	M.2 Modular TCSS: HDMI Re-driver Module	On board type-C port 2
TCP2	M.2 Modular TCSS: USB-C Re-timer Module	Barlow Ridge DP-In port 2	On board type-C port 1	M.2 Modular TCSS: USB-C Re-timer Module
TCP3	M.2 Modular TCSS: HDMI Re-driver Module	Barlow Ridge DP-In port 3	On board type-C port 2	M.2 Modular TCSS: HDMI Re-driver Module

**Note:**

- (a) Multiple configurations of modular TCSS AICs (such as TBT / HDMI / USB type-A / eDP) are available.
  - a. All these modular TCSS AICs are interchangeable on TCP0 and TCP1 ports (except for eDP module).
  - b. The above table lists the POR modules as per landing zone and does not restrict the usage of other modules.
  - c. All modular TCSS AICs are ‘plug and play’ in G3 state.
- (b) The eDP modular AIC can be validated only on TCP0 ports
  - a. Secondary eDP on type-C is enabled only on TCP0 port of PTL-U/H SOC.
  - b. High power eDP panels are not supported on the eDP module.

For more details on modular TCSS AICs and user guide, please refer below link:

<https://goto/tcssmodule>

User Guide : [LINK](#)

#### 6.2.1

#### List of POR TCSS Modules

The list below shows the POR TCSS modules planned on PTL RVP

**Table 14: POR TCSS modules on PTL-U/H RVPs**

Module Name	Module Class	Module No.	Volume
TBT-40G Hayden Bridge Retimer, TI-PD Module	100	103	Y
TBT-40G Hayden Bridge Retimer – CCG6	100	104	N
TBT-40G Retimer (RTK) - Chrome	100	105	N
HDMI 12Gbps Redriver Module	300	301	Y
HDMI 12Gbps Retimer Module	300	302	N
eDP short length Module	500	500	N
eDP long length Module	500	501	N
Type-A Redriver less Module	600	600	Y
USBC Internal Cable	900	900	N
Gothic Bridge Module - non cascaded	700	700	N
Gothic Bridge Module – cascaded	700	701	N

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*Note: Please refer to the Modular TCSS wiki page <https://goto/tcssmodule> for the latest information of modules, block diagrams and collaterals of the modules*

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## 6.3

### Discrete TBT Barlow Ridge support

PTL-U/H LP5 CAMM SKU (RVP2) shall support discrete Thunderbolt/USB4.2 Type-C ports with Barlow Ridge discrete Thunderbolt controller soldered down on the mother board.

Barlow Ridge Device/Hub is a USB4 Ver2 controller that acts as a Hub or a point of exit in the USB4 Ver2 domain. The USB4 Ver2 domain is built as a tiered-star topology of TBT/USB4 enabled products. USB3, PCIe and DisplayPort protocols are encapsulated into the USB4 fabric and can be tunneled across the USB4 domain. The Barlow Ridge Thunderbolt controller also acts as a flexible re-timer for DP protocol, or a USB3.2 Hub.

Barlow Ridge USB4 connection data rate is 40Gbps per lane (supporting overall TBT 80G / 120G speeds) and is compatible with USB4 Ver2 specification enabling USB4 link at Gen4, as well as backward compatible with Gen3 and Gen2 lane speeds.

Barlow Ridge supports multiple standard protocol IOs such as,

- PCIe Gen4
- DisplayPort (DP) 2.1
- USB4 v2.0 or TBT Gen3
- USB 3.2 Gen2x2
- USB 2.0
- SPI
- JTAG
- I2C
- SMBus

#### 6.3.1

### High level features of Thunderbolt host controller

Following table describes the high-level features of Barlow Ridge host controller,

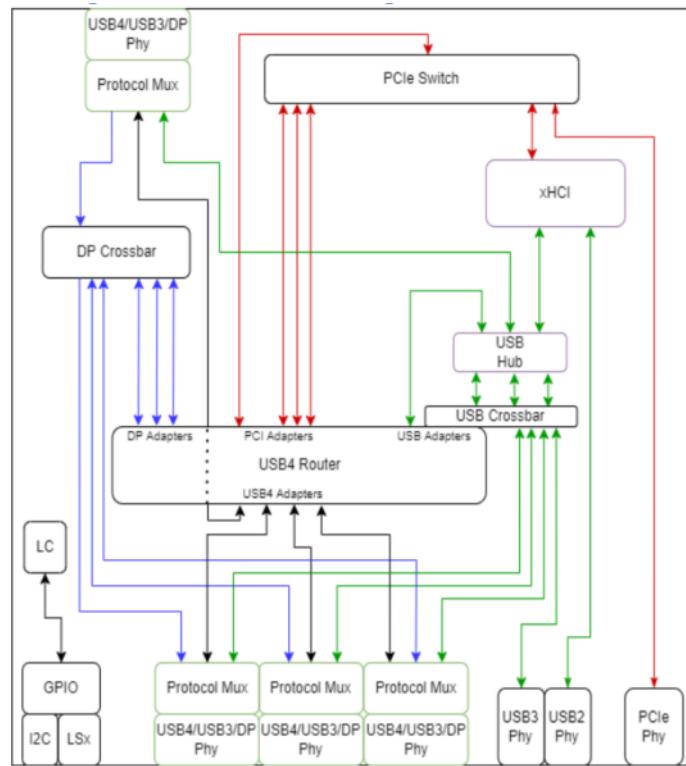
**Table 15: High level features of Barlow Ridge TBT controller**

Protocol		Barlow Ridge (Host)
Thunderbolt / USB4 Ports	TBT / USB4 Ports (Interface rate)	2x TBT 80/120G (JHL9580 SKU) (10.0/10.3/20.0/20.6/40)
		2x TBT4 (JHL9540 SKU) (10.0/10.3/20.0/20.6)
	Tunneled Protocols	DisplayPort2.1, PCIe, USB3
	USB4 v2 Support	Yes, w/ asymmetry (120/40)
Additional Ports / Pins	PCIe (to/from host)	x4 Gen 4
	DP-in (from GFX)	3x (up to UHBR20)
	DP-out (side port)	1x
USB2 / 3 Native	USB2	Split (from SoC/PCH)
	USB3 xHCI	USB3 (20G)
Display Native	DisplayPort / MFDP	DP2.1 (up to UHBR20) / USB3 (10G)
TBT / USB4 Protocols	DMA Tunnel	64Gbps (aggregate, via PCIe)
	USB3 Tunnel	20G
	DP Tunnel	3 Streams
	DP Features	SST, MST, DSC1.2, FEC, LTTPR, Panel Replay
	PCIe Tunnel	64 Gpbs
	PCIe Features	VTd, ACS, FBP, PTM, P2P, 256b PL
Others	Power Modes	Thunderbolt Link Electrical Idle
	Solution Power	3.25 - 4W
	CM Support	SW only
	vPro Dock Support	Yes
	Package	13 x 13mm

### 6.3.2

### Internal block diagram

Below figure is the internal block diagram of Barlow Ridge Host controller.

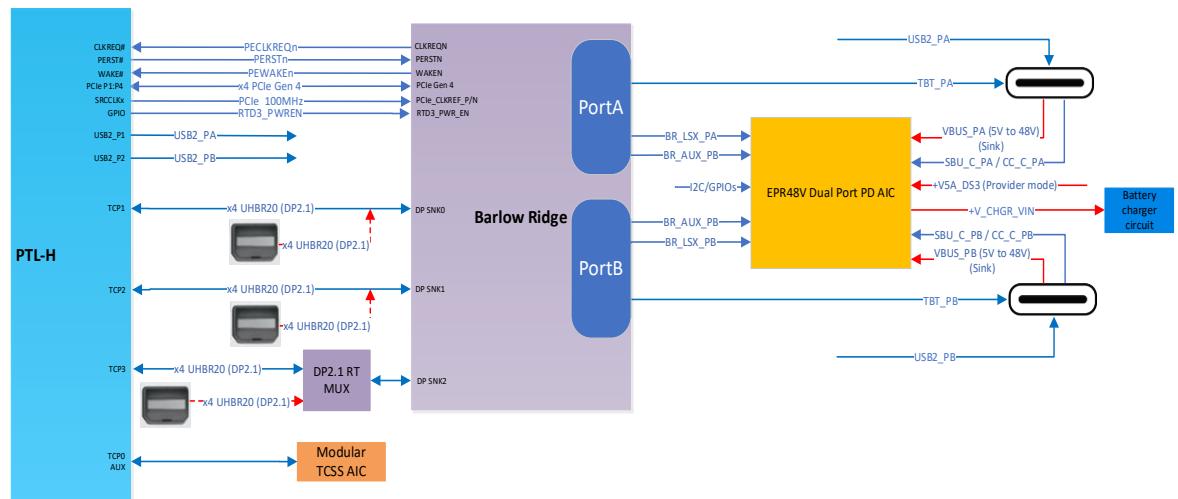


**Figure 17: Internal block diagram of Barlow Ridge controller**

### 6.3.3

### Power and data path on Barlow Ridge

Below figure shows the power and data path block diagram on Barlow Ridge controller,



**Figure 18: High level power and data path block diagram**

The following subsections describes the major interfaces that will be connected to Barlow Ridge / type-C connectors.

#### 6.3.3.1

#### PCIe interface

Barlow Ridge support x4 PCIe interface which operate at Gen4 speed. The PCIe ports 1 to 4 along with PCIe specific signals such as PERST#, WAKE#, CLKREQ#, SRCCLK# from SOC will be interfaced with Barlow Ridge for data path.

#### 6.3.3.2

#### DP2.1 interface

There are 3 DP sink ports supported, each operating at UHBR20 (DP2.1) speeds. Enhanced mini-DP connectors will be provided on each these DP sink ports. Either internal or external graphics display can be connected to these ports. Minimum number of DP streams are required to be connected for proper TBT 80 / 120Gbps functionality.

DP AUX shall follow as per DP AUX source implementation. Please refer Figure 19 for DP AUX implementation.

#### 6.3.3.3

#### USB2.0 interface

Each of the 2 type-C ports supported by Barlow, requires USB2.0 connectivity, which is enabled and driven by SOC.

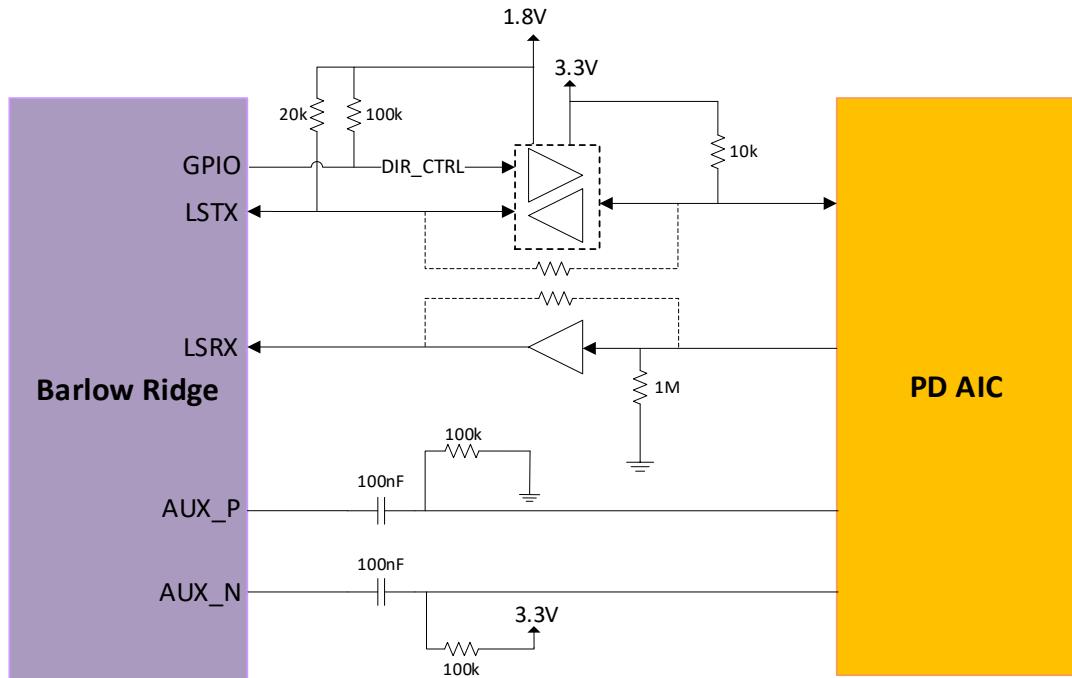
#### 6.3.3.4

#### LSx interface

To enable TBT mode on type-C ports, the LSx ports are interfaced with PD AIC.

The level shifters (1.8V to 3.3V) for LSx signals will be placed on RVP.

LSTX shall have a bidirectional level shifter, while LSRX shall have unidirectional level shifter.



**Figure 19: LSx and DP AUX implementation on dTBT SKU**

The LSx and DP AUX signal will be multiplexed in 3:1 SBU MUX present within the PD controller on PD AIC.

#### 6.3.3.5 SPI flash

Barlow Ridge uses flash memory for initialization of various internal parameters, enable/disable bits, analog modules configuration, and internal microcontrollers' ucode patches.

The flash memory map is divided into sections, which are contiguous and expected in the defined order. Each section starts with a and is followed by data.

The SPI flash will support at least 50MHz clock rate operating at 1.8V.

#### 6.3.3.6 I2C interface

Barlow Ridge communicates as an I2C master with a PD Controller as an I2C slave. As I2C master it operates at Fast mode (400KHz) speed.

Barlow Ridge I2C master supports a multi-master environment and clock stretching. It operates at 1.8V.

### 6.3.3.7

#### SML0 interface

To support vPro feature on type-C ports, SML0 will be connected between Barlow Ridge and SOC. SML0 interface will operate at 1.8V levels.

### 6.3.3.8

#### I3C / Debug support

There will be no I3C / debug support on Barlow Ridge based type-C ports.

### 6.3.3.9

#### GPIOs

RTD3\_PWREN signal is a GPIO from SOC that acts as a power enable for Barlow Ridge TBT controller and is timing critical in nature.

### 6.3.4

#### DP2.1 MUX + retimer support

DP2.1 MUX + retimer is supported on TCP3 port of SOC (DP SNK1 of Barlow Ridge).

The PS8481, a 2:1 DP jitter cleaning multiplexer for source and sink applications, accepts two DisplayPort dual-mode inputs and provides one DisplayPort dual mode output. It supports DP 2.1 all link rates up to UHBR20 (20Gbps).

Only one input port is selected at a time. Input port selection is by GPIO control (*SW* pin), which is defaulted to IN1 (SOC to retimer) path on UH-05 SKU.

On UH-13 SKU, the SW pin setting is changed in hardware to enable IN2 selection (DP connector to retimer path).

### 6.3.5

#### PD AIC support

Each Barlow Ridge will use a dedicated PD AIC to support various power and data roles on type-C ports from multiple PD vendors. EPR48V with dual port configuration shall be supported.

For more details on PD AIC, please refer to [section 6.6](#).

## 6.4

### BSSB/I3C debug

#### 6.4.1

#### I3C debug impact

The debug mode is entered through debug Accessory mode and the Analog Mux switching is handled by the PD controller on the PD AIC. I3C/BSSB closed chassis debug feature on Type-C will only be provided on TCPO port.

### 6.5

### TBT Repeaters Support

- The SoC output is a muxed port that supports TBT4/DP2.1/HDMI2.1/USB3.2/USB4 protocols. PCIe is not supported as native or alternate mode.

- In order to support TBT protocol at 40Gbps, TBT retimer is implemented on the path. Each integrated TBT type-C port requires a retimer in PTL-U/H RVP. Aux/LSx signals are routed to the retimer where they are muxed internally.
- Hayden Bridge (HBR) multiprotocol retimer is used on PTL-U/H RVP. Due to SI impact and high cost, retimer socket support is not provided on RVPs.
- SMBus would be connected to SML0 of SOC for vPRO support over TBT dock and shared with LPSS I2C (for one USBC port) for support programming of retimer in USB/DP only mode.

### 6.5.1 Hayden Bridge Retimer (HBR)

Hayden Bridge is a Type-C multi-protocol retimer to be used in on-board applications.

Hayden Bridge offers the ability to latch protocol signals into on-chip memory before retransmitting them onwards. It can be used to extend the physical length of the system without increasing high frequency jitter.

Hayden Bridge supports spec compliant retimer of following protocols:

- Display Port: four unidirectional DP lanes
- USB3.2 Gen1/2: two bi-directional USB lanes
- Thunderbolt/USB4: two bi-directional USB4 lanes
- Multifunction Display (MFD): two unidirectional lanes of DP and one bi-directional lane of USB3.2 Gen1/2

Few Features and limitations on HBR:

- Hayden Bridge device is not a symmetrical retimer. Its port B side should be always facing toward the Type-C device.
- Hayden Bridge cannot be used in multi-master applications
- Hayden Bridge doesn't implement high speed lane crossing function
- The pin type is defined to be fail-safe when it is designed to sustain voltage without current flowing into it, when there is no external power provided to the re-timer.
- Flash (1.8V, at least 50MHz clk) can be updated either through LSx or SMBUS interface.
- When operating in Bypass mode, no cable orientation supported, so BSBU1 pin will be always connected to LSTX\_SBU1 pin and BSBU2 pin will be always connected to LSRX\_SBU1 pin.
- High Speed Interface Insertion Loss
  - SoC to re-timer channel: 17dB@10GHz
  - Re-timer to Type-C connector channel: 4.5dB@10GHz (+ 0.5dB@10GHz for the type-C receptacle).
  - Re-timer to re-timer channel (for dual re-timer mode): 15dB@10GHz

#### 6.5.1.1 Hayden Bridge I2C Addressing

Hayden Bridge supports standard I2C interface. It is used for communication between the internal link controller and PD controller on the PD AIC.

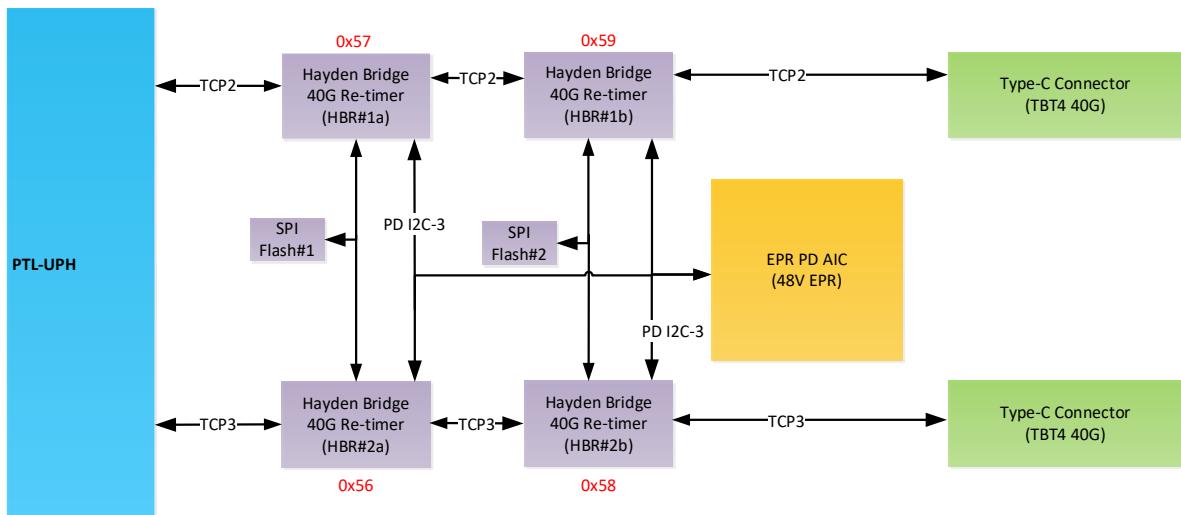
The slave address of Hayden Bridge is configured through re-timer NVM. There are four supported configurations in each NVM. The selection between the address is done by POC\_GPIO\_7 and POC\_GPIO\_11 according to the below configuration:

I2C Address	POC_GPIO_7	POC_GPIO_11 (master / slave)	HBR#
0x57	0	0	HBR#1a
0x56	0	1	HBR#2a
0x59	1	0	HBR#1b
0x58	1	1	HBR#2b

**Table 16: Hayden Bridge I2C addressing**

POC\_GPIO\_7 is I2C address select pin in HBR, while POC\_GPIO\_11 is a master / slave select strap pin in flash sharing mode.

Please refer below figure for more details on HBR numbering and I2C address correlation.



**Figure 20: I2C addressing scheme for cascaded Hayden Bridge re-timers**

### 6.5.2

### Retimer Flash Sharing

PTL-U/H RVP supports the flash sharing feature between 2 re-timers that are located close to each other physically and are connected to 2 different ports of same topology i.e

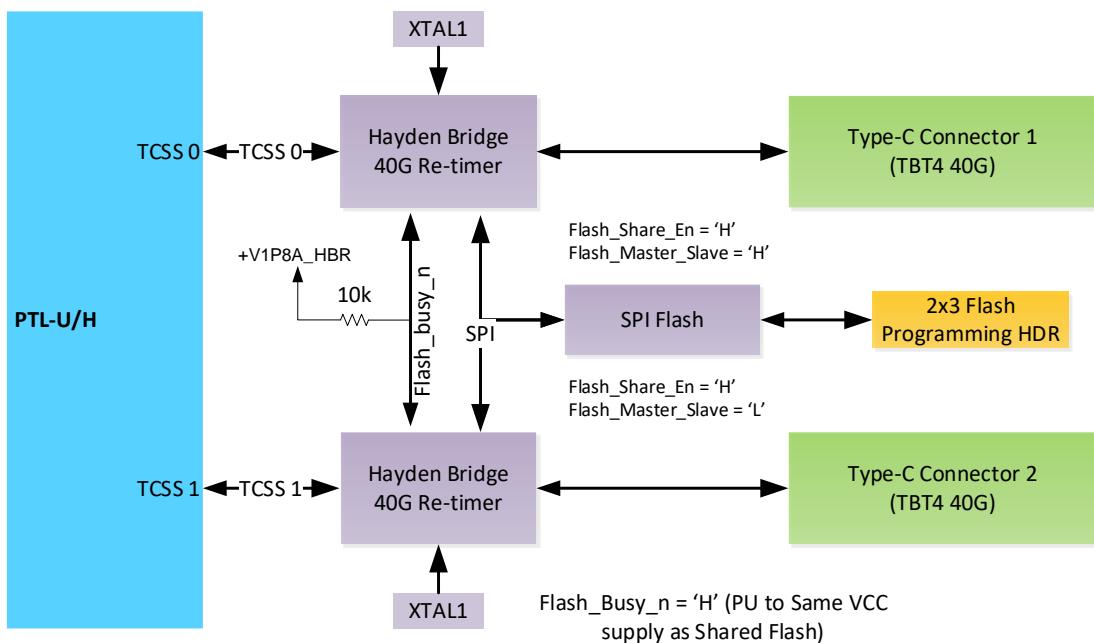
- 2 single re-timers from 2 different ports

Or

- In case of 2 cascaded re-timers ports-
  - the re-timers which are closer to SoC can share flash
  - the re-timers which are closer to type-C can share flash

Sharing flash between 2 re-timers on the same port isn't POR. PTL-U/H RVP implements the following to support the flash sharing feature:

- SPI signals should be shared (DI, DO, CS#, CLK)
- Flash\_Busy# should be shared between HBR#1 and HBR#2 with PU to flash supply
- Flash\_Master\_Slave of HBR#1 (set as Master) should be PU and PD for HBR#2 (set as Slave)
- Flash\_Share\_enable should be PU.



**Figure 21: Flash Sharing between 2 Re-timers**

As mentioned above, flash SPI lines are shared between two re-timers. SF100-dediprog header shall be provided for shared Flash initial programming. Below are the details of Dediprog Header.

- 1.27mm pitch 2x3 header is provided on RVP.
- Need Universal Adapter board and cable for programming - <https://www.dediprog.com/product/ISP-ADP-127>
- Cable as 2x4 header and Last two pins are NC in it. Hence leave last two pins unconnected and connect just 6 pins as below.
- Flash to be programmed in **RVP powered OFF**, Dediprog will be Master and 1.8V from the Dediprog shall be used on RVP



This FW programming needed only when the TBT interface is not up (initial stages of bring-up). Once the TBT interface is up and working, programming through a host is possible. Alternatively, unstuffed independent Flash footprint will be provided for the Slave retimer when flash is shared on the board.

### 6.5.3 Legacy Display ports Support

- RVP supports native HDMI connector over modular TCSS HDMI AIC.
- Secondary eDP over type-C is supported only on TCP0 port.
- Native DP ports are not supported on PTL-U/H RVP.
  - Only DP alt / tunneling mode is supported on type-C ports.

## 6.6 PD Controller Support

There is no motherboard down PD controller on PTL-U/H SKUs. Only PD AIC is POR for PTL-U/H RVPs for TCP2 and TCP3 ports. Modular TCSS AICs are supported on TCP0 and TCP1 ports. The TBT modular TCSS AIC has on board PD controller.

Port controller (TCPC) is only supported on Chrome PTL-U/H RVP SKU. Refer to [Chrome Requirements](#) section for more details.

### 6.6.1 On Board PD Controller

Not supported on PTL-U/H SKUs

### 6.6.2 Power Delivery Add-In-Card (PD AIC) Support

In RVP, Power Delivery controller Add-in Cards (PD AIC) are used for enabling multiple PD controller vendors with common footprint (complying with CFP spec rev 0.8). All the PTL-U/HRVP SKUs have support for Modular Power Delivery Add In Card (PD AIC) for TCP2 and TCP3 ports only. There is no support for motherboard down PD controller.

Power Delivery Add-In-Card (PD AIC) connector is supported for enabling PD controllers that support iTBT based SoC communications. There is no internal validation/BKC planned for multiple/different PD controller vendors on the same platform. The plan is to enable the PD AIC through plug-fest.

PD AIC will be offered through RVP demand collection window as an independent item **and it will NOT be shipped as part of boot kit.**

The new modular PD AIC 120 pin connector is supported for enabling PD controller vendors to validate new PD controllers on all the SKUs of PTL-U/H RVP platforms. PD AIC complies with PD AIC spec rev 2.05.

### 6.6.3

#### 28V and 48V EPR AIC support on PTL-U/H

On PTL-U/H platform, 28V and 48V EPR AICs will be supported. Only 2 ports out of 4 Type-C ports on the PTL-U/H RVP shall be supporting the EPR consumer profile.

Below table lists the PD vendors and SPR / EPR support across multiple PTL-U/H RVPs. Please note that SPR / EPR support on a particular RVP will be decided based on the silicon segment (TDPs).

For more information, please refer to **WSIV config sheet for latest data and BKC support for PTL Silicon (U/H12Xe/H4Xe)**.

**Table 17 : PD controller and SPR / EPR support across various PTL-U/H RVP's**

TCSS ports	RVP1: PTL U/H - T3PCB - LP5 MD		RVP2: PTL U/H – T3PCB - dTBT Barlow – LP5 CAMM		RVP3: PTL-U/H - T4PCB - LP5 MD		RVP4: PTL U/H - T3 PCB - DDR5 SODIMM
	PTL-H 12Xe	PTL-U	PTL-H 4Xe	PTL-H 4Xe	PTL-U	PTL-H 12Xe	PTL-H 4Xe
TCP0	TI EPR (48V)	-	TI SPR (20V)	TI SPR (20V)	-	GBR dual retimer EPR	CCG6 EPR (48V)
TCP1	TI EPR (48V)	-	TI SPR (20V)	-	-	GBR dual retimer EPR	CCG6 EPR (48V)
TCP2	TI SPR (20V)	GBR+HBR EPR	TI EPR (48V)	TI EPR (48V)	Realtek (data path only)	-	CCG6 SPR (20V)
TCP3	TI SPR (20V)	GBR+HBR EPR	TI EPR (48V)	TI EPR (48V)		-	CCG6 SPR (20V)

### 6.6.4

#### PD Controller Communication

- PD controller communication could be over I2C or through GPIOs as below:
  - PD (slave) to EC through I2C communication for UCSI communication (I2C1)
  - PD (slave) to PMC through USBC SML or Smlink1 Communication (I2C2)
  - PD (master) to TBT retimer for configuration (I2C3)

The I2C addresses for various PD controllers are collated in the document available in below link,

[CFP PD Controller I2C address](#)

## 6.6.5

**PD GPIO Configurations**

Below is the pinout of PD AIC connector on RVP SKU. And is also available at the SharePoint link below,

[PD\\_AIC\\_specification](#)**Table 18: 120 pin PD AIC connector pinouts**

Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
No Connect	-	NC	1	2	NC	-	No Connect
Port A VBUS Power Rail	Bi-Dir	VCC_PORTA_VBUS	3	4	VCC_PORTB_VBUS	Bi-Dir	Port B VBUS Power Rail
	Bi-Dir	VCC_PORTA_VBUS	5	6	VCC_PORTB_VBUS	Bi-Dir	
	Bi-Dir	VCC_PORTA_VBUS	7	8	VCC_PORTB_VBUS	Bi-Dir	
	Bi-Dir	VCC_PORTA_VBUS	9	10	VCC_PORTB_VBUS	Bi-Dir	
	Bi-Dir	VCC_PORTA_VBUS	11	12	VCC_PORTB_VBUS	Bi-Dir	
	Bi-Dir	VCC_PORTA_VBUS	13	14	VCC_PORTB_VBUS	Bi-Dir	
No Connect	-	NC	15	16	NC	-	No Connect
Port A CC1 (Configuration Channel) from the protection circuit on the mother board	Bi-Dir	CC1_PortA	17	18	CC1_PortB	Bi-Dir	Port B CC1 (Configuration Channel) on the mother board
Port A CC2 (Configuration Channel) from the protection circuit on the mother board	Bi-Dir	CC2_PortA	19	20	CC2_PortB	Bi-Dir	Port B CC2 (Configuration Channel) on the mother board
Port A SBU1 (Alternate Mode) facing USB C protection circuit on the mother board	IN	SBU1_PortA_USBC	21	22	SBU1_PortB_USBC	IN	Port B SBU1 (Alternate Mode) facing the USB-C protection circuit on the mother board
Port A SBU2 (Alternate Mode) facing USB C protection circuit on the mother board	IN	SBU2_PortA_USBC	23	24	SBU2_PortB_USBC	IN	Port B SBU2 (Alternate Mode) facing the USB-C connector side.
Ground	G	GND	25	26	GND	G	Ground
I2C Clock for EC (Embedded Controller) - PD controller is Slave	IN	EC_I2C_SCL	27	28	TBT_I2C_SCL	IN	I2C Clock for Thunderbolt Controller - PD controller is Slave

Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
I2C Data for EC (Embedded Controller) - PD controller is Slave	Bi-Dir	EC_I2C_SDA	29	30	TBT_I2C_SDA	Bi-Dir	I2C Data for Thunderbolt PMC Controller - PD Controller is Slave
I2C Interrupt to EC (Embedded Controller) from PD Controller	OUT	EC_I2C_INT	31	32	TBT_I2C_INT_PortA	OUT	I2C Interrupt for Thunderbolt Controller (Port A) - From PD controller, may be merged with Port B interrupt.
Thunderbolt Controller Main Reset / Re-Timer Reset for Port A. PD Controller is the source.	OUT	TBT_PortA_RESET#	33	34	TBT_I2C_INT_PortB	OUT	I2C Interrupt for Thunderbolt Controller (Port B) - From PD controller, may be merged with PortA interrupt.
Thunderbolt Controller Main Reset / Re-Timer Reset for Port B. PD Controller is the source.	OUT	TBT_PortB_RESET#	35	36	CPU_PD_PROCHOT_N	OUT	Consolidated Prochot signal to the CPU. This should be open drain active low signal. Pull up is provided on the mother board
No Connect	-	NC	37	38	NC	-	No Connect
Ground	G	GND	39	40	GND	G	Ground
Port A SBU1 (Alternate Mode) facing Interface Controller/Lsx Tx	IN	LSx_TX_PortA_CNTRL	41	42	LSx_Tx_PortB_CNTRL	Bi-Dir	Port B SBU1 (Alternate Mode) facing Interface Controller / Lsx Tx
Port A SBU2 (Alternate Mode) facing Interface Controller/Lsx Rx	IN	LSx_RX_PortA_CNTRL	43	44	LSx_Rx_PortB_CNTL	Out	Port B SBU2 (Alternate Mode) facing interface Controller / Lsx Rx
I2C Clock for Retimer / Mux devices - PD is Master	OUT	PD_I2C3_SCL	45	46	PD_I2C3_SDA	Bi-Dir	I2C Data for Retimer / Mux devices - PD is Master

Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
I2C Interrupt input from Port A retimer / mux into PD. May be combined with Port B interrupt.	IN	PD_I2C_INT_PortA	47	48	PD_I2C_INT_PortB	IN	I2C Interrupt input from Port B retimer / mux into PD. May be combined with Port A interrupt.
Port A SBU1 (Alternate Mode) facing Interface Controller / Display Auxiliary interface for PORTA; AUX_P	BiDir	SBU1_PORTA_AUX_P	49	50	NC	-	No Connect
Port A SBU2 (Alternate Mode) facing Interface Controller / Display Auxiliary interface for PORTA;AUX_N	BiDir	SBU2_PORTA_AUX_N	51	52	NC	-	No Connect
No Connect	-	NC	53	54	NC	-	No Connect
Ground	G	GND	55	56	GND	G	Ground
No Connect	-	NC	57	58	BSSB PORTA_I3C_SCL_BS SB_TX	Bi-Dir	Debug option for SBU MUX / BSSB PORTA_I3C_SCL_BSSB _TX
Thunderbolt Re-Timer Load Switch Enable for Port A	OUT	DG_TBT_LS_EN_Port A	59	60	BSSB PORTA_I3C_SDA_B SSB_RX	Bi-Dir	Debug option for SBU MUX / BSSB

Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
							PORTA_I3C_SDA_BSSB_RX
Thunderbolt Re-Timer Load Switch Enable for Port B	OUT	DG_TBT_LS_EN_Port B	61	62	PORTB_CCD_SBU1	Bi-Dir	Alternate Closed Chassis Debug (CCD) SBU1 on PortB
I2C Interrupt to EC (Embedded Controller) from PD Controller for PORTB only (Chrome only)	OUT	EC_I2C_INT_PORTB	63	64	PORTB_CCD_SBU2	Bi-Dir	Alternate Closed Chassis Debug (CCD) SBU2 on PortB
Ground	G	GND	65	66	NC	-	No Connect
3.3V power from motherboard to PD AIC	IN	VCC3V3_DS3	67	68	NC	-	No Connect
1.8V power from motherboard to PD AIC	IN	VCC1V8_DS3	69	70	SBU1_PORTB_AUX_P	Bi-Dir	Port B SBU1 (Alternate Mode) facing Interface Controller / Display Auxiliary interface for PORTB;AUX_P
Ground	G	GND	71	72	SBU2_PORTB_AUX_N	Bi-Dir	Port B SBU2 (Alternate Mode) facing Interface Controller / Display Auxiliary interface for PORTB;AUX_N
No Connect	-	NC	73	74	NC	-	No Connect

Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
Port A Voltage sense (+)	Out	+V5A_TCP_PA_CSP	75	76	NC	-	No Connect
Port A Voltage sense (-)	Out	+V5A_TCP_PA_CSN	77	78	NC	-	No Connect
No Connect	-	NC	79	80	GND	G	Ground
Ground	G	GND	81	82	GND	G	
	G	GND	83	84	+V5A_TCP_PB_CSP	Out	Port B Voltage sense (+)
Input 5V @ 4.7A max. Mother board to supply DS3 Power rail.	IN	V5_DS3	85	86	+V5A_TCP_PB_CSN	Out	Port B Voltage sense (-)
	IN	V5_DS3	87	88	DG_SLOT_ID	IN	AIC Slot Identification
							0 --> PD AIC1
							1 --> PD AIC2

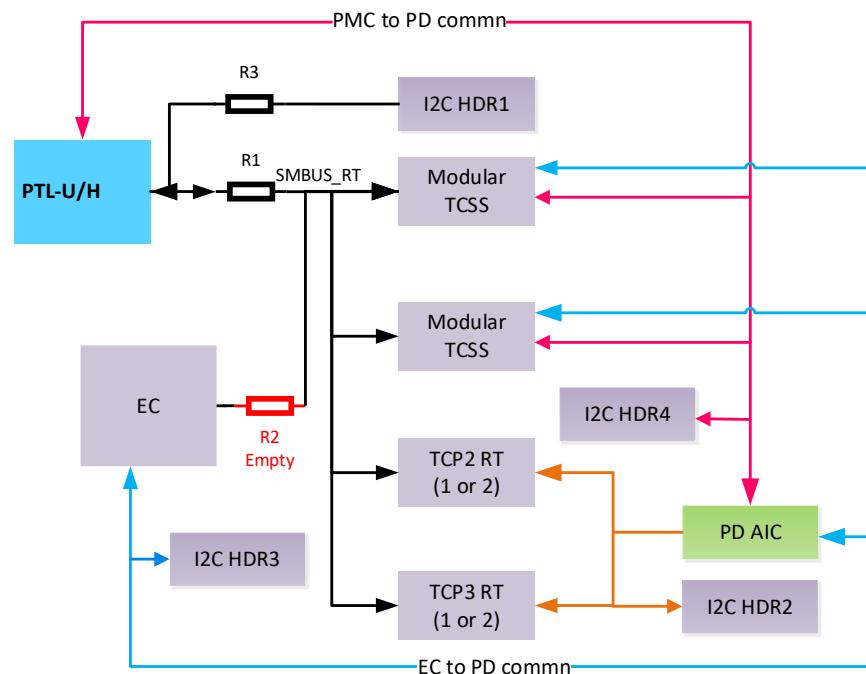
Description	Dir w.r.t. PD AIC	Net Name	Pin #	Pin #	Net Name	Dir w.r.t. PD AIC	Description
	IN	V5_DS3	89	90	NC	-	No Connect
	IN	V5_DS3	91	92	I2C_ADDR1	IN	EC_I2C address configuration bit 1 (ADCIN1 on T1 and Strapping if any on other PD Controllers)
	IN	V5_DS3	93	94	+VCC3V3_LDO_PD_AIC	Out	3.3V LDO generated by PD controller for ADCIN address
	IN	V5_DS3	95	96	TP_GPIO_SPARE9	-	Test point
	IN	V5_DS3	97	98	GND	G	Ground
Ground	G	GND	99	100	GND	G	
	G	GND	101	102	PW_VCCHV_VBUS	IN	VBUS for Charging input
VBUS for charging input	IN	PW_VCCHV_VBUS	103	104	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	105	106	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	107	108	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	109	110	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	111	112	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	113	114	PW_VCCHV_VBUS	IN	VBUS for Charging input
	IN	PW_VCCHV_VBUS	115	116	PW_VCCHV_VBUS	IN	VBUS for Charging input
Ground	G	GND	117	118	GND	G	Ground
	G	GND	119	120	GND	G	

## 6.6.6

**PD and Retimer Debug Support**

All the RVP SKUs supports following headers for debug purposes. By default, all the debug headers paths are enabled. All headers related to PD controller will be provided on PD AIC

- Individual JTAG headers (HDR\_2X3) on all the retimers – Present on RVP
- PD to retimer I2C header (HDR\_2X3) – Present on PD AIC
- EC to PD I2C header (HDR\_1X3) – Present on RVP
- PMC (USBC SML or SMLink1) to PD I2C header (HDR\_1X3) – Present on RVP
- Soc (SMLink0) to Retimer (HDR\_1X3) – PRESENT ON RVP



**Figure 22: PD/Retimer I2C debug headers**

## 6.7

## Download & Execute (DnX) Support

This feature allows to download and execute the content from another system over USB2.

To enter in DnX mode, the DnX forcedload GPIO should be asserted. In case of RVP, the DnX forcedload is asserted by EC based on button press. On RVP, the LED is available to indicate the DnX progress.

This is supported on lowest USB2 port number in SoC. In PTL-U/H, USB2.0 port-0 is the lowest port number from the SoC.

The USB2.0 port mapping on the type-C ports should be in incremental order, to support the device mode. The violation of the incremental order port mapping may affect the device mode operation. Refer USB section of this document for PTL-U/H RVP port mapping.

Example for correct incremental order port mapping

**Table 19: Correct incremental order for USB2.0 and TCP port mapping**

TCP port number	USB 2 port number	Remarks
TCP0	USB2_0	
TCP1	USB2_2	
TCP2	USB2_4	TCP1 is assigned with USB2_2; then USB2_1 should not be used in TCP2
TCP3	USB2_7	TCP (0,1,2,3) and USB2(0,2,4,7) both port numbers are in incremental order

Example for incorrect incremental order port mapping

**Table 20: Incorrect incremental order for USB2.0 and TCP port mapping**

TCP port number	USB 2 port number	Remarks
TCP0	USB2_0	
TCP1	USB2_7	
TCP2	USB2_2	Incorrect assignment; TCP1 is assigned with USB2_7; then USB2_2 should not be used in TCP2
TCP3	USB2_4	Incorrect assignment; TCP1 is assigned with USB2_7; then USB2_4 should not be used in TCP3

## 6.8

### Feature list supported on PTL-U/H RVPs

The Table 21 provides the quick features list. The below table provides complete feature list supported on various PTL-U/H RVPs:

**Table 21 : Various Type-C port Features in PTL-U/H RVPs**

SL No	Features	Mode	RVP1: PTL U/H - T3PCB - LP5 MD	RVP2: PTL U/H – T3PCB - dTBT Barlow – LP5 CAMM	RVP3: PTL-U/H - T4PCB - LP5 MD	RVP4: PTL U/H - T3 PCB - DDR5 SODIMM
1	Number of USBC ports		2	2	2	2
2	Power Profile - Consumer	5V-20V @ 5A	Yes	Yes	Yes	Yes
3	EPR Power Profile - Consumer	5V-48V @ 5A (PTL-U/H)	Yes	Yes	Yes	Yes
4	Power Profile – Provider (On board type-C ports)	5V @ 3A, 5V @ 1.5A. 1 port at 3A and other ports at 1.5A at a given time.	Yes	Yes	Yes	Yes
5	Power Profile – Provider (Modular TCSS AIC based type-C ports)	5V @ 3A, 5V @ 1.5A. 1 port at 3A and other ports at 1.5A at a given time	Yes	Yes	Yes	Yes
6	POR PD controller	Modular PD AIC	Only PD AIC	Only PD AIC	Only PD AIC	Only PD AIC
7	USBC Internal cable topology	<a href="#">5V@3A power profile FFC cable</a>	No	No	No	No
8	BC1.2 support for Chrome	<a href="#">5V@1.5A provider</a>	No	No	No	No
9	Non-TBT, USB/DP direct port	DP/USB/PCIE tunneling	No	No	No	No
10	DP2.0 with Repeater	HBR3	Not POR	Not POR	Not POR	Not POR
11	USB3.2 redriver	USB3.2 Gen2x2	Not POR	Not POR	Not POR	Not POR
12	TBT - Single Retimer 40G	HB retimer TBT/USB/DP	Yes, 2 No's	No	Yes, 2 No's	No
13	TBT - Retimer 20G	HB retimer TBT/USB/DP	No	No	No	No
14	Dual TBT retimer 40G	HB retimer TBT/USB/DP	No	No	No	Yes
15	USB4 Retimerless 20G	TBT/USB/DP	No	No	No	No
16	3 <sup>rd</sup> party redriver + TBT retimer	3 <sup>rd</sup> party Redriver + BB retimer TBT/DP/USB	No	No	No	No
17	dTBT Barlow Ridge support solder down	BR dTBT TBT/USB/DP	No	Yes	No	No
18	dTBT Maple Ridge + Burnside Bridge support	MR dTBT+BB TBT/USB/DP	No	No	No	No

19	DP-in (DP2.1 input) support for switchable graphics	Via dTBT Barlow Ridge Controller.	No	Yes	No	No
20	DP2.1 support over enhanced mini-DP connectors	DP2.1 output from SOC	No	Yes	No	No
21	DnX Support	DnX supported with external jumper or via EC	Yes. One port	Yes. One port	Yes. One port	Yes. One port
22	USBC debug support	USB3 DbC/ USB2 DbC/HTI Trace boxes ("Unitracer", "PRI7" or "VPlus")	Yes, 2 No's	Yes, 2 No's	Yes, 2 No's	Yes, 2 No's
23	USBC debug support	2-wire DCI-OOB over I3C platform mux / Debug accessory mode	Yes, 1 No's	Yes, 1 No's	Yes, 1 No's	Yes, 1 No's
24	USBC switching AIC support - Cswitch 2.0 <sup>v</sup>	Not supported on vertical ports.	Yes	Yes	Yes	Yes
25	USBC switching AIC support Cswitch Rev4.0 <sup>v</sup>	54mm spacing between Type-C (or other) Con	No*	No*	No*	No*
26	VPRO support	SML1 connection between retimer and PCH	Yes	Yes (over Barlow Ridge)	Yes	Yes
27	Ardent connector		No	No	No	No

\*Left and right C-Switch combo should be used on the adjacent Type-C ports. 54mm spacing from other connectors is not feasible.

## 6.9

### Chrome Connector Support

The plan is to support Type C on chrome SKU through MTL TCPC AIC for TCP2/3 port. Chrome USB-C modular AIC based on TCPC shall be used for TCP0/1 ports. Refer to [Chrome section](#) for more details.

## 6.10

### Protection Circuit

Specific ESD protection diodes are provided for all the signals close to the Type C port connector. The Type-C connector has a higher pin density than legacy USB connectors. As a result, it is easier to accidentally short VBUS to adjacent pins. With the potential of having VBUS of up to 48 V, it is possible to have a short between the 48V and a 5V line (such as SBU, CC and so on). To protect against this potentially catastrophic event, VBUS short circuit protection is required. Short circuit protection on the SBU and CC lines are taken care in PD add-in card. No additional protector IC is provided on RVP board.

VBUS is also adjacent to the high differential lines, refer to the connector pinout in the Type C specification. These pins are protected using a series Resistor-Capacitor combination between the pins of the Type C connector and the chip. Refer to the Product Design Guide (PDG) document for more accurate details on the same.

# 7 HSIO

PTL-U/H PCD Die supports various HSIO interfaces to connect different peripheral devices.

## 7.1 PTL-U/H Platform HSIO support details

PTL-U/H PCD die supports:

1. 2 USB 3.2 Gen2x1(10G) lanes.
2. 8 PCIe Gen4 lanes. 1 of these lanes is muxed with Gbe interface.
3. PTL-P PCD die supports 4 PCIe Gen5 lanes; PTL-H PCD die supports 12 PCIe Gen5 lanes.

### 7.1.1 PCIe device support on PTL-U/H RVP

PTL-U/H RVP supports the following PCIe Devices/ IO connectors:

1. Gen1 Integrated Gbe LAN
2. Gen4 M.2 Key-E WLAN
3. Gen4 M.2 Key-B WWAN
4. Gen4 Barlow Ridge discrete TBT controller
5. Gen4 / Gen5 M.2 Key-M SSD
6. Gen4 x1 / x2 PCIe DT Slot (Open ended) – for SD 7.0 AIC, Foxville discrete LAN AIC
7. Gen4 / Gen5 x4 PCIe DT Slot (Open ended) – for various FV test cards
8. Gen5 x8 PCIe DT Slot (Open ended) – for discrete GFx

### 7.1.2 HSIO configurations in PTL-U/H RVP's

Based on the platform LZ, POR & platform requirement HSIO Mapping has been done for PTL-U/H Platform. RVP ModPHY Mapping table will be used by the soft strap team & BIOS team to configure the individual lane as per RVP recommendation. RVP Implementation will support multiple configurations by sharing the same lanes for different function. Board rework and IFWI changes will be required to enable the shared feature which has different function.

**Table 22 : HSIO support on PTL-U/H Platform**

Die	PTL-U/H HSIO ports						
	PCD-P	PCD-H	Port #	USB 3.2 10G	Gbe LAN	PCIe	PCIe Port Configs
PCD Die	Yes	Yes	USB3.2 Gen2x1(10G) 1	Yes			
	Yes	Yes	USB3.2 Gen2x1(10G) 2	Yes			
	Yes	Yes	PCIe Gen4 1 / Gbe LAN		Yes	Yes	x2 x1
	Yes	Yes	PCIe Gen4 2			Yes	x4 x2 x1
	Yes	Yes	PCIe Gen4 3			Yes	x2 x1
	Yes	Yes	PCIe Gen4 4			Yes	x2 x1
	Yes	Yes	PCIe Gen4 5			Yes	x2 x1
	Yes	Yes	PCIe Gen4 6			Yes	x4 x2 x1
	Yes	Yes	PCIe Gen4 7			Yes	x2 x1
	Yes	Yes	PCIe Gen4 8			Yes	x2 x1
	Yes	Yes	PCIe Gen5 1			Yes	x2
	Yes	Yes	PCIe Gen5 2			Yes	x4 x2
	Yes	Yes	PCIe Gen5 3			Yes	
	Yes	Yes	PCIe Gen5 4			Yes	

	Yes	PCIe Gen5 5			Yes			
	Yes	PCIe Gen5 6			Yes			
	Yes	PCIe Gen5 7			Yes			
	Yes	PCIe Gen5 8			Yes			
	Yes	PCIe Gen5 9			Yes			
	Yes	PCIe Gen5 10			Yes			
	Yes	PCIe Gen5 11			Yes			
	Yes	PCIe Gen5 12			Yes			

Table 23 : HSIO Mapping on PTL-U/H RVP's

PTL-U/H HSIO ports		RVP1: PTL U/H - LP5 T3		RVP2: PTL U/H - dTBT BR - LP5 CAMM T3		RVP3: PTL-U/H - LP5 T4		RVP4: PTL U/H - DDR5 SODIMM T3	
D i e	Port #	RVP-1 (default)	RVP-1a (rework)	RVP-2 (default)	RVP-2a (rework)	RVP-3 (default)	RVP-3a (rework)	RVP-4 (default)	RVP-4a (rework)
P C D D i e	USB3.2 Gen2x1 (10G) 1	USB3.2 gen1 TAP-1	-	USB3.2 gen2 TAP-1 (vertical)	-	USB3.2 gen2 TAP-1 with RDRVR	-	USB3.2 gen2 TAP-1 with RDRVR	-
	USB3.2 Gen2x1 (10G) 2	USB3.2 gen2 TAP-2 with RDRVR	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRVR	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRVR	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRVR	M.2 WWAN Key-B
	PCIe4 1/Gbe	Gbe LAN Jacksonville	-	Gbe LAN Jacksonville	-	Gbe LAN Jacksonville	-	Gbe LAN Jacksonville	x4 gen4 DT CEM - LR
	PCIe4 2	M.2 WWAN Key-B		M.2 WWAN Key-B		M.2 WWAN Key-B		M.2 WWAN Key-B	
	PCIe4 3	x1 gen3 DT CEM		x1 gen3 DT CEM		x2 gen3 DT CEM (x2 over x4) - LR		x2 gen4 DT CEM (x2 over x4) - LR	
	PCIe4 4	M.2 WLAN Key-E		M.2 WLAN Key-E		M.2 WLAN Key-E		M.2 WLAN Key-E	
	PCIe4 5	M.2 Gen4 SSD Key-M (NIST)	-	x4 Gen4 dTBT BR device down	-	M.2 Gen4 SSD Key-M (NIST)	-	M.2 Gen4 SSD Key-M (NIST)	-
	PCIe4 6								
	PCIe4 7	M.2 Gen5 SSD Key-M	x4 Gen5 DT CEM	M.2 short channel 1A Gen5 SSD Key-M (NIST)	M.2 Gen5 flex topology AIC	M.2 Gen5 SSD Key-M	-	M.2 Gen5 SSD Key-M	-
	PCIe4 8								
	PCIe5 1								
	PCIe5 2								
	PCIe5 3								
	PCIe5 4								
PCIe5 5	PCIe5 5	x8 Gen5 DT CEM	-	x8 Gen5 DT CEM	-	x8 Gen5 DT CEM	x4 Gen5 DT CEM (x4 over x8)	x8 Gen5 DT CEM - LR+PI	-
	PCIe5 6								
	PCIe5 7								
	PCIe5 8								
	PCIe5 9								
	PCIe5 10								
	PCIe5 11								
	PCIe5 12								

## 7.2

### PTL-U/H RVP HSIO Mapping

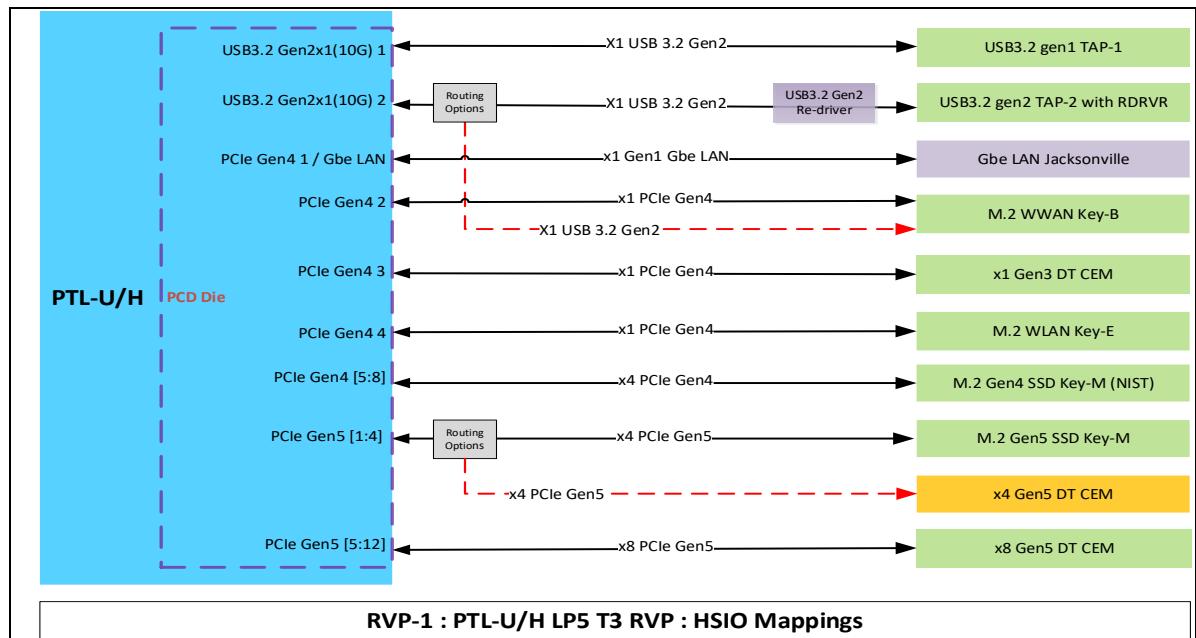


Figure 23 : RVP-1: PTL-U/H LP5 T3 RVP : HSIO Mappings

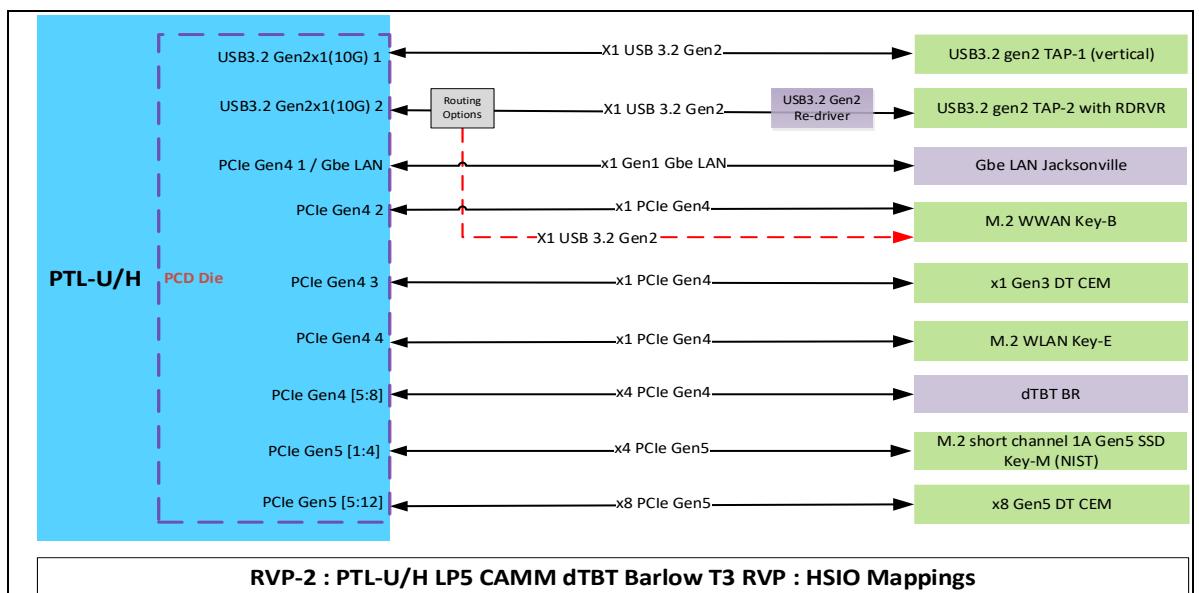


Figure 24 : RVP-2: PTL-U/H LP5 CAMM dTBT Barlow T3 RVP : HSIO Mappings

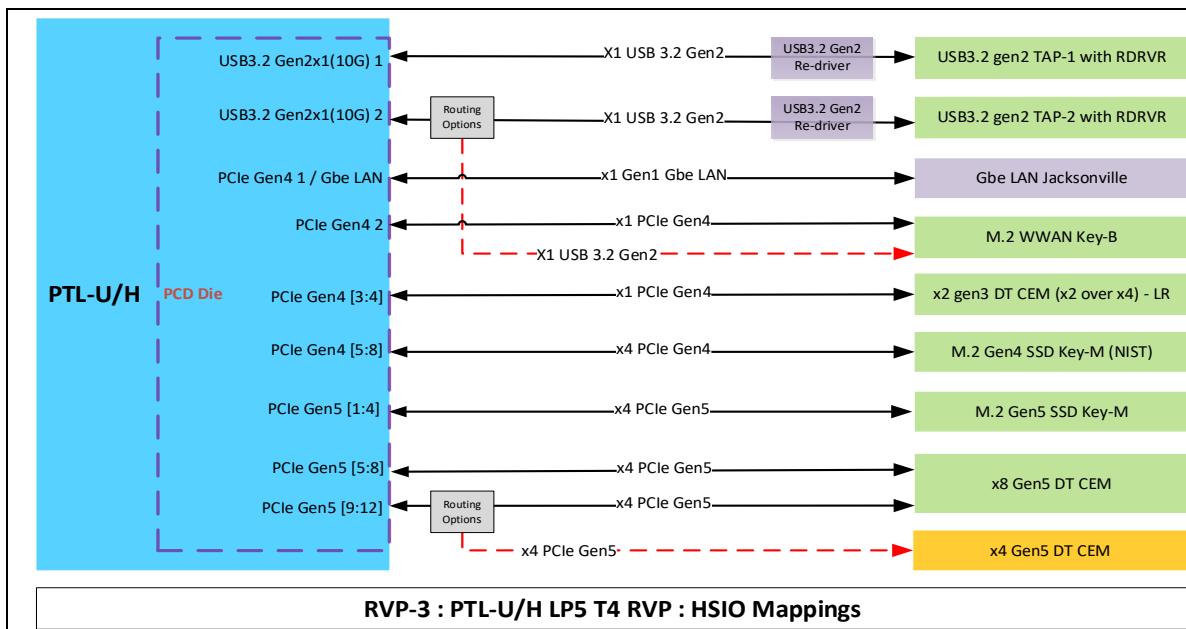


Figure 25 : RVP-3: PTL-U/H LP5 T4 RVP: HSIO Mappings

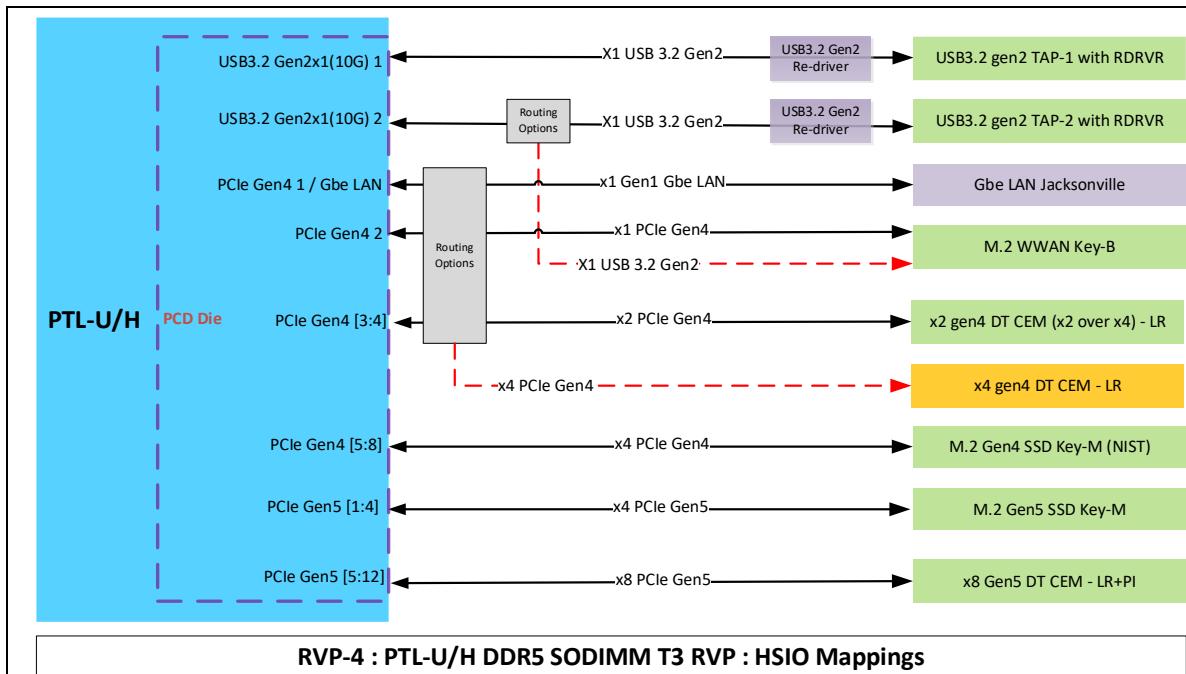


Figure 26 : RVP-4: PTL-U/H DDR5 SODIMM T3 RVP : HSIO Mappings

***PCIe: Requests from teams to accommodate other delta configs***

Ask	Proposed Solution
Dual x2 PCIE5 SSD support on x4 Gen5 (x2+x2 config)	Teams to use MCIO AoB adapter boards
GPIO header on PCIE5 lanes [1:4] routed from M.2 connector over RVP-1,2 & from CEM Slot over RVP-1	For MCIO AOB adapter to test 2x2 furcation options - Supported over RVP-1 for PXPB & PXPC - Supported over RVP-2 for PXPC - Supported over RVP-3 for PXPB & PXPC - Supported over RVP-4 for PXPA , PXPB & PXPC
GPIO header on PCIE4 lanes [1:4] routed from M.2 connector over RVP-1 & from CEM Slot over RVP-4	For MCIO AOB adapter to test 4x1, 2x2, 1x2 & 2x1 furcation options - Supported over RVP-4 for PXPA & PXPB
SD8.0 support over RVP-4	Teams to reuse existing DT slots as per SD8.0 AIC config - Gen4 x1 CEM slot over RVP-1,2 - Gen4 x2 CEM slot over RVP-3,4
Dual x4 Gen5 M.2 support over RVP-3	Teams to use CEM to M.2 adaptor over PCIe Gen5 x4 CEM slot connector to validate the 2 <sup>nd</sup> Gen5 SSD.
Header support for DGFX PCIE5 x8 CEM slot for wake signal	Supported through rework over header pin : - RVP-1 in J8A6.3 - RVP-2 in J8A3.3 - RVP-3 in J8A4.3 - RVP-4 in J8A4.3
PCIE5 internal cable FFC topology support over RVP-2	Supported over new AIC design through short channel topology of RVP-2
RPB full size single width test card support on PCIE4 CEM slots	- Supported
PCIE5 x8 CEM slot & PCIE5 X4 slot on RVP-3 to support 2.5 width dGFX card	- Supported on x8 & x4 slot over RVP-3; but not for simultaneous test case
Cambria card on PCIE slot should not interfere with M.2 HDD	- Supported

***USB3.2 Gen2x1 : Requests from teams to accommodate other delta configs***

1. USB32 Gen1x1 Internal Cable Topology support on RVP-2
  - Request ZBB'ed.

## 8

# USB2.0

PTL-U/H PCD die supports 8 USB2.0 ports.

## 8.1

## PTL-U/H RVP : USB 2.0 Mapping

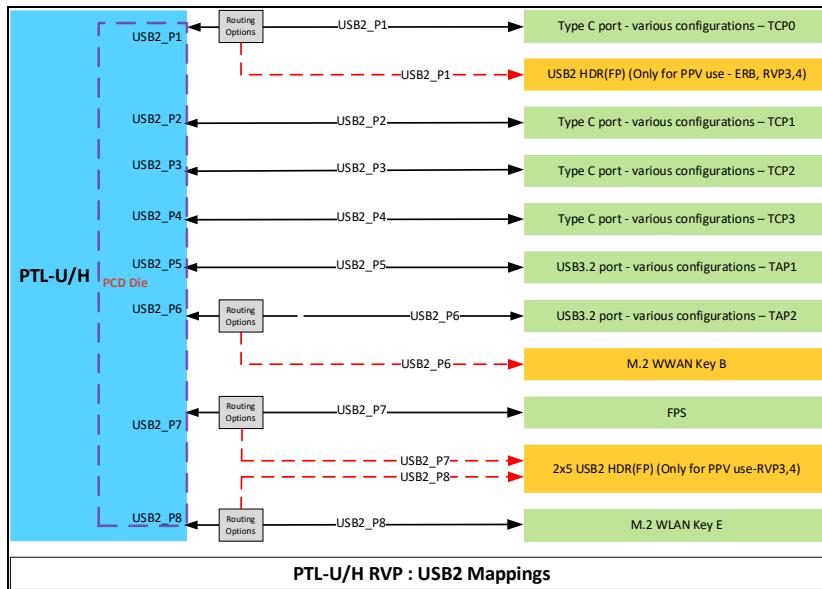


Figure 27: PTL-U/H RVP: USB2 Mappings (Only in-RVP1,3,4)

Table 24 : PTL-U/H RVP USB 2.0 port mapping across SKUs

PTL-U/H USB 2.0 ports		RVP1: PTL U/H - LP5 T3		RVP2: PTL U/H - dTBT Barlow - LP5 CAMM T3		RVP3: PTL U/H - LP5 T4		RVP4: PTL U/H - DDR5 SODIMM T3	
Die	Port #	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)
P C D D i e	P1	TCP-0 (ONBOARD TBT PORT-1)	2x5 PPV HDR	TCP-0 (M.2 MODULAR TCSS AIC-1)	-	TCP-0 (M.2 MODULAR TCSS AIC-1)	2x5 PPV HDR	TCP-0 (ONBOARD TBT PORT-1)	2x5 PPV HDR
	P2	TCP-1 (ONBOARD TBT PORT-2)	-	TCP-1 (dTBT BR)		TCP-1 (M.2 MODULAR TCSS AIC-2)	-	TCP-1 (ONBOARD TBT PORT-2)	-
	P3	TCP-2 (M.2 MODULAR TCSS AIC-1)	CRD-1 (ALTEK SUNNY A1)	M.2 WLAN Key-E	CRD-1 (ALTEK SUNNY A1)	TCP-2 (ONBOARD TBT PORT-1)		TCP-2 (M.2 MODULAR TCSS AIC-1)	CRD-1 (ALTEK SUNNY A1)
	P4	TCP-3 (M.2 MODULAR TCSS AIC-2)	-	-	-	TCP-3 (ONBOARD TBT PORT-2)		TCP-3 (M.2 MODULAR TCSS AIC-2)	-
	P5	USB3.2 gen1 TAP-1		USB3.2 gen2 TAP-1 (vertical)		USB3.2 gen2 TAP-1 with RDRV		USB3.2 gen2 TAP-1 with RDRV	
	P6	USB3.2 gen2 TAP-2 with RDRV	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRV	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRV	M.2 WWAN Key-B	USB3.2 gen2 TAP-2 with RDRV	M.2 WWAN Key-B
	P7	FPS	2x5 PPV HDR	FPS	-	FPS	2x5 PPV HDR	FPS	2x5 PPV HDR
	P8	M.2 WLAN Key-E		TCP-2 (dTBT BR)		M.2 WLAN Key-E		M.2 WLAN Key-E	

## 8.2

### USB Overcurrent (OC) Protection

PTL-U/H PCD die has implemented programmable USB OC signals. 4 OC pins are to be shared across the Type-C, USB2.0 & USB3.2 Gen2x1 Type-A ports. This allows the platform designer flexibility in routing of the OC pins & allows for unused pins to be configured as GPIOs. The current limits for the USB3.2 Gen2x1 Type-A ports is set to 900mA typical.

**Table 25: OC Protection from the individual OC protection controllers in PTL-U/H RVP**

Pin Name	PTL-U/H Configuration
Virtual	Type C port - various configurations – TCP0 Type C port - various configurations – TCP1 Type C port - various configurations – TCP2 Type C port - various configurations – TCP3
USB2_OCB_0	USB3.2 port - various configurations – TAP1 USB3.2 port - various configurations – TAP2
USB2_OCB_3	TCSS Module - Type-A over TCP module
USB2_OCB_1 / USB2_OCB_2	-

## 8.3

### USB Signal Protection

PTL-U/H RVP shall have a CMC and ESD diodes for Signal protection as suggested by PDG.

## 8.4

### USB Debug Support

Intel® DCI (Direct Connect Interface) is an Intel Technology that allows debug access by re-purposing a USB3.2 Gen 2x1 port. Advantage is debug functions & trace features can be connected using existing USB3 ports, rather than additional connectors. It supports many debug functions & can be implemented “closed chassis”. DCI connection supports run-control debug, validation, trace, DMA, OS Debug and scripting. DCI is implemented using 2 primary transport topologies:

- Intel® DCI.OOB (formerly BSSB)
- Intel® DCI.USB2/USB3 (formerly DbC)

**Table 26: USB Debug Support on PTL-U/H RVP**

Connector Details	Supported Topologies
Connector1: Type-A USB Walk-Up Port USB3.2 Gen 2x1_Port 1 & USB2_Port5	USB.DbC
Connector2: Type-A USB Walk-Up Port USB3.2 Gen 2x1_Port 2 & USB2_Port6	USB.DbC
Type C Port0: USB2_Port1	USB.DbC DCI.OOB – 2 Wire
Type C Port 1: USB2_Port2	USB.DbC DCI.OOB – 2 Wire
Type C Port2: USB2_Port3	USB.DbC DCI.OOB – 2 Wire
Type C Port3: USB2_Port4	USB.DbC DCI.OOB – 2 Wire

#### **USB2.0 : Requests from teams to accommodate other delta configs**

1. 1x4 HDR support for USB2.0 port connected to CNVi M.2 WLAN connector.
  - Teams to reuse USB2.0 2X5 FP PPV CONNECTOR-1 available over ERB , RVP-3,4.

# 9

## Clocks

PTL-U/H SOC is the primary clock generator for all sub-system on PTL-U/H RVP. The chipset has 2 major clock sources out of which all the sub-system clocks and external clock outputs are derived through internal PLLs. A high-level block diagram of the chipset clock interface is given below.

**Table 27: Clock Inputs on PTL-U/H**

Clock Name	Description
RTCX1/ RTCX2	32.768KHz crystal input for Real time clock
Single ended Crystal RTCX1	Single-ended RTC crystal input by driving 32.768Khz CMOS clock on RTCX1 [Not used on RVP]
XTAL_IN/OUT	38.4MHz crystal input for iSCLK (integrated System Clock) block
CRF_CLKREQ	To be sent to iSCLK & CRF Quasar to Synchronize CRF & Quasar
SRCCCLKREQB [8:0]	SRCCCLKREQB is used to support clock request protocol to enable or disable SRC clocks distribution to off-chip. In addition, the SRCCCLKREQB is also used for PCIe power management (L1.off, etc.).
OBS[1:0]MON_ISCLK	iSCLK monitoring pins for debug usage
SOC_REFRCOMP_ISCLK	Connected to an external precision resistor for Differential buffer, RCOMP between VSS and this pad.

**Table 28: Output signals from Clock function on PTL-U/H**

Signal Name	Frequency & SSC Support	Description
SUSCLK	32.768KHz without SSC	Suspend clock that generated from the RTC crystal oscillator
CLKOUT_SOC_[0:8]_N/P	100MHz - Gen5 Capable with SSC	100MHz differential source clock for external PCIe Device
GPP_D_21_UFS_REFCLK_SRCCCLKREQ8_B	19.2 MHz with SSC	19.2MHz single-ended reference clock for external UFS device
IMGCLKOUT [0:2]	19.2 MHz	Clock for external camera sensor, from is CLK Main PLL (low power PLL)

All SRC CLK's from SOC are Gen5 capable.

- PTL- U/P SOC support 7 SRC CLK's & 7 CLKREQ signals.
- PTL-H SOC support 9 SRC CLK's & 9 CLKREQ signals.

MFIT will expose the enables for only 7 CLKOUT[0:6] for CCG's U/P & for all 9 CLKOUT[0:8] for CCG's PTL-H. NEX/IOTG must have different MFIT to expose enables for CLKOUT 7,8 if they intend to use the same CCG's PTL-U/P package for their platforms.

By default, CLKREQ will be enabled as Native GPIO function. To use these pins as a CLKREQ it needs to be mapped in the BIOS.

The Gbe LAN PHY needs 25MHz input which will be fed from an external crystal input. The Embedded controller has the external 32.768kHz crystal input as the default option along with

SUS\_CLK option driven from SOC. Any other interface specific clocks required for third party devices will be derived out of the external crystals specific to the device requirements.

## 9.1 PTL-U/H RVP : SRC Clock and CLK REQ Mapping

Table 29 : PTL-U/H RVP SRC Clock port mapping across SKUs

PTL-U/H SRC Clock ports		RVP1: PTL U/H - LP5 T3		RVP2: PTL U/H - dTBT Barlow - LP5 CAMM T3		RVP3: PTL-U/H - LP5 T4		RVP4: PTL U/H - DDR5 SODIMM T3	
Device	Port #	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)
P C D D i e	P0	x8 Gen5 DT CEM	-	x8 Gen5 DT CEM	M.2 short channel 1A Gen5 SSD Key-M (NIST)	x8 Gen5 DT CEM	M.2 Gen5 SSD Key-M	x8 Gen5 DT CEM - <b>LR+PI</b>	
	P1	M.2 Gen5 SSD Key-M	x4 Gen5 DT CEM	M.2 short channel 1A Gen5 SSD Key-M (NIST)		M.2 Gen5 SSD Key-M		M.2 Gen5 SSD Key-M	
	P2	x1 gen3 DT CEM	Gbe LAN Jacksonville	x1 gen3 DT CEM		x2 gen3 DT CEM <b>(x2 over x4) - LR</b>		x2 gen4 DT CEM <b>(x2 over x4) - LR</b>	
	P3	Gbe LAN Jacksonville		Gbe LAN Jacksonville		Gbe LAN Jacksonville		Gbe LAN Jacksonville	
	P4	M.2 WLAN Key-E		M.2 WLAN Key-E		-		-	
	P5	M.2 WWAN Key-B		M.2 WWAN Key-B		M.2 WWAN Key-B		M.2 WWAN Key-B	
	P6	M.2 Gen4 SSD Key-M (NIST)	x4 Gen4 dTBT BR device down	x4 Gen4 dTBT BR device down		M.2 Gen4 SSD Key-M (NIST)		M.2 Gen4 SSD Key-M (NIST)	
	P7	-		-		x4 DT CEM Gen5		-	
	P8	-		-		-		-	

Table 30 : PTL-U/H RVP CLK REQ port mapping across SKUs

PTL-U/H SRC Clock ports		RVP1: PTL U/H - LP5 T3		RVP2: PTL U/H - dTBT Barlow - LP5 CAMM T3		RVP3: PTL-U/H - LP5 T4		RVP4: PTL U/H - DDR5 SODIMM T3	
Device	Port #	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)	Topology1 (Default)	Topology2 (Rework)
P C D D i e	P0	x8 Gen5 DT CEM	-	x8 Gen5 DT CEM	M.2 short channel 1A Gen5 SSD Key-M (NIST)	x8 Gen5 DT CEM	M.2 Gen5 SSD Key-M	x8 Gen5 DT CEM - <b>LR+PI</b>	MCIO AOB HDR P4
	P1	M.2 Gen5 SSD Key-M	x4 Gen5 DT CEM	M.2 short channel 1A Gen5 SSD Key-M (NIST)		M.2 Gen5 SSD Key-M		M.2 Gen5 SSD Key-M	
	P2	x1 gen3 DT CEM	MCIO AOB HDR P2	x1 gen3 DT CEM		x2 gen3 DT CEM <b>(x2 over x4) - LR</b>		MCIO AOB HDR P2	x2 gen4 DT CEM <b>(x2 over x4) - LR</b>
	P3	Gbe LAN Jacksonville	-	Gbe LAN Jacksonville		Gbe LAN Jacksonville		Gbe LAN Jacksonville	
	P4	M.2 WLAN Key-E	MCIO AOB HDR P1	M.2 WLAN Key-E		-		MCIO AOB HDR P1	
	P5	M.2 WWAN Key-B	M.2 WWAN Key-B x4 Gen4 dTBT BR device down	M.2 WWAN Key-B		M.2 WWAN Key-B		M.2 WWAN Key-B	MCIO AOB HDR P3
	P6	M.2 Gen4 SSD Key-M (NIST)		x4 Gen4 dTBT BR device down		M.2 Gen4 SSD Key-M (NIST)		M.2 Gen4 SSD Key-M (NIST)	
	P7	-		-		x4 DT CEM Gen5		-	MCIO AOB HDR P2
	P8	UFS AIC		M.2 FF - UFS AIC		UFS AIC		UFS AIC	

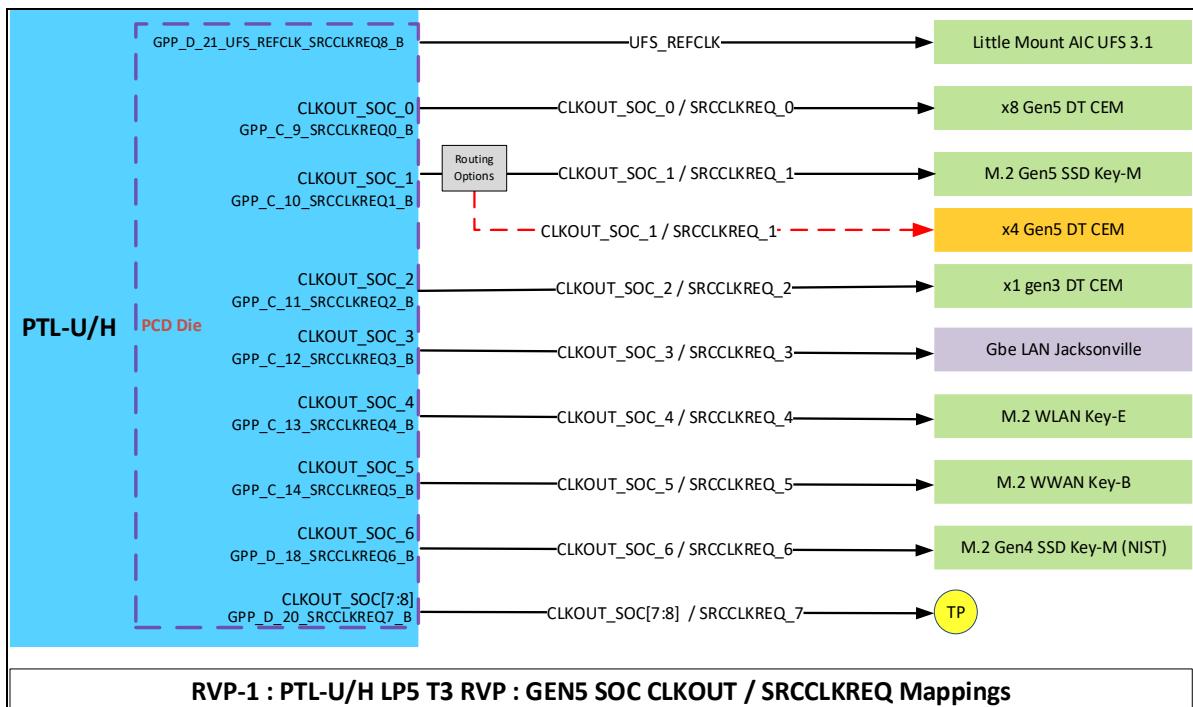


Figure 28 : RVP-1 : PTL-U/H LP5 T3 RVP : GEN5 SOC CLKOUT / SRCCCLKREQ Mappings

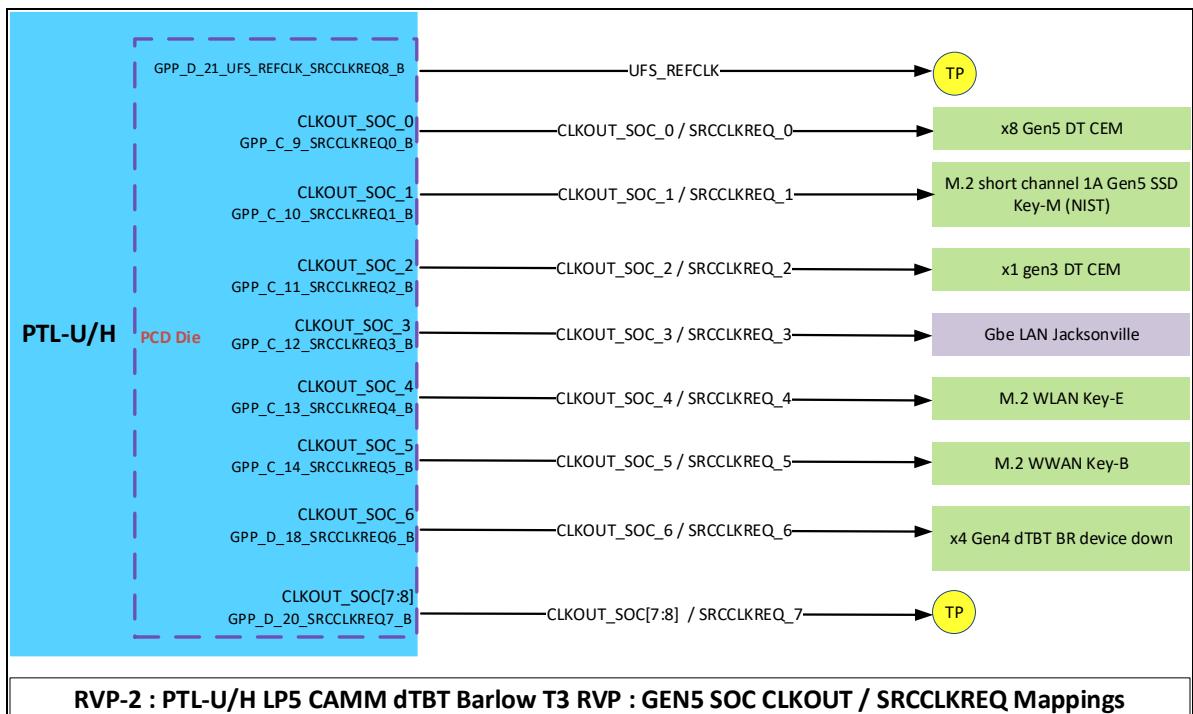


Figure 29 : RVP-2 : PTL-U/H LP5 CAMM dTBT Barlow T3 RVP : GEN5 SOC CLKOUT / SRCCCLKREQ Mappings

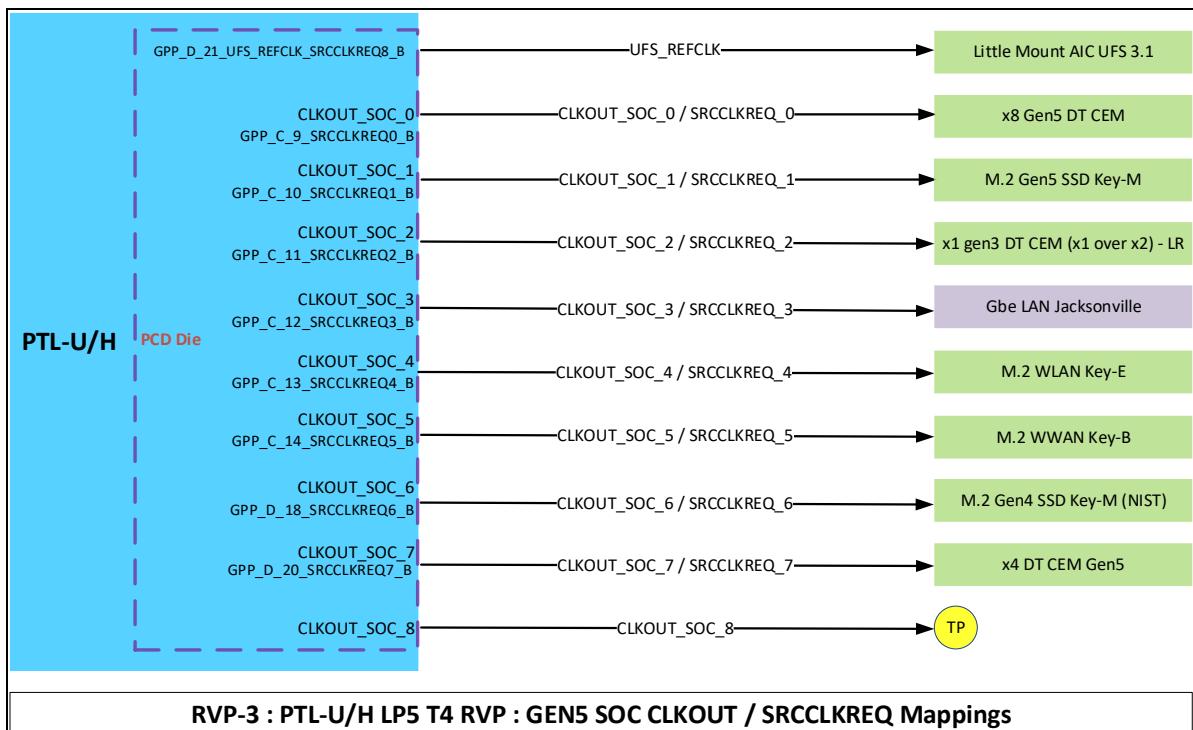


Figure 30 : RVP-3 : PTL-U/H LP5 T4 RVP : GEN5 SOC CLKOUT / SRCCCLKREQ Mappings

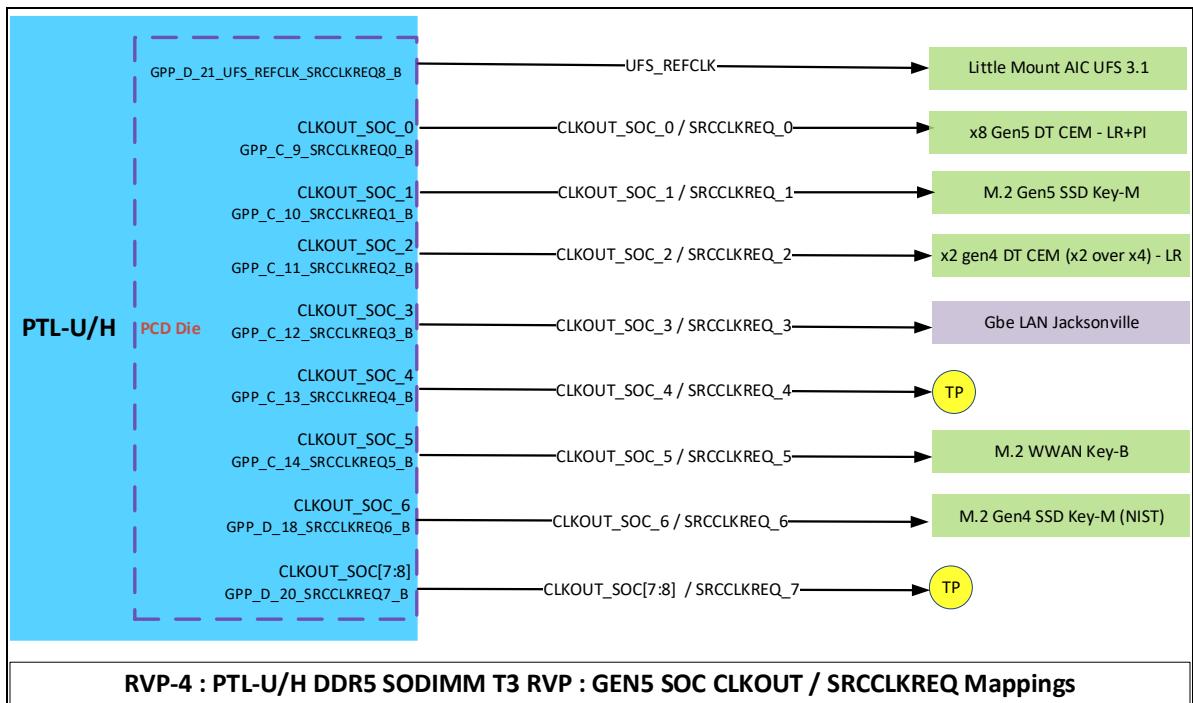


Figure 31 : RVP-4 : PTL-U/H DDR5 SODIMM T3 RVP : GEN5 SOC CLKOUT / SRCCCLKREQ Mappings

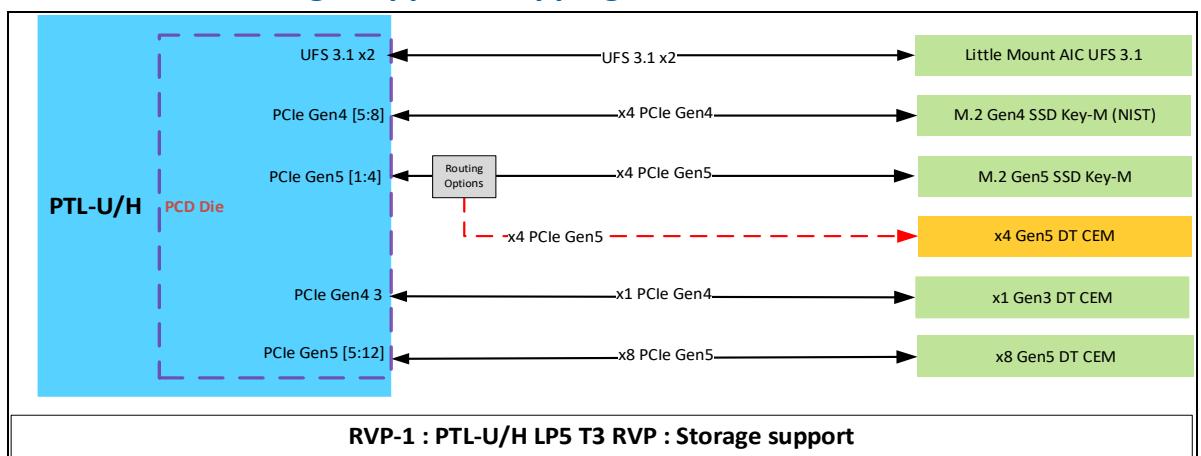
# 10 Storage

PTL-U/H supports different storage options whose high level block diagram & details are as below.

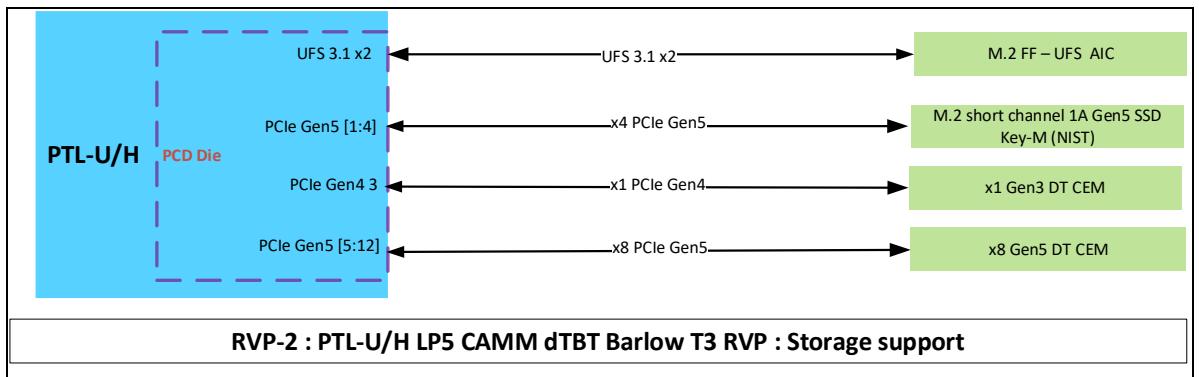
**Table 31: Storage options supported on PTL-U/H**

Sl. No	Interface	PTL-U/H RVP
1	PCIe NAND SSD	Share same M.2 2280 connector interfaced Modules
2	SD CARD over PCIe	Realtek PCIe to SD Card reader (Through PClex1 slot)
3	UFS (only in PTL-U)	Supported through Little mount AIC

## 10.1 PTL-U/H RVP : Storage support Mapping



**Figure 32 : RVP-1: PTL-U/H LP5 T3 RVP : Storage support high level block diagram**



**Figure 33 : RVP-2: PTL-U/H LP5 CAMM dTBT Barlow T3 RVP : Storage support**

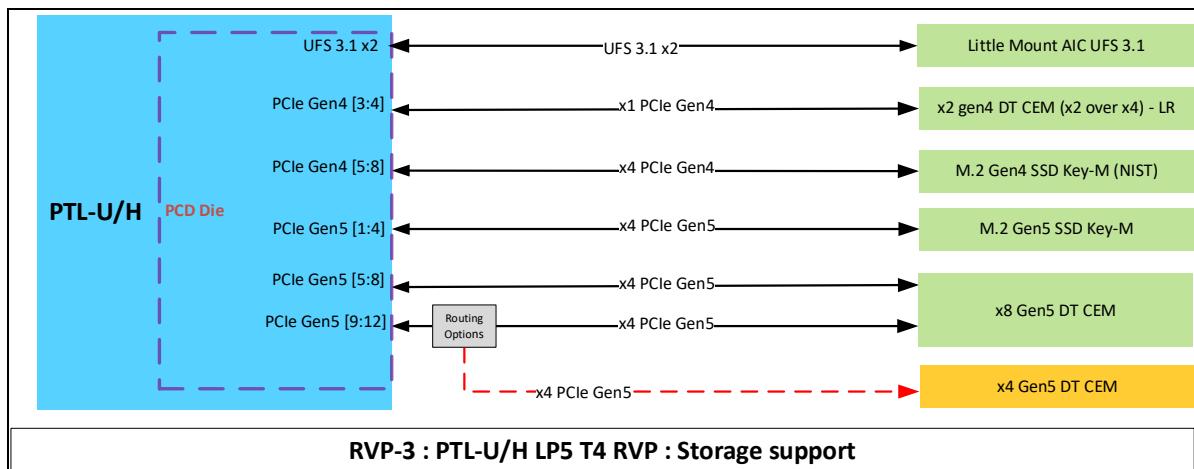


Figure 34 : RVP-3: PTL-U/H LP5 T4 RVP : Storage support

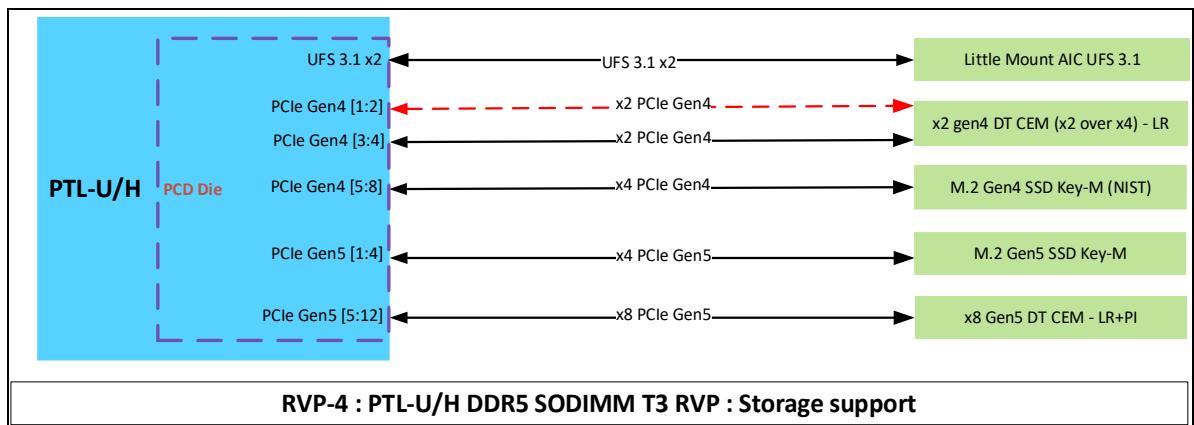


Figure 35 : RVP-4: PTL-U/H DDR5 SODIMM T3 RVP : Storage support

## 10.2

### M.2 Key-M Connector

PTL-U/H RVP's support M.2 SSD Key-M connectors following the PCI SIG M.2 spec. All the M.2 Key-M SSD ports will have RTD3 capability for PERST & WAKE signal coming from SOC.

#### 10.2.1

##### Dynamic M.2 Key-M SSD sideband GPIO voltage level switching (3.3V vs 1.8V)

PTL-U/H platform supports 1.8V IO level only. Platforms need level shifter to support legacy M.2 SSD modules with 3.3V sideband GPIO signaling. Upcoming M.2 modules are coming up with 2 configurations:

1. Support both 1.8V/3.3V sideband GPIO signal level
2. Support only 1.8V sideband GPIO signal level

For supporting both legacy & upcoming SSD modules, we need dynamic switching of sideband GPIO voltage level between 3.3V & 1.8V.

PTL-U/H RVP supports dynamic M.2 Key-M SSD sideband GPIO voltage level (3.3V vs 1.8V) switching.

- VIO\_CFG is a signal indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. It is output signal from M.2 Module. Sideband signaling is 3.3V when VIO\_CFG signals is low and NC when sideband signaling is 1.8V.

#### 10.2.2

#### Power Loss Notification (PLN) Support

A sudden loss of power can cause an SSD to lose user data in its volatile write cache & the 3 primary cause for power loss are:

- User presses & holds power button for more than power button overrise time (4s/ 10s/ Custom)
- Battery disconnected in case of notebooks & AC power loss in case of DT systems without UPS.
- Battery runs down.

This proposal will address first cause, the user turning off the power without going through the Windows shut-down process. It is proposed to connect Power Button signal passing through an Open Drain Buffer to M.2 SSD connector Pin 8 & a GPIO from EC to the same open drain buffer. This implementation will be on all the SKUs of the PTL-U/H RVPs.

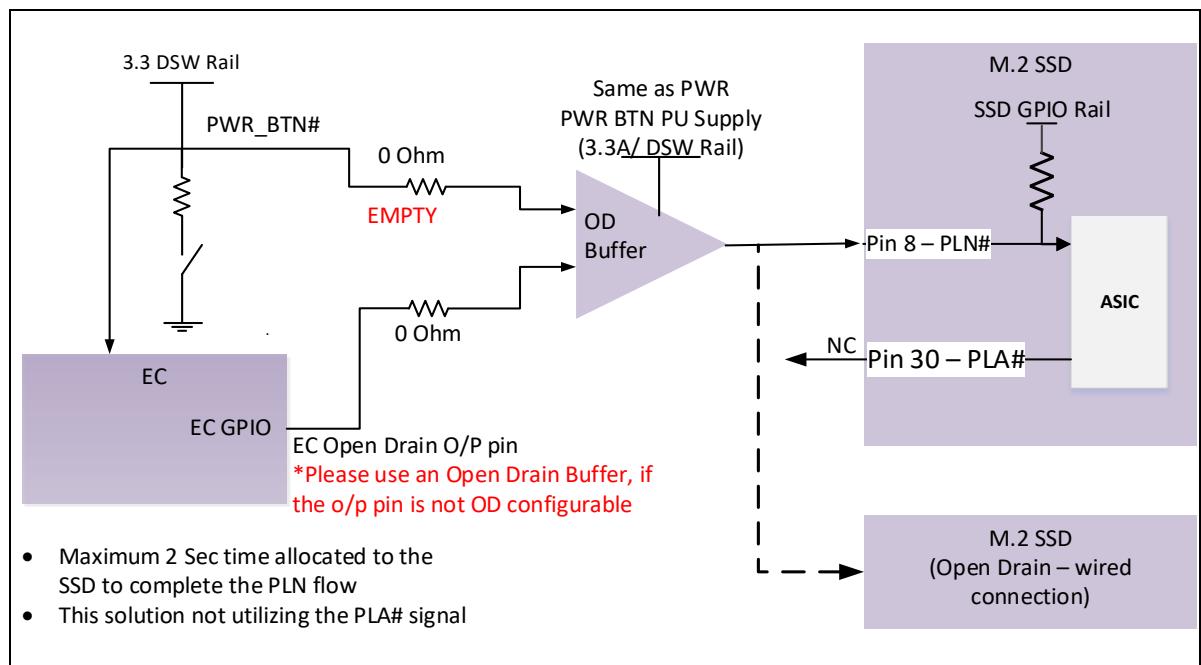


Figure 36: PLN circuit implementation

### 10.2.3

#### BIOS recovery architecture

NVMe BIOS recovery feature supports on SSD which is connected to PCIe Gen4 lane [5:8] in RVP-1,3,4 & to PCIe Gen5 lane [1:4] in RVP-2.

##### 10.2.3.1

###### SPI Descriptor Recovery

SPI Descriptor recovery in PTL-U/H is achieved by Descriptor verification (Detection) and recovery by the SPI controller in SOC. Since the Descriptor is required for any firmware to be loaded, it can't be recovered by firmware component.

SPI Descriptor are used in SPI FLASH to access control of the SPI FLASH regions to different masters & specify various properties of these regions. If a SPI-Descriptor gets corrupted the platform will not be bootable. To recover from SPI-Description corruption, the SPI flash will now contain 3 descriptors & the SPI controller in SOC is modified to read the subsequent descriptor if it finds a corrupted descriptor. This will enable the system to boot even in the presence of 2 corrupted descriptor.

There are 2 straps used for SPI Descriptor recovery, mentioned below:

**Table 32: SPI Descriptor Recovery Strap details**

GPIO Pin	Strap Details	Strap Functionality	Comment
GPP_H1	SPI FLASH Descriptor Recovery strap	0= Recovery Disable (Default) 1= Recovery Enable.	Weak Internal 20K PD, Sampled at RSMRSTB.
GPP_H2	SPI Flash Descriptor recovery source selection strap	0=Flash descriptor recovery internal source (Default) 1= Flash descriptor recovery external source	Weak Internal 20K PD, Sampled at RSMRSTB.

##### 10.2.3.2

###### NVMe Recovery

If the BIOS/CSME partition in the Flash is corrupted, this feature enables the EC to use an out of band mechanism (I2C/SMBUS) with the NVMe drive & rewrite the BIOS/CSME partition into SPI flash. This enables the system to boot in the presence of a corrupted BIOS partition in SPI-NOR. To support this feature, the following are implemented in the design,

- The firmware issue detection & recovery occur in pre-boot stage. Hence, EC and primary M.2 SSD shall be powered up and running before CPU/PCH is enabled.
- When NOT using the recovery mode, the SSD shall be power gated (off) in Sx.
- EC can override the SSD power while in Sx for the recovery.
- EC shall access M.2 SSD secondary partition over I2C/SMBus signals during recovery mode. Level translator is used to convert EC driven 3.3V I2C/SMBus signals to M.2 SSD 1.8V levels.
- EC shall have recovery indication signal (GPIO).
- Flash descriptor override strap is sampled at RSMRST in PTL-U/H silicon to enable CSME recovery in MAF mode. EC firmware needs to wait for 100ms before trying to access the SPI

flash after FDO strap is sampled high to prevent any conflicting case where SoC & EC both are trying to access SPI flash.

- EC Recovery indication GPIO should drive Flash descriptor override strap (Active high) of SOC as high to hold CSME communication with Flash Chip.
  - In MAF mode during BIOS/CSME recovery, platform power sequencing will be halted at SLP\_S3. This is because in MAF mode, for EC to access the SPI flash the eSPI & SPI interface needs to be alive & for that we need RSMRST to be high. So, we can't halt at RSMRST, so we halt at SLP\_S3 signal.
  - In G3/SAF mode during BIOS/CSME recovery, platform power sequencing will be halted at RSMRST. This is because in G3/SAF mode, EC can directly access the flash so we can halt at RSMRST also.

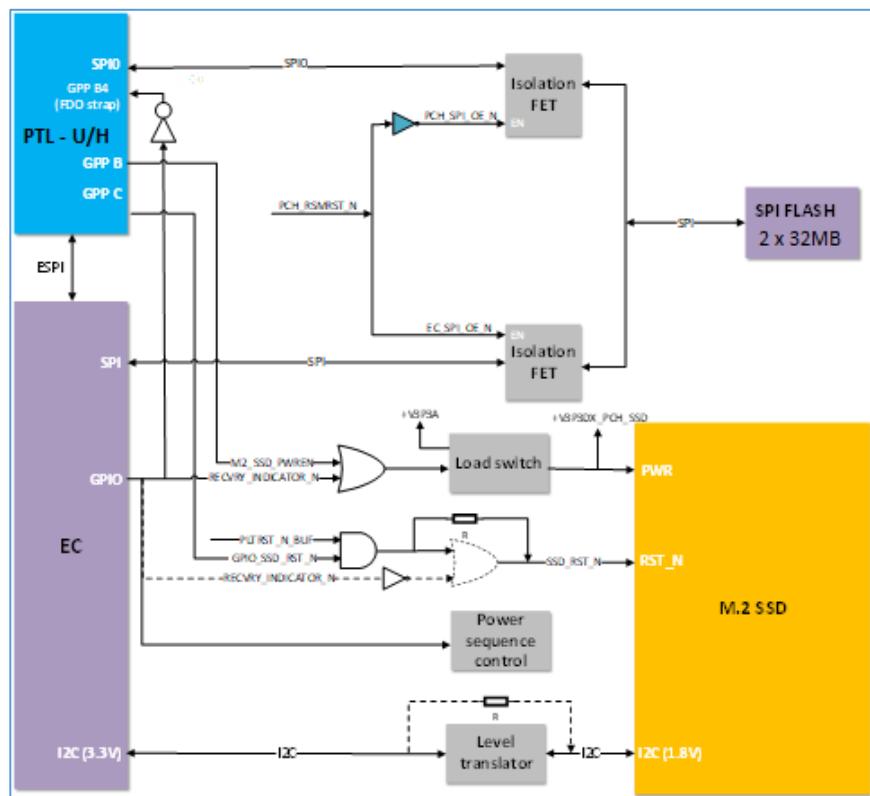


Figure 37: NIST193 Recovery Hardware implementation block diagram

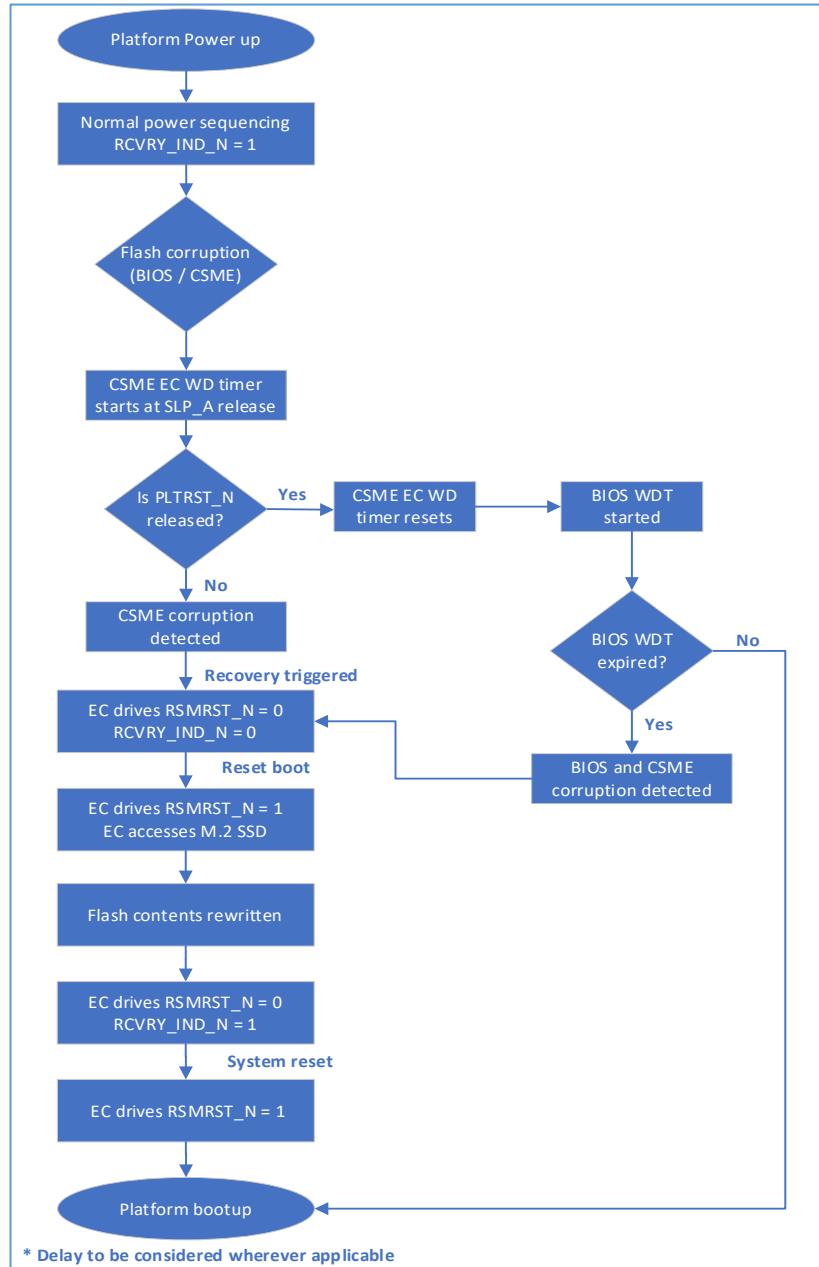


Figure 38: MAF Recommended Platform Flow

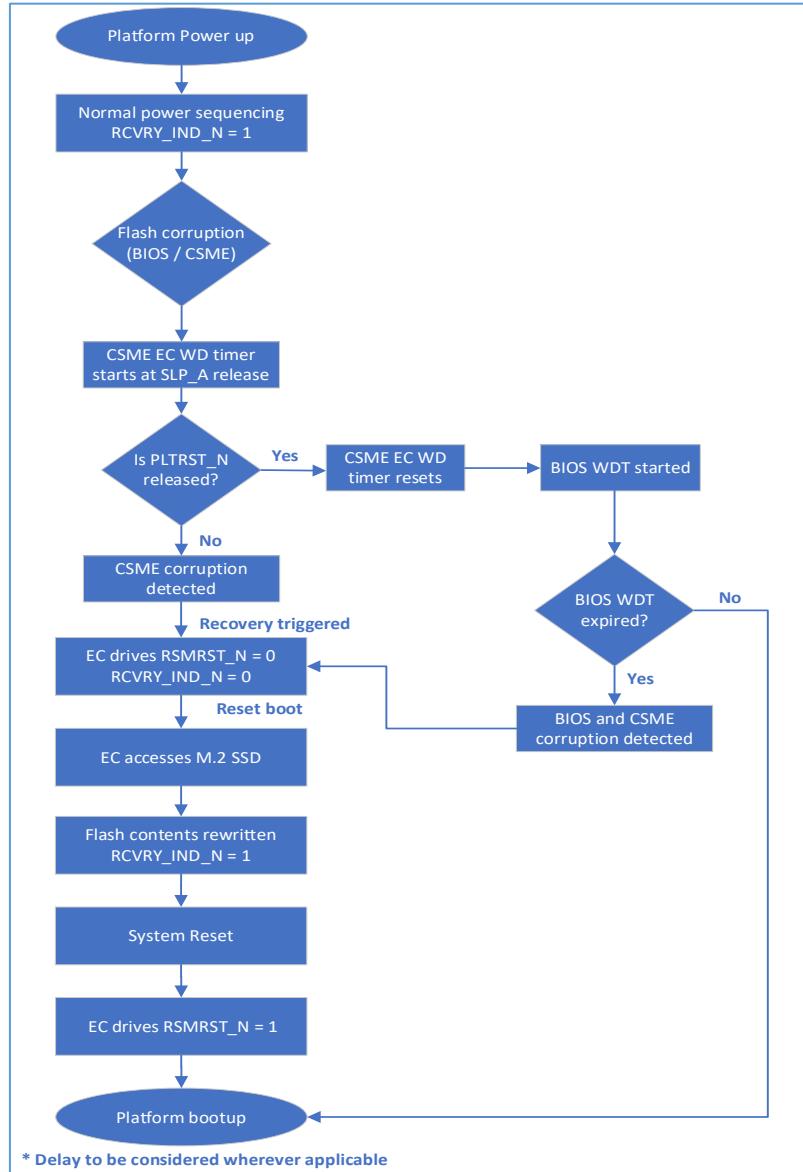


Figure 39: SAF/G3 Mode recommended Platform Flow

## 10.3

### SD card over PCIe DT CEM Slot

On the PTL-U/H RVP the PCIe to SD card interface is validated using the **Realtek RTS5261** SD4.2/7.0/8.0 PCIe to SD bridge IC based AIC & will be plugged on to x1 PCIe DT Slot.

Refer to the **WSIV Config sheet** for the latest information on PCIe to SD card used as part of the BKC support.

## 10.4

### UFS3.1

UFS 3.1 x2 Gear 4 is supported in PTL-U/H RVP. Little mount connector is used for UFS AIC plugging. UFS storage supported on all PTL-UH RVP SKU. UFS power rails work in S0/S0ix Platform state. No RTD3 support for UFS power rails. UFS two lanes fitted with CMC (EMC requirement) with bypass option. UFS device soldered on LM (Little mount) UFS AIC and UFS cards plugged on the B2B connector (IPN# E21540-001) provided on RVP.

**Note:** M.2 UFS is supported on CAMM SKU based on RVP CCB.

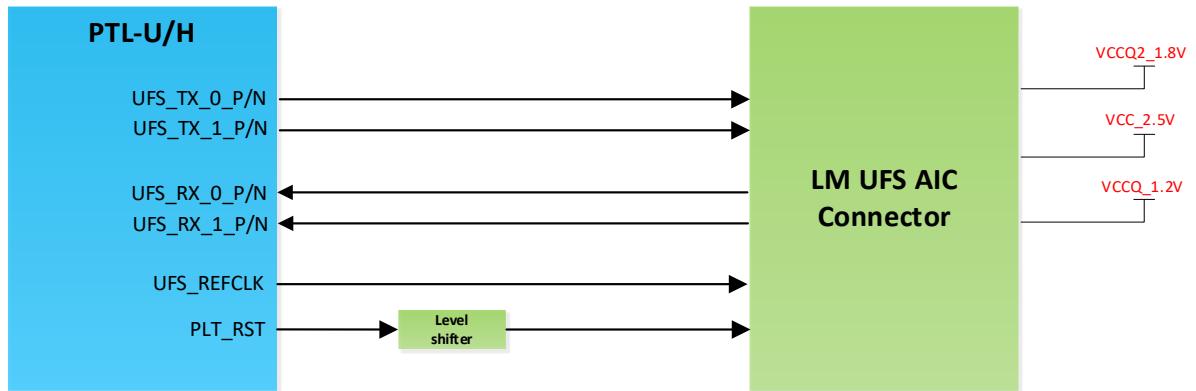


Figure 40: PTL-U UFS AIC CONN high level block diagram

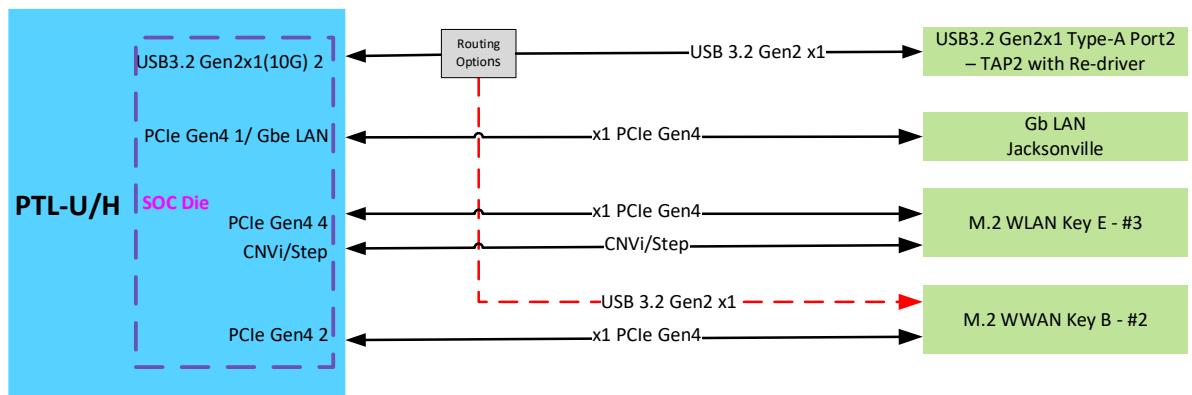
## 11 Connectivity

The primary connectivity interface for the PTL U/H RVP lies with the Chipset. The PTL U/H chipset supports integrated connectivity CNVi core which eliminates the need for an external WiFi chip. The other connectivity options are GbE LAN and WWAN. Table 33 gives the list of Modules supported on PTL U/H RVP SKUs as connectivity solutions.

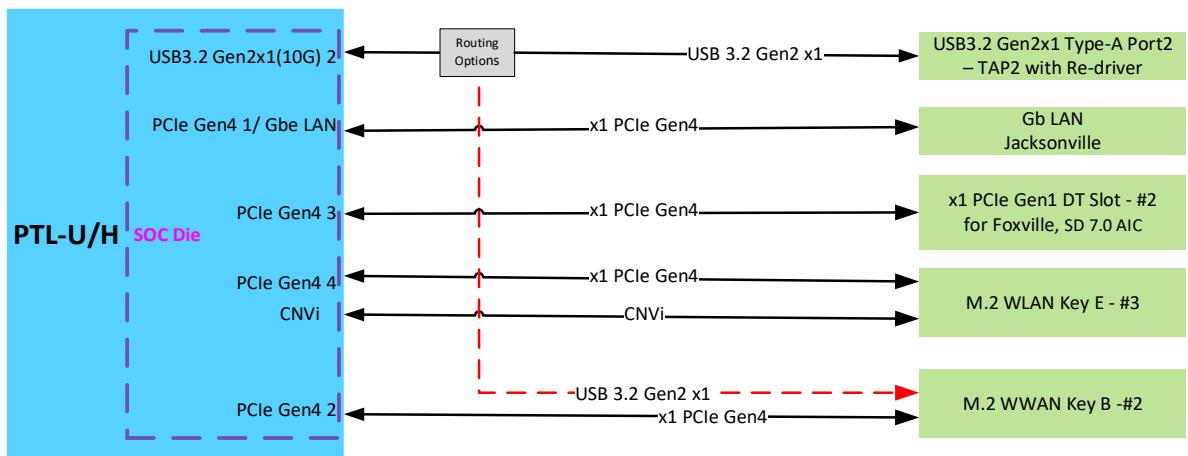
Note: In PTLU/H RVP there is no RTD3 support for both WLAN and WWAN and the corresponding load switches for enabling power is no longer supported.

**Table 33: Connectivity Support on PTL U/H RVP boards**

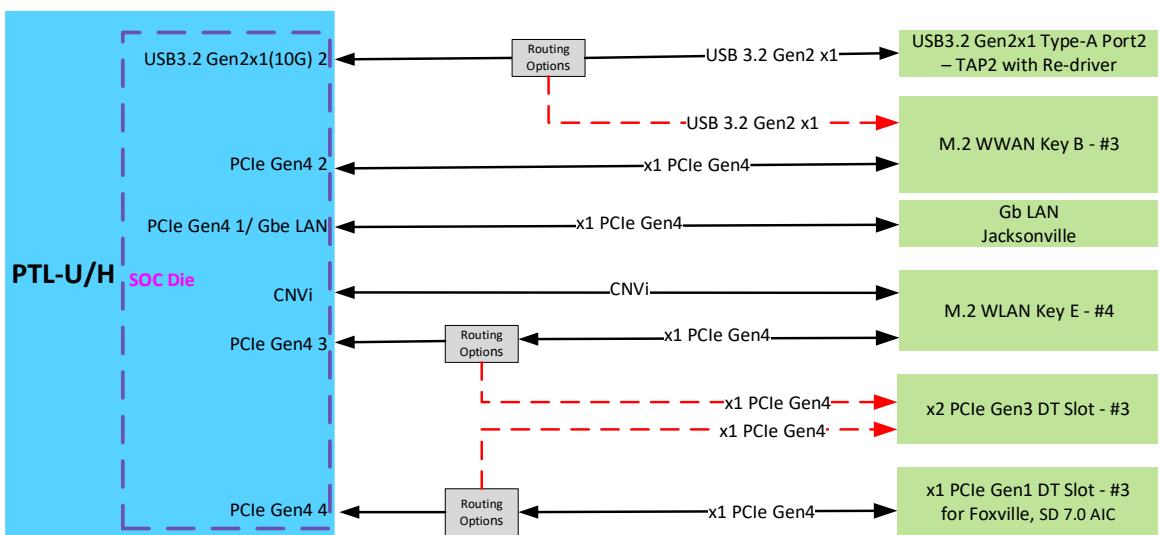
Interface Name	Module Name	Remarks
Integrated CNVio	Whale peak 2, Spider Peak 2, Garfield Peak 2, Filmore Peak 2	M.2 Key E Socket 3
Discrete WLAN+BT	Gale peak 2	M.2 Key E Socket 3
WWAN	Maple spring FM350-GL (5G Module)	M.2 Key B Socket 2
Gbe LAN	Jacksonville (device down)	RJ-45 Jack
Gbe LAN	Fox-Ville Add-In Card	x1 PCIe AIC



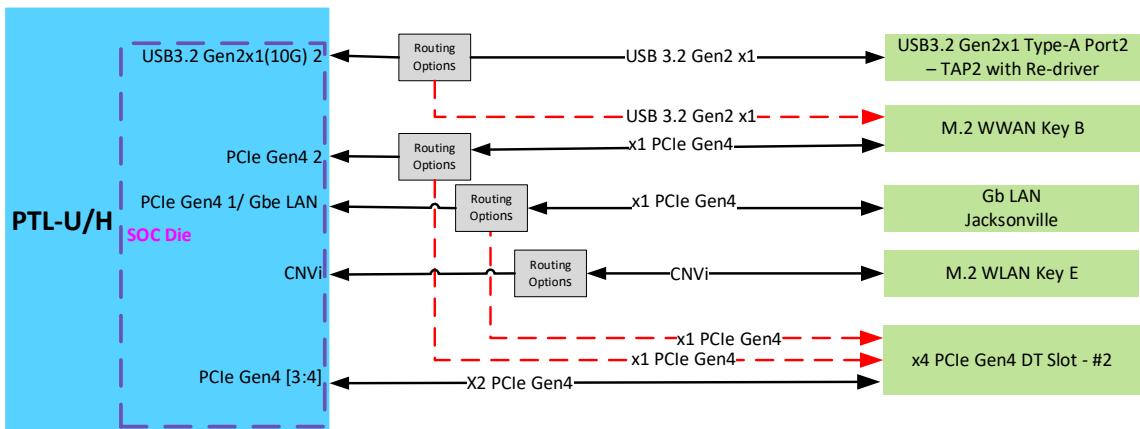
**Figure 41 : RVP-1: PTL-U/H LP5 T3 RVP Connectivity Block Diagram**



**Figure 42 : RVP-2: PTL-U/H LP5 CAMM dTBT Barlow T3 RVP Connectivity Block Diagram**



**Figure 43: RVP-3 : PTL-U/H LP5 T3 RVP Connectivity Block Diagram**



**Figure 44: RVP-4: PTL-U/H DDR5 SODIMM T3 RVP Connectivity Block Diagram**

## 11.1

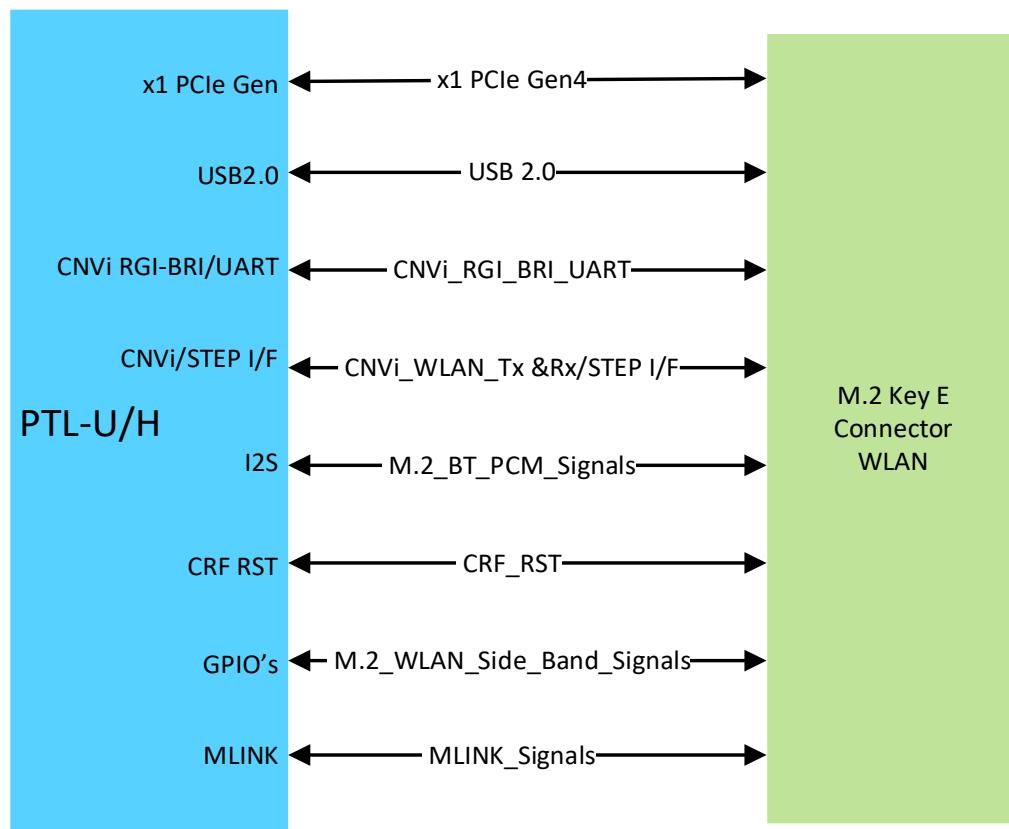
### Connectivity Integration (CNVi)

The RVP supports a M.2 Hybrid Key E slot for Wireless connectivity solutions, it supports a Combo WiFi + BT M.2 module. The Wi-Fi interfaces are over integrated CNVi or x1 PCIe port while the Bluetooth connectivity is supported over CNVi, USB2 or UART+I2S interfaces based on modules is getting plugged in.

Connectivity integration (CNVi) is a general term referring to a family of connectivity solutions which are based on the hard macro (Magnatar) embedded within Intel Silicon. Besides the Magnatar, the CNVi contains an external RF companion module (CRF) and RF antennas. This module will be implemented as a M.2 (2230) module solution on PTL-U/H RVP. The RF companion will be Whale Peak 2, Filmore Peak 2, Garfield Peak based M.2 Key E module with provision for connecting the external RF antennas.

For Integrated WiFi and Bluetooth, CNVi DPHY TX/RX, STEP I/F/CNVio gen2 and RGI/BRI signals are used respectively. For discrete WiFi x1 PCIe is used and for discrete Bluetooth-USB2.0 and UART signals are used.

In the below diagram, all necessary signals from PTL U/H to the M.2 Key E connector has been shown.



**Figure 45: PTL U/H RVP M.2 Key E WLAN implementation high level block diagram**

**Table 34: Interface Details for WLAN Module**

Description	Interface Name/ Signal Name	Support on PTL U/H RVP
WIFI	<ul style="list-style-type: none"> <li>• CNVi DPhy &amp; STEP</li> <li>• PCIe</li> <li>• CLINK(CSME)</li> </ul>	Yes
BT DATA	<ul style="list-style-type: none"> <li>• USB2.0,</li> <li>• BRI</li> </ul>	Yes
WLAN M.2 Control	<ul style="list-style-type: none"> <li>• RGI</li> <li>• RF_RESET#</li> <li>• WIFI_RFKILL#</li> <li>• BT_RFKILL#1</li> <li>• WLAN_LED#</li> <li>• BT_LED#</li> </ul>	Yes
BT AUDIO	<ul style="list-style-type: none"> <li>• PCM</li> </ul>	Yes
RF Coexistence	<ul style="list-style-type: none"> <li>• UART_RX</li> <li>• UART_TX</li> <li>• UART supports Real-Time Coexistence</li> </ul>	Yes

### 11.1.1

#### M.2-1A Key E Connector

Next generation WLAN modules need more power to meet performance and feature targets. M.2 specification is restricting these features due to the limited current supply (2.5A) allowed in the connector specification.

The new M.2-1A connector will support 1A per pin, with 4pin it will support 4A. New mechanical key allowing current M.2 and New M.2-1A insertion but not allow M.2-1A to work in old M.2 connectors.

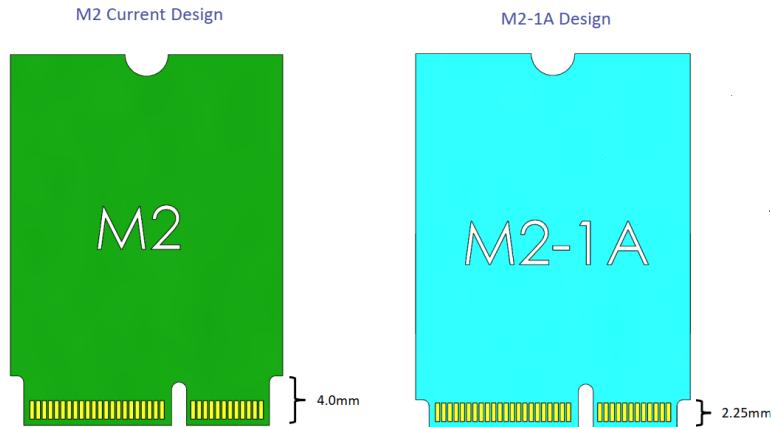
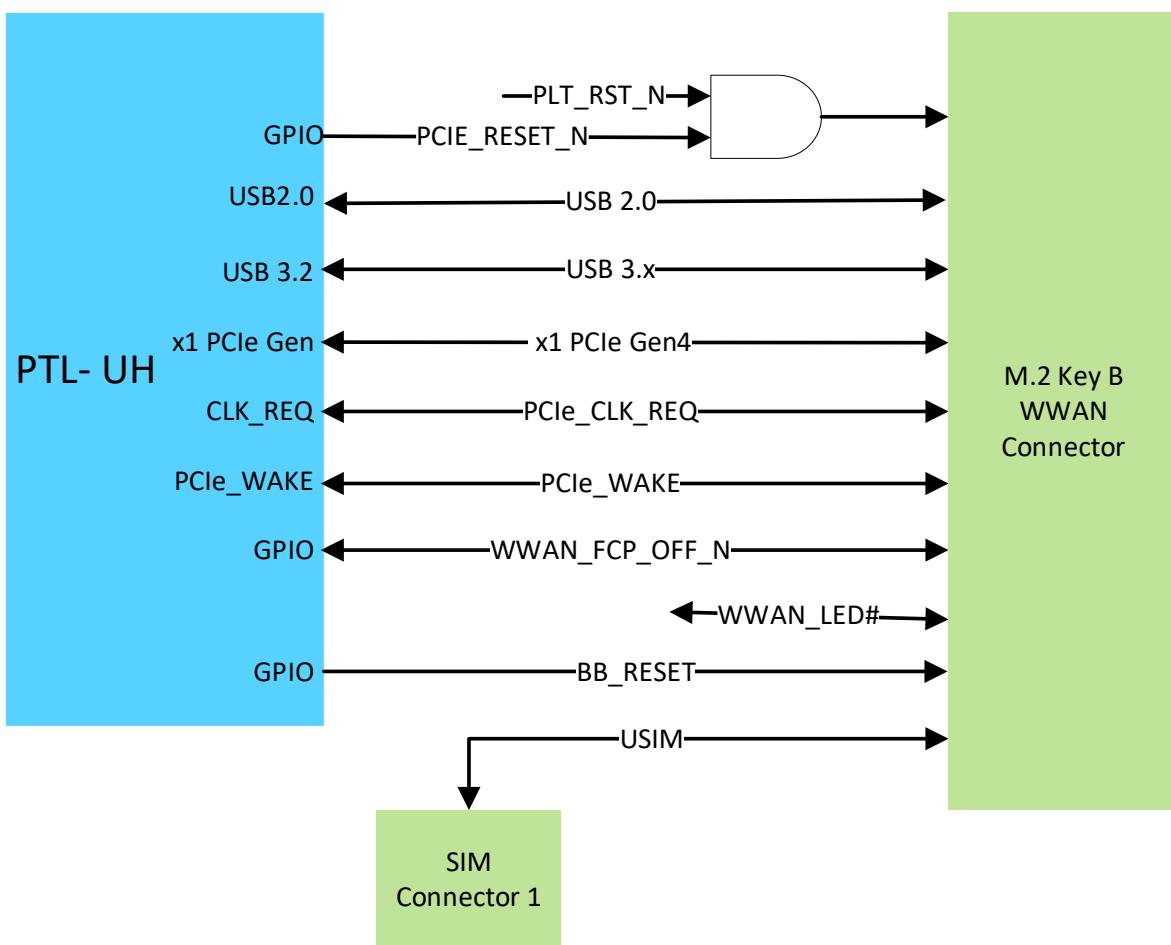


Figure 46: New M.2-1A design

### 11.2

#### WWAN M.2 Module

PTL-U/H RVP supports M.2 30X52 Socket 2 WWAN module. Single PCIe lane, x1 interface, and USB2.0 interface is routed to M.2 WWAN Key B connector. The USB 2.0 interface is used only during the production testing and debugging activities. Figure 40 below shows the interface connectivity of WWAN Module to PTL -U/H.



**Figure 47: PTL-U/H RVP M.2 Key-B WWAN implementation high level block diagram**

Further details on SIM Card Signals, Module WAKE and Reset etc. are listed in below table.

**Table 35: Interface Details for WWAN Maple spring FM350-GL(5Gmodule)**

Description	Interface Name/ Signal Name	Support on PTL-UH RVP
<b>Inter-processor Communications</b>	<b>PCIe USB 2.0</b>	<b>Yes</b>
<b>USIM with Card Detect</b>	<b>SIM_CLK, SIM_RESET, SIM_IO, SIM_PWR, SIM_DETECT</b>	<b>Yes</b>
<b>WWAN M.2 Control</b>	<b>FULL_CARD_POWER_OFF# RESET# PERST# W_DISABLE# LED#1 DPR (Body SAR)</b>	<b>Yes</b>

<b>Global Positioning (GPS/GLONASS)</b>	<b>TX_BLANKING, FINE_TUNE_AIDING (FTA)</b>	<b>Yes</b>
<b>CSME</b>	<b>I2C</b>	<b>No</b>
<b>RF Coexistence</b>	<b>UART_RX UART_TX UART supports Real-Time Coexistence</b>	<b>No</b>

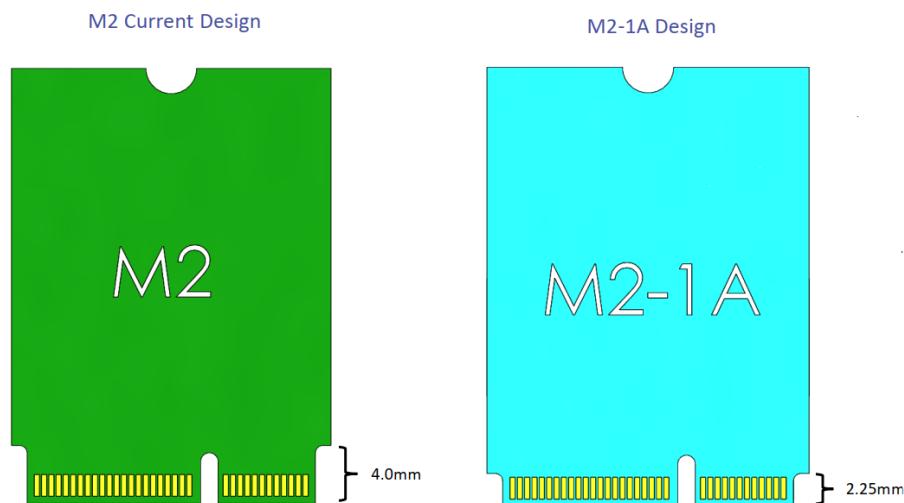
An LED is used to provide status indications to users via system provided indicators. LED#1 is an active low open drain output signal intended to drive system-mounted LED.

**Table 36: LED Indicator description for WWAN**

<b>State</b>	<b>Definition</b>	<b>WWAN State</b>
<b>OFF</b>	<b>The LED is emitting no light</b>	<b>Not powered</b>
<b>ON</b>	<b>The LED is emitting light in a stable non-flashing state</b>	<b>Powered registered but not transmitting or receiving</b>
<b>BLINKING</b>	<b>State Blinking</b>	<b>TX / RX activity in progress</b>

#### 11.2.1 M.2-1A Key B Connector

Next generation WWAN modules need more power to meet performance and feature targets. M2 specification is restricting these features due to the limited current supply (2.5A) allowed in the connector specification. The new M.2-1A connector will support 1A per pin (Total 5A). New mechanical key allowing current M.2 and New M.2-1A insertion but not allow M.2-1A to work in older M.2 connectors.



**Figure 48: New M.2-1A design**

## 11.3

### GbE LAN

PTL RVP supports Wired Gigabit Ethernet interface through on-board Intel 1000Base-T PHY LAN Controller I219 (Jacksonville) that connects to PCH through an x1 PCIe interface. The LAN PHY operates in Gen1 PCIe mode.

2.5G Base-T MAC/PHY LAN Controller I225 (Foxville) based wired Ethernet will be validated through AIC. SMLink would be provided for the Foxville AIC.

The LED indications for connectivity status of GbE LAN are listed in table below.

**Table 37: LED definition for RJ45 Connector**

LED Function	State Description
Speed	<b>OFF: 10Mbps</b> <b>GREEN: 100Mbps</b> <b>YELLOW: 1Gbps</b>
Activity	<b>GREEN: Link is up there no activity on the lines</b> <b>GREEN BLINKING: Tx / Rx or both Activity on the lines</b>

RVP supports standard x4 PCI express desktop slots from SOC which can be used to plug-in a x1 or x4 Network Interface Cards for enabling the validation of third-party connectivity solutions.

#### 11.3.1

### Jackson Ville Controller

The Ethernet Connect I219 is a single-port Gigabit Ethernet Physical Layer Transceiver. It connects to an integrated Media Access Controller (MAC) through a dedicated interconnect.

- I219 supports operation at 10/100/1000 Mb/s data rates.
- Provides IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications.
- Support for the Energy Efficient Ethernet (EEE) 802.az specification.
- IEEE 802.3u auto-negotiation conformance
- Supports carrier extension (half duplex)
- 802.1as/1588 conformance
- No support for Gb/s half-duplex operation
- Intel® vPro support with appropriate Intel chipset components.
- Ultra-Low Power at cable disconnect (<1 mW) enables platform support for connected standby.
- PCIe-based interface for active state operation (S0 state)
- SMBus-based interface for host and management traffic (Sx low power state)

#### 11.3.2

### Foxville Controller

The Intel® Ethernet Controller I225 (I225) is a single-port, compact, low power Gigabit Ethernet (GbE) controller. It is a fully integrated GbE Media Access Control (MAC) and Physical Layer (PHY) device, offering 10/100/1000/2500 Mb/s data rates. The interface-to-host system is a one lane PCI Express\* (PCIe\*) Gen 2 version 2.1

- 802.1q VLAN support
- 802.3az EEE support
- Support for AMT / Intel® vPro™ Technology
  - Host onboard & Dock
  - Intel Stable Image Platform Program (SIPP™) support
- Automatic polarity correction
- Network proxy/ARP Offload
- MDC/MDIO management interface
  - MDI Lane Swap design support
- Smart speed operation for automatic speed reduction on faulty cable plants
- Power Optimizer Support

On the PTL-U/H RVP the Foxville controller is validated by using the Foxville AIC plugged on to x1 PCIe DT Slot

## 12 Audio

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PTL-UH RVP enables value system with single-chip audio solution. On board codec upgraded to ALC722-CG [SDCA 0.8] compliant soundwire based codec which can be configured in SNDW3 multilane or SNDW1 single lane mode. Refer [ALC722 CODEC](#) section for more detail.

RVP supports different audio codecs validation through add-in-card solution. Realtek AIOC GEN6 is the POR AIC for PTL-UH & Cirrus AIC v3 will support delta validation configuration and existing Realtek AIOC GEN3 to support HDA [ALC245] validation. Refer [AUDIO AIC](#) section for more detail.

**Figure 49: PTL-UH RVP Audio interface landing zone details**

RVP SKU's	RVP Feature
<b>RVP 1: PTL U/H LP5 Memory Down (7500Mbps) T3 PCB-Base SKU</b>	<b>Audio Options-</b> 1. Full Function ALC722 Codec Solder Down 2. Audio HDR - JA (HDA/I2S Codec Support) 3. Audio HDR - JD (DMIC support) 4. Audio HDR - JE (SNDW Codec support) 5. Power HDR - JH (Additional PWR support) 6. Audio HDR – JS (Codec DMIC & SPKR support) 7. I2S2 to M.2 Key-E for BT
<b>RVP 2: PTL U/H – T3 PCB - dTBT Barlow – LP5 CAMM (7500Mbps)</b>	
<b>RVP 3: PTL U/H - T4 PCB- LP5 Memory Down (8533Mbps)</b>	
<b>RVP 4: PTL U/H - T3 PCB - DDR5 SODIMM (7200Mbps)</b>	

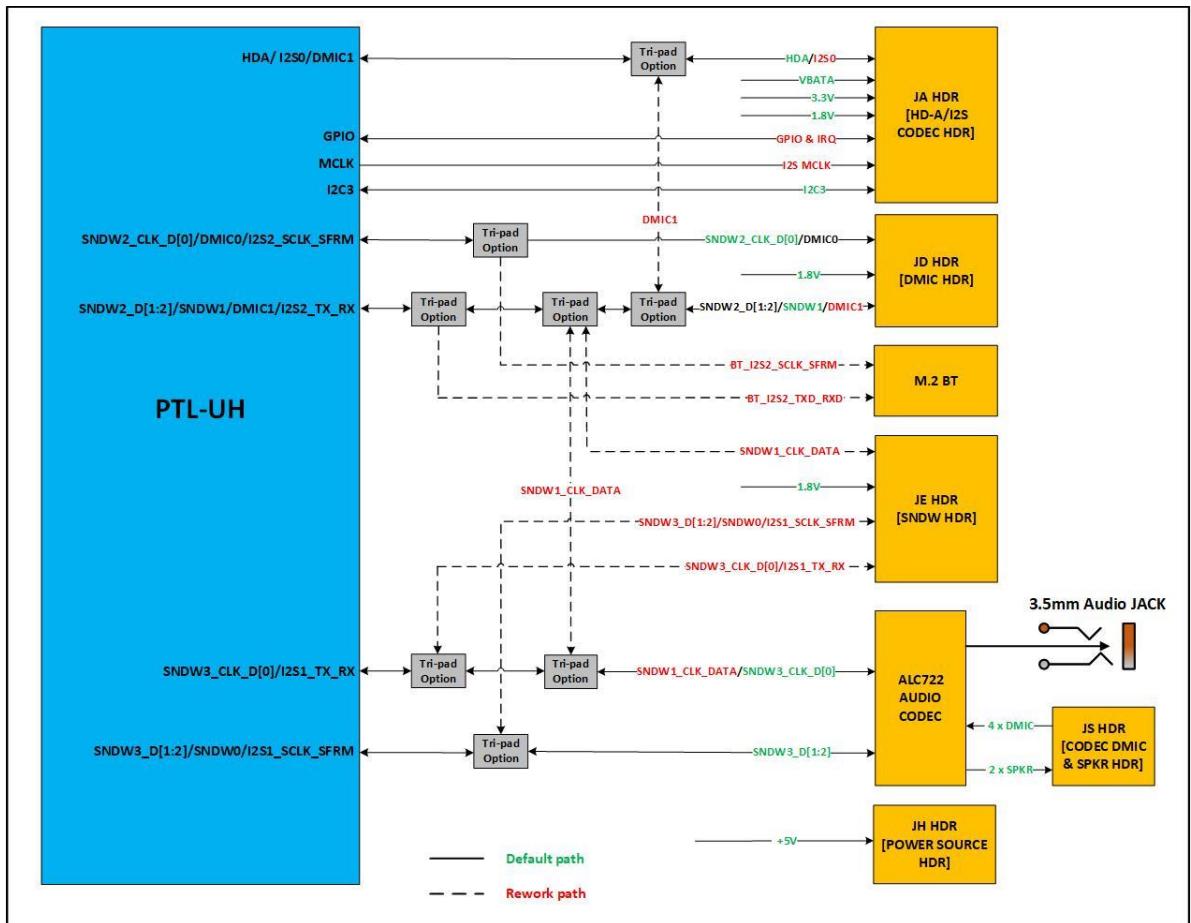


Figure 50: PTL-UH RVP Audio high level block diagram

## 12.1 ALC722 SNDW on-board CODEC

The ALC722-CG is compliant to SDCA v0.8[MIPI04], where SDCA stands for SoundWire Device Class for Audio architecture that standardizes the interface for software to control the audio function through a SoundWire interface.

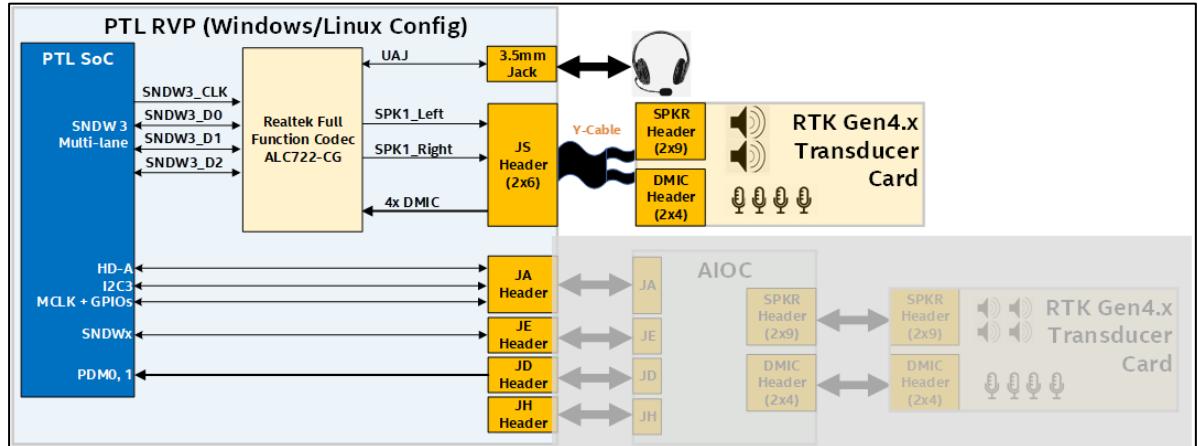
- The ALC722 integrates a headphone amplifier can drive 15-ohm headphone & supports legacy Universal Audio Jack.
- An integrated stereo Class-D amplifier directly drives the speakers. The Class-D amplifier is designed to drive speakers with as low as 4Ω impedance. Its maximum output power is 2.8W per channel at 5V power supply. The advantage of an integrated Class-D amplifier in the ALC722 is high efficiency with lower power consumption.
- The ALC722 has two stereo digital microphone inputs.

PLT-UH RVP enables dedicated 12-pin header [JS] on RVP to connect Realtek Gen4.x transducer card for this on-board configuration using a Y-cable solution as shown below.

- SNDW3 multilane connects to ALC722 codec by default, SNDW1 single lane can be enabled with a rework option.

-Realtek GEN4.x card (same as existing GEN 3.1 transducer card) supports 4xDMIC's and 2x SPKR assembly. PLT-UH LP5x ERB

**Figure 51: PTL-UH RVP Audio ALC722 on-board configuration**



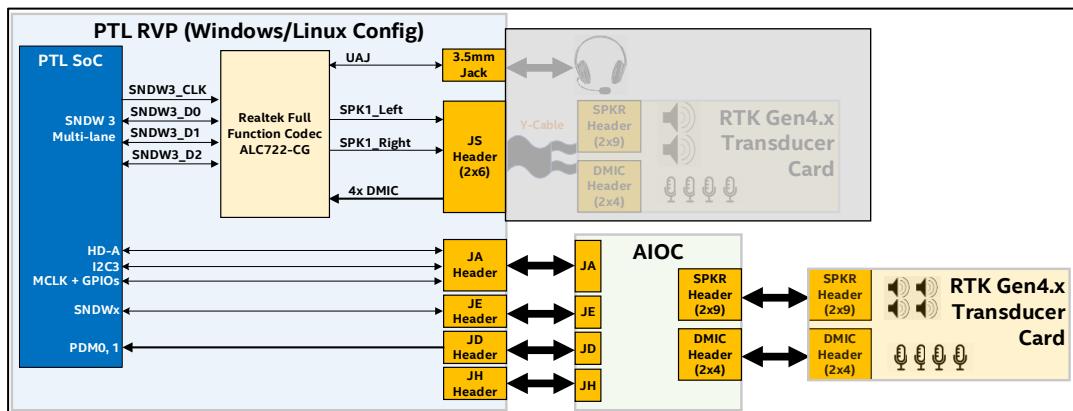
## 12.2

### AUDIO AIC Validation Configuration

PTL-UH RVP supports below new AIOC (All-in-One Card) with SDCA 1.0 components.

- Realtek AIOC Gen6 (Golden Config)
- Realtek AIOC Gen3 (Delta Config)
- Cirrus AIOC v3 (3\* Delta Config)

**Figure 52: PTL-UH RVP Audio Windows/Linux [non-BT] configuration**



**Note:** BT-audio offload support via I2S2 port can be enabled only through resistor rework option on RVP.

Refer below table for AIOC supported CODECs versus validation configuration details.

**Figure 53: PTL-UH RVP Audio Windows/Linux build validation configuration table**

Val. Config	AIOC	Driver	Components			I/Os	Notes
			Full Function Codec (UAJ, DMIC, Spk Out)	Jack Codec (UAJ, DMIC)	SmartAmp		
GC (5*)	RTK AIOC Gen6	SNDW ACX	1x ALC712-VB	-	1x ALC1320	<ul style="list-style-type: none"> <li>• 3.5mm UAJ (Hi-Z HP)</li> <li>• 4x speaker (aggregated to stereo)</li> <li>• 4Ch DMIC (ALC712 attached)</li> </ul>	<ul style="list-style-type: none"> <li>• Speaker protection supported by all AMPS</li> <li>• Hi-impedance HP Out</li> <li>• Hi-Res audio up to 192kHz in hardware</li> </ul>
4*-1	RTK AIOC Gen3	HD-A portCl.	1x ALC245	-	-	<ul style="list-style-type: none"> <li>• 1x 3.5mm UAJ</li> <li>• 2x speakers</li> <li>• 4ch DMIC (PCH attached)</li> </ul>	<ul style="list-style-type: none"> <li>• Supported for legacy designs</li> <li>• PCH attached DMIC</li> </ul>
4*-2	N/A	SNDW ACX	1x ALC722-CG	-	-	<ul style="list-style-type: none"> <li>• 1x 3.5mm UAJ</li> <li>• 2x speaker (Class D, simple power limit)</li> <li>• 2/4ch DMIC (ALC722 attached)</li> </ul>	<ul style="list-style-type: none"> <li>• Additional Restackable Jack not supported</li> </ul>
4*-3	RTK AIOC Gen6	SNDW ACX	-	1x ALC713-VB	2x ALC1320	<ul style="list-style-type: none"> <li>• 3.5mm UAJ (Hi-Z HP)</li> <li>• 4x speakers (aggregated to stereo)</li> <li>• 4Ch <u>ALC713-VB attached</u></li> </ul>	<ul style="list-style-type: none"> <li>• Speaker protection supported by all AMPS</li> </ul>
3*-1	Cirrus AIC v3	SNDW ACX	1x Cohen (CS42L43)	-	6x Jamerson (CS35L56)	<ul style="list-style-type: none"> <li>• 1x 3.5mm UAJ</li> <li>• 6x speakers (aggregated to stereo)</li> <li>• 2ch DMIC via Cohen</li> </ul>	<ul style="list-style-type: none"> <li>• AIOC v3 is required to meet PTL RVP compatibility</li> </ul>
3*-2	TI AIOC Gen1	SNDW ACX	1x TAC5682	-	2x TAS2880 (Stereo)	<ul style="list-style-type: none"> <li>• 1x 3.5mm UAJ (Hi-Z HP)</li> <li>• 6x speakers (aggregated to stereo)</li> <li>• 4ch DMIC via codec</li> </ul>	<ul style="list-style-type: none"> <li>• Placeholder and pending for CCB. Onboard codec to be used until CCB approves.</li> </ul>
3*-3	RTK AIOC Gen3	HD-A portCl.	1x ALC245	-	-	<ul style="list-style-type: none"> <li>• 1x 3.5mm UAJ</li> <li>• 2x speakers</li> <li>• 4ch DMIC (ALC245 attached)</li> </ul>	<ul style="list-style-type: none"> <li>• Supported for legacy designs</li> <li>• DMIC attached to ALC245</li> <li>• No rework needed on RVP</li> </ul>

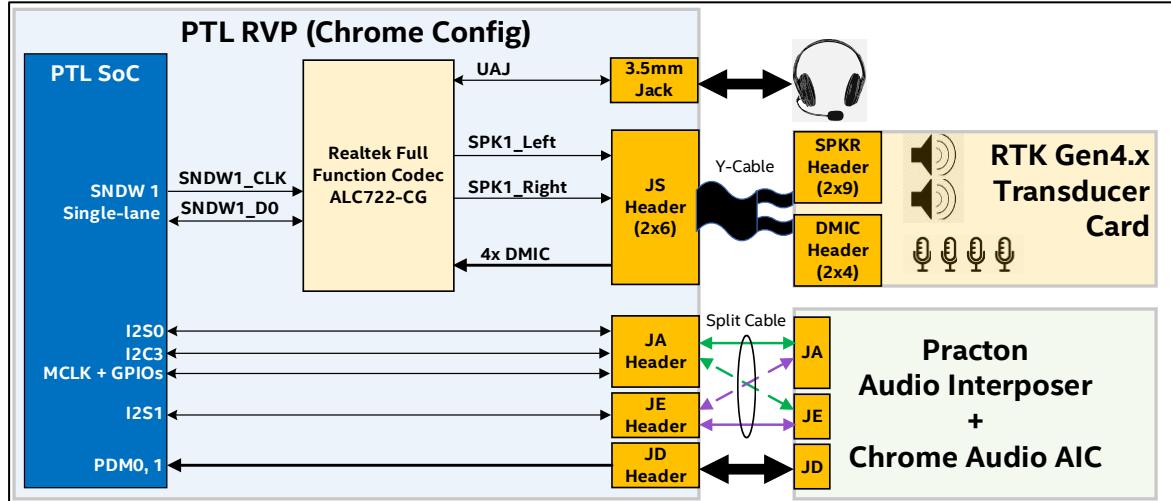
PTL-UH RVP CHROME sku supports following validation use-cases, without need for any resistor rework

- I2S config using Pranton Audio Interposer (+ Chrome Audio AIC):
  - Codec (JA – I2S0) + Amp (JE – I2S1) + DMIC (JD – PDM0,1)
  - Dedicated GPIO for Codec\_IRQ.
- SNDW config using on-board codec ALC722-CG
  - SNDW1 single lane configured by default. SNDW3 Multilane can be chosen in future with resistor stuff/un-stuff.

**Figure 54: PTL-UH RVP Audio CHROME SoC pin configuration**

	Chrome
xxgpp_d_9_i2s_mclk1_out	
xxgpp_d_10_hda_bclk_i2s0_sclk_hdacpu_bclk	I2S0
xxgpp_d_11_hda_sync_i2s0_sfrm	
xxgpp_d_12_hda_sdo_i2s0_txd_hdacpu_sdo	
xxgpp_d_13_hda_sdi_0_i2s0_rxd_hdacpu_sdi	
xxgpp_d_16_hda_RST_B_dmic_clk_a_1	PDM1
xxgpp_d_17_hda_sdi_1_dmic_data_1	
xxgpp_s_0_sndw3_clk_i2s1_txd	I2S1
xxgpp_s_1_sndw3_data0_i2s1_rxd	
xxgpp_s_2_sndw3_data1_sndw0_clk_dmic_clk_a_0_i2s1_sclk	
xxgpp_s_3_sndw3_data2_sndw2_data1_sndw0_data0_dmic_data_0_i2s1_sfrm	
xxgpp_s_4_sndw2_clk_dmic_clk_a_0_i2s2_sclk	PDM0
xxgpp_s_5_sndw2_data0_dmic_data_0_i2s2_sfrm	
xxgpp_s_6_sndw2_data1_sndw1_clk_dmic_clk_a_1_i2s2_txd	
xxgpp_s_7_sndw3_data3_sndw2_data2_sndw1_data0_dmic_data_1_i2s2_rxd	SNDW1

Figure 55: PTL-UH RVP Audio AIC CHROME build validation configuration



## 12.3 RVP Audio Headers

PTL-UH silicon supports only 15 audio functionality pins. SoC muxing consideration is driven by CCG Platform team (comprising of Audio Domain Architects, as well as Platform EIO stakeholders) to balance between total GPIO pins needed/reserved for Audio while meeting primary requirements for the different segments (Windows, Chrome, IOT, etc). Pin muxing with reduced pin count for the PTL-UH SoC is shown in the below table.

Table 38: PTL-UH Audio pin muxing

SoC Pin Name	SoundWire 3	SoundWire 2	SoundWire 0/1	DMIC	I2S / PCM	HD-A
GPP_D_10_HDA_BCLK_I2S0_SCLK_HDACPU_BCLK					I2SSCLK[0]	HDA_BCLK
GPP_D_11_HDA_SYNC_I2S0_SFRM					I2SSFRM[0]	HDA_SYNC
GPP_D_12_HDA_SDO_I2S0_TXD_HDACPU_SDO					I2STXD[0]	HDA_SDO
GPP_D_13_HDA_SDIO_I2S0_RXD_HDACPU_SDIO					I2SRXD[0]	HDA_SDIO
GPP_D_16_HDA_RST_B_DMIC_CLK_A_1				DMIC_CLKA[1]		HDA_RST#
GPP_D_17_HDA_SDIO_1_DMIC_DATA_1				DMIC_DATA[1]		HDA_SDIO1
GPP_D_9_I2S_MCLK1_OUT					I2SMCLK[0]	
GPP_S_0_SNDW3_CLK_I2S1_TXD	SNDW_CLK[3]				I2STXD[1]	
GPP_S_1_SNDW3_DATA0_I2S1_RXD	SNDW_DATA[3][0]				I2SRXD[1]	
GPP_S_2_SNDW3_DATA1_SNDW0_CLK_DMIC_CLK_A_0_I2S1_SCLK	SNDW_DATA[3][1]		SNDW_CLK[0]	DMIC_CLKA[0]	I2SSCLK[1]	
GPP_S_3_SNDW3_DATA2_SNDW2_DATA1_SNDW0_DATA0_DMIC_DATA_0_I2S1_SFRM	SNDW_DATA[3][2]	SNDW_DATA[2][1]	SNDW_DATA[0]	DMIC_DATA[0]	I2SSFRM[1]	
GPP_S_4_SNDW2_CLK_DMIC_CLK_A_0_I2S2_SCLK		SNDW_CLK[2]		DMIC_CLKA[0]	I2SSCLK[2]	
GPP_S_5_SNDW2_DATA0_DMIC_DATA_0_I2S2_SFRM		SNDW_DATA[2][0]		DMIC_DATA[0]	I2SSFRM[2]	
GPP_S_6_SNDW2_DATA1_SNDW1_CLK_DMIC_CLK_A_1_I2S2_TXD		SNDW_DATA[2][1]	SNDW_CLK[1]	DMIC_CLKA[1]	I2STXD[2]	
GPP_S_7_SNDW3_DATA3_SNDW2_DATA2_SNDW1_DATA0_DMIC_DATA_1_I2S2_RXD	SNDW_DATA[3][3]	SNDW_DATA[2][2]	SNDW_DATA[1]	DMIC_DATA[1]	I2SRXD[2]	

PTL-UH RVP supports different codec validation via AIC connected through JA, JD, JE & JH headers.

### 12.3.1 JA Header [HDA/I2S Header]

JA header is used to provide clock & data transmission in HDA mode & I2S mode.

For HDA mode, Realtek GEN3 AIC (ALC245) will be used along with the transducer card.

In SNDW mode, it will be used as power source for AIC. Refer below table for the header pinout vs silicon pin mapping details.

**Table 39: Audio Header (JA) Connection**

JA Header Pin Number	SoC Signal Name	Header Signal Definition
JA.1	GPP_D_10_HDA_BCLK_I2S0_SCLK_HDACPU_BCLK	HDA_BCLK_I2S0_SCLK_HDR
JA.2	NA	GND
JA.3	GPP_D_16_HDA_RST_B_DMIC_CLK_A_1 / GPP_D_9_I2S_MCLK1_OUT	HDA_RST_N_I2S_MCLK1_HDR
JA.4	NA	+V1P8DX_AUDIO_JA
JA.5	GPP_D_11_HDA_SYNC_I2S0_SFRM	HDA_SYNC_I2S0_SFRM_HDR
JA.6	NA	GND
JA.7	GPP_D_12_HDA_SDO_I2S0_TXD_HDACPU_SDO	HDA_SDO_I2S0_TXD_HDR
JA.8	NA	+V3P3DX_AUDIO_JA
JA.9	GPP_D_13_HDA_SDIO_0_I2S0_RXD_HDACPU_SDIO	HDA_SDIO_I2S0_RXD_HDR
JA.10	NA	+VBATA_V5DX_AUDIO_JA
JA.11	GPP_D_17_HDA_SDIO_1_DMIC_DATA_1 / GPP_E_19_PMC_I2C_SDA	HDA_SDIO_1_GPIO_EN_HDR
JA.12	NA	RESERVED(key)
JA.13	GPP_H_7_I2C3_SCL_UART1_TXD_A_ISH_UART1_RXD	I2C3_SCL_AUDIO_HDR
JA.14	GPP_H_6_I2C3_SDA_UART1_RXD_A_ISH_UART1_RXD	I2C3_SDA_AUDIO_HDR
JA.15	GPP_F_17_THC1_SPI2_CS_B_A_ISH_SPI_CS_B_GSPI1_CS0_B	CODEC_IRQ_HDRX45
JA.16	NA	GND

### 12.3.2 JD Header [DMIC Header]

The JD header can be configured to drive 2-SPKR/4-SPKR using ALC1320 stereo amplifier codecs on Realtek GEN6 AIC or it can drive 6-SPKR using 6x Jamerson CS35L56 smart amplifiers on cirrus v3 AIC and it can be used to connect 4xDMIC's directly (via Transducer card). Refer below table for the header pinout vs silicon pin mapping details.

**Table 40: Audio Header (JD) Pinout**

JD Header Pin Number	SoC Signal Name	Header Signal Definition
JD.1	GPP_S_4_SNDW2_CLK_DMIC_CLK_A_0_I2S2_SCLK	DMICO_CLK_SNDW2_CLK_HDR
JD.2	GPP_S_5_SNDW2_DATA0_DMIC_DATA_0_I2S2_SFRM	DMICO_DATA_SNDW2_DATA0_HDR
JD.3	NA	GND
JD.4	NA	V1P8DX_DMIC_JD
JD.5	GPP_S_6_SNDW2_DATA1_SNDW1_CLK_DMIC_CLK_A_1_I2S2_RXD / GPP_D_16_HDA_RST_B_DMIC_CLK_A_1	DMIC1_CLK_SNDW1_CLK_SNDW2_DATA1_HDR
JD.6	GPP_S_7_SNDW3_DATA3_SNDW2_DATA2_SNDW1_DATA0_DMIC_DATA_1_I2S2_RXD / GPP_D_17_HDA_SDIO_1_DMIC_DATA_1	DMIC1_DATA_SNDW1_DATA0_SNDW2_DATA2_HDR
JD.7	NA	GND
JD.8	NA	RESERVED(key)

### 12.3.3

#### JE Header [SNDW Header]

The JE header can be used to drive ALC712-VB full function codec or ALC713-VB UAJ codec in multilane operation on Realtek GEN6 AIC. It can also drive Cohen CS42L43 jack codec in multilane operation on Cirrus v3 AIC. Refer below table for the header pinout vs silicon pin mapping details.

**Table 41: Audio Header (JE) Pinout**

JE Header Pin Number	SoC Signal Name	Header Signal Definition
JE.1	GPP_S_2_SNDW3_DATA1_SNDW0_CLK_DMIC_CLK_A_0_I2S1_SCLK	SNDW0_CLK_SNDW3_DATA1_I2S1_CLK_HDR
JE.2	GPP_S_3_SNDW3_DATA2_SNDW2_DATA1_SNDW0_DATA0_DMIC_DATA_0_I2S1_SFRM	SNDW0_DATA0_SNDW3_DATA2_I2S1_SFRM_HDR
JE.3	NA	GND
JE.4	NA	+V1P8DX_V5DX_AUDIO_JE
JE.5	GPP_S_6_SNDW2_DATA1_SNDW1_CLK_DMIC_CLK_A_1_I2S2_TXD	SNDW1_CLK_HDR
JE.6	GPP_S_7_SNDW3_DATA3_SNDW2_DATA2_SNDW1_DATA0_DMIC_DATA_1_I2S2_RXD	SNDW1_DATA0_HDR
JE.7	NA	GND
JE.8	NA	RESERVED(key)
JE.9	GPP_S_0_SNDW3_CLK_I2S1_TXD	SNDW3_CLK_I2S1_TXD_HDR
JE.10	GPP_S_1_SNDW3_DATA0_I2S1_RXD	SNDW3_DATA0_I2S1_RXD_HDR

### 12.3.4

#### JH Header

JH header will be used as additional power source in 4-SPKR/6-SPKR configuration. It also provides, SUS\_CLK connection as always-on-clock for future use (Smart DMIC use-cases), PLT\_RST\_N is routed additionally so that when AIOC is powered from external supply and power recycle is done for RVP, PLT\_RST\_N can be used to ensure AIOC power recycle in such cases.

**Table 42: Audio Header (JH) Pinout**

JH Header Pin Number	SoC Signal Name	Header Signal Definition
JH.1	NA	V5DX_AUDIO_JH
JH.2	NA	V5DX_VBATA_AUDIO_JH
JH.3	NA	RESERVED(key)
JH.4	NA	GND
JH.5	GPP_B_13_PLTRST_B/GPP_V_4_SLP_S3_B/PRIM_VR_BFR_OUT	PLT_RST_PWREN_HDR
JH.6	GPP_D_9_I2S_MCLK1_OUT MIC_PRIVACY_HDR/GPP_V_7_SUSCLK	MIC_PRIVACY_I2S_MCLK_SUS_CLK_HDR

### 12.3.5

#### JS Header (ALC722 codec DMIC & SPKR Header)

JS header is used to connect on-board ALC722 codec DMIC and SPKR load using Y-cable on transducer AIC. It can drive 4xDMIC & 2 SPKR's.

**Table 43: Audio Header (JS) Pinout**

JS Header Pin Number	SoC Signal Name	Header Signal Definition
JS.1	DMIC_CLK	CODEC_DMIC_CLK_HDR
JS.2	DMIC_DATA12	CODEC_DMIC_DATA12_HDR
JS.3	NA	GND
JS.4	NA	+V1P8DX_DMIC_JS_HDR
JS.5	NA	GND
JS.6	DMIC_DATA34	CODEC_DMIC_DATA34_HDR
JS.7	NA	GND
JS.8	NA	RESERVED(key)
JS.9	SPK_OUT_L+	CODEC_SPKR_OUT_L_P_HDR
JS.10	SPK_OUT_L-	CODEC_SPKR_OUT_L_M_HDR
JS.11	SPK_OUT_R+	CODEC_SPKR_OUT_R_P_HDR
JS.12	SPK_OUT_R-	CODEC_SPKR_OUT_R_M_HDR

## 12.4 Privacy Microphone Protection Feature

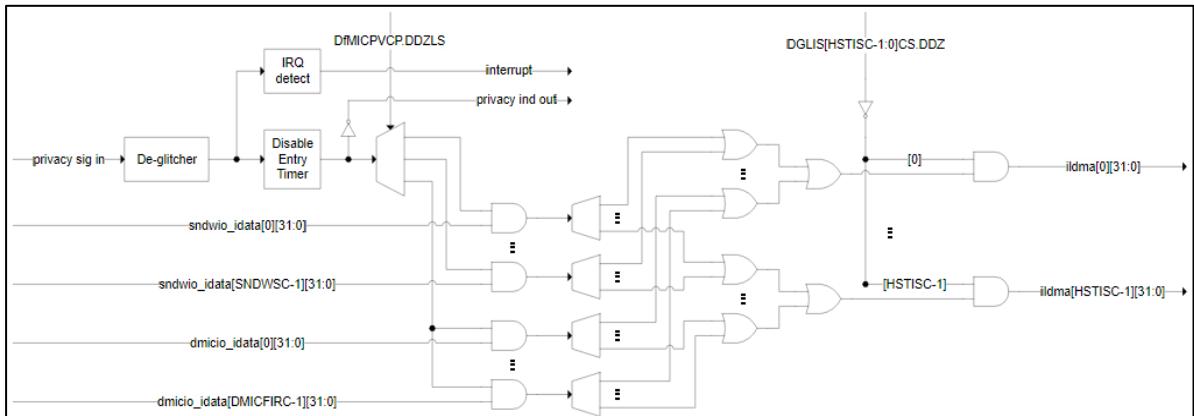
Privacy microphone protection feature is POR in PTL-UH RVP.

The ACE (Audio Context Engine) IP offers a microphone privacy protection scheme through a HW DMA (Dynamic Memory Access) data zeroing mechanism, if parameter (Microphone Privacy Enable) MICPVCE = 1.

The HW will take in a privacy signaling input from the GPIO pin (which typically connects to a mic disable switch), indicating the current user privacy mode setting on the system.

If the mic disable switch is turned on, and the DfMICPVCP.DDZE policy register indicates privacy mode is enabled, the HW will interrupt DSP FW (if link management is offloaded) / host SW (if link management is not offloaded) indicate the mic disable entry (allow DSP FW / host SW to gracefully [ the audio capture stream without any audible glitches), and then mask the data from the microphone to zeros after a time-out period programming in DfMICPVCP.DDZWT register. It also turns on a privacy indicator output through the GPIO pin (which typically connects to a privacy LED).

When the mic disable switch is turned off later, the HW will unmask the data from the microphone (immediately) and interrupt DSP FW indicating the mic re-enabling (allow DSP FW / host SW to gracefully unmute), as well as turning off the privacy LED indication through the GPIO pin.



**Figure 56: Privacy microphone protection conceptual diagram**

**Reference:**

[https://docs.intel.com/documents/iparch/ace/ACE%20IP/3.x/Integration%20Specs/PTLSM/PTLSM\\_ACE3.x\\_I/integration\\_HAS.html#privacy-microphone-protection](https://docs.intel.com/documents/iparch/ace/ACE%20IP/3.x/Integration%20Specs/PTLSM/PTLSM_ACE3.x_I/integration_HAS.html#privacy-microphone-protection)

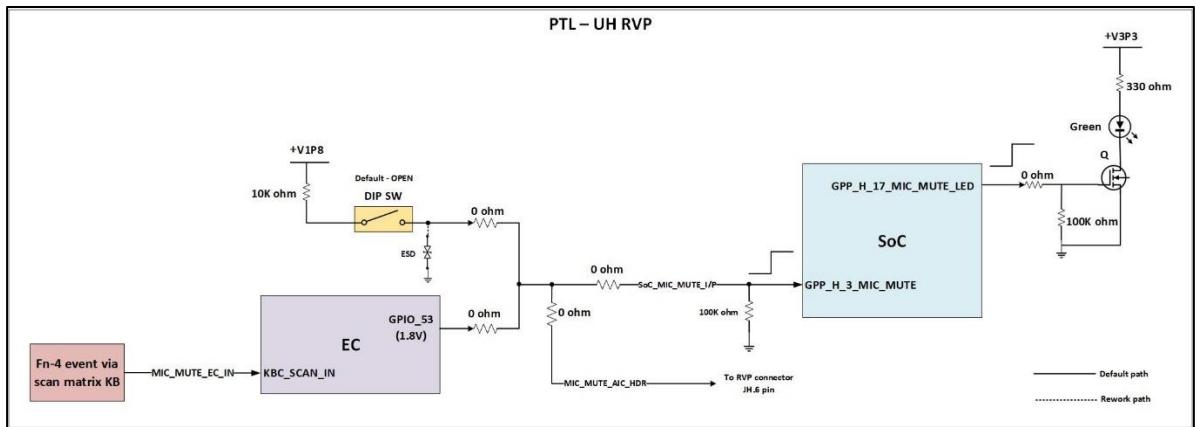
Below table represents the **privacy sig in & privacy ind out** signal description.

SIGNAL NAMES	TYPE	DESCRIPTION
PVC_SIG_IN	I	<b>Privacy Signaling Input:</b> Privacy microphone disable signaling input, typically for connection to a switch. Asserted high to indicate the microphone disabled state (HW will ensure the data output from the microphone is masked to zero).
PVC_IND_OUT	O	<b>Privacy Indicator Output:</b> Privacy microphone disable indication output, typically for connection to an LED. Asserted high to indicate the microphone disabled state (after HW has masked the data output from the microphone to zero).

**Figure 57: Privacy microphone protection signal description**

**Note:** These pins are typically associated with DMIC interface, but also usable by microphone connected over SoundWire interfaces.

PTL-UH RVP uses SoC pins MIC\_MUTE and MIC\_MUTE\_LED to support microphone privacy protection. The below diagram represents RVP implementation.

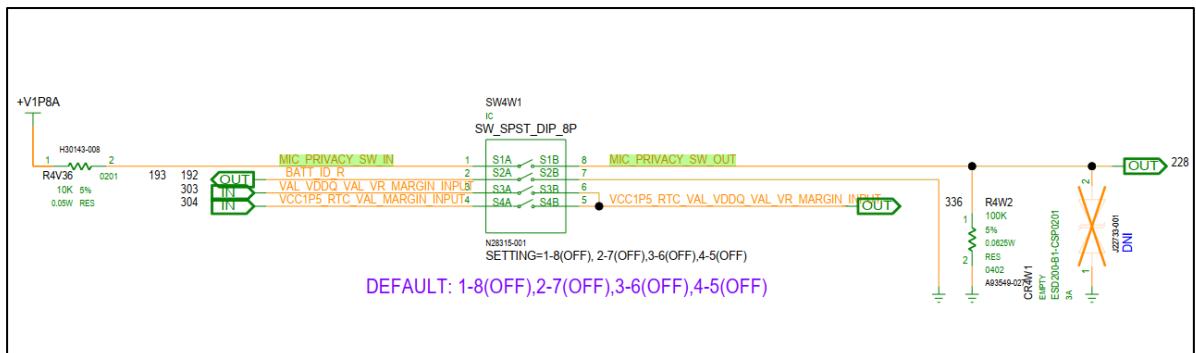


**Figure 58: PTL-UH RVP audio MIC privacy support block diagram**

SIGNAL NAME	DESCRIPTION
GPP_H_3_MIC_MUTE	Mic mute - Indicate the user privacy mode setting on the system (ON : gate the clock to the mic, OFF : ungate the clock to the mic)
GPP_H_17_MIC_MUTE_LED	Mic mute led- Led to Indicate the user privacy mode setting on the system. (ON : gate the clock to the mic, OFF : ungate the clock to the mic)

PTL-UH RVP has switch SWxx to control the MIC privacy operation. Default SWxx pin [1-8] is OFF, when user wants to turn on the MIC mute option then SWxx pin [1-8] should be ON. Alternately, MIC mute can also be controlled via EC using scan matrix Fn key.

**Figure 59: PTL-UH RVP audio MIC privacy switch**



## 12.5

### Audio section circuit optimization

PTL-UH RVP audio power supply generation optimized with default load switch bypass configuration for all the audio power generation (no RTD3 support) as compared to the load switch controlled in the previous generation of program. RVP team will monitor the no risk in the ERB validation with load switch bypass configuration and completely remove the load switch circuit from PTL-UH CRB onwards.

ALC722-CG codec & AIC rails will follow default platform sequencing of **VBATA -> 5V&3.3V -> 1.8V** supply.

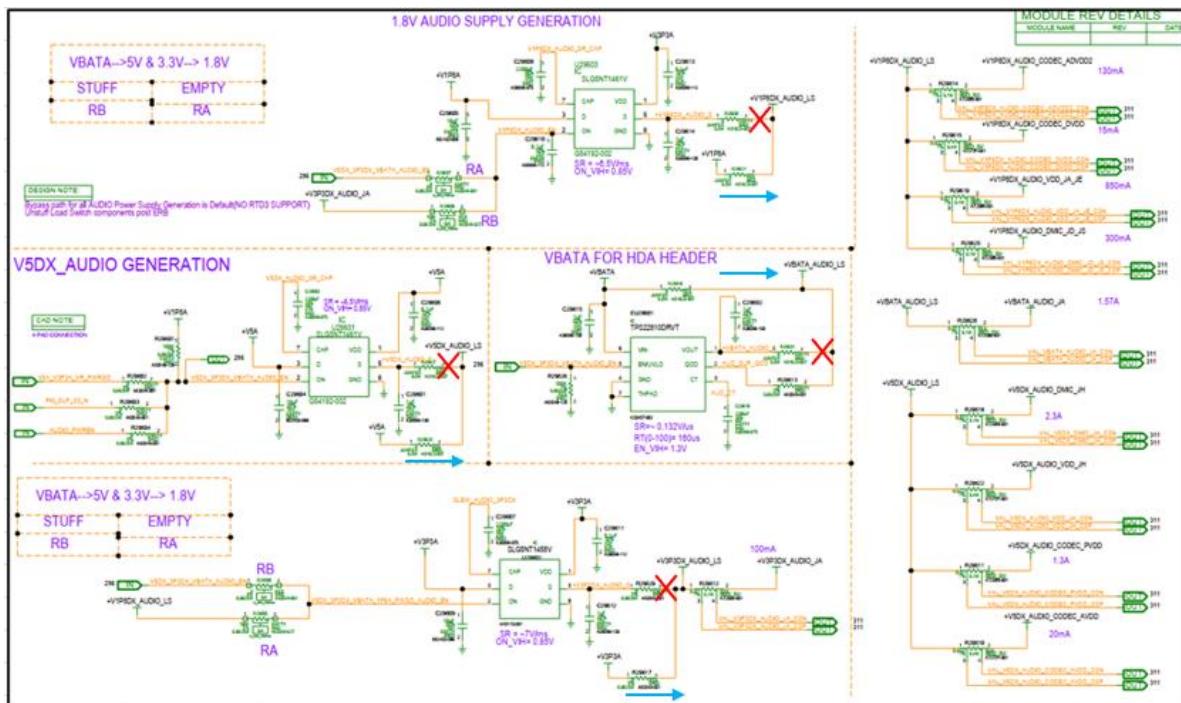
Below table captures the audio power rails load current requirement followed in PTL-UH RVP. ALC722 load current requirements are aligned with the Realtek team and AIC power rail requirements are aligned with Realtek/Cirrus and CHROME audio AIC stakeholders.

**Table 44: PTL-UH RVP audio power requirements**

Source power domain	Source power rail	Audio section voltage rail	Header/CODEC	Voltage [V]	Current [mA]	Remarks
+V1P8A	+V1P8DX_AUDIO_LS	+V1P8DX_AUDIO_VDD_JA_JE	JA.4, JE.4	1.8V ± 5%	850	
		+V1P8DX_AUDIO_DMIC_JD_JS	JD.4, JS.4	1.8V ± 5%	300	
		+V1P8DX_AUDIO_CODEC_ADVDD2	ALC722 AVVD2 supply	1.8V ± 5%	130	
		+V1P8DX_AUDIO_CODEC_DVDD	ALC722 DVDD supply	1.8V ± 5%	15	
+V3P3A	+V3P3DX_AUDIO_LS	+V3P3DX_AUDIO_JA	JA.8	3.3V ± 5%	100	
+V5A	+V5DX_AUDIO_LS	+V5DX_AUDIO_CODEC_PVDD	ALC722 PVDD supply	5V ± 10%	1300	
		+V5DX_AUDIO_CODEC_AVDD	ALC722 AVDD supply	5V ± 10%	20	
		+V5DX_AUDIO_DMIC_JH	JH.1	5.0V ± 5%	2300	
		+V5DX_AUDIO_VDD_JH	JH.2	5.0V ± 5%		
+VBATA	+VBATA_AUDIO_LS	+VBATA_AUDIO_JA	JA.10	13V ± 5%	1575	19V DC [AC-DC output adaptor] corresponding VBATA = 13V

Refer PTL-UH RVP schematic pdf page number 296 for audio power supply generation scheme.

**Figure 60: PTL-UH RVP audio power supply generation load switch bypass approach**



## 13 Serial Interfaces- SPI, eSPI, SMBus, SM Link, MLink/CLink

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This chapter discusses about the various serial interfaces namely SPI, eSPI, THC-SPI, SMBus, SMLink, MLink. The SPI, eSPI and THC-SPI are functionally similar IPs. The mapping of all serial ports is as shown below. The mapping is subjected to change based on the inputs from design or validation teams.

**Notes:**

1. For probing these signals, test points will be provided by opening the via masks on the SOC side. For the device side, series resistors or pull ups close to the device will be used for probing. If there are no components available near the end device for probing, then the test points will be provided closest to the device. However, if the test points are adding additional vias and violate the SI guidelines, then test points will not be provided.
2. For all the serial interfaces, for only one of the ports, A dummy test structure consisting on VCC pull up resistor (empty), load capacitor to ground(empty) and 0-ohm series resistor(populated) sharing pads as close as possible to SOC side and device side will be implemented.
3. Following options are not provided on RVP for any of the LPSS / ISH / Serial interfaces:  
TLA footprint, midbus probes, Beagle headers, Aardwark support.
4. The mapping of ports and GPIOs will be same for all the RVP SKUs to ease software effort. Deviations will be mentioned in the specific sections.

### 13.1 SPI & THC SPI Ports

The PTL SOC provides Serial Peripheral Interfaces (SPI) for connecting BIOS Flash, TTK3 and TPM. Which is 1.8V IO voltage only with maximum speed of 50MHz.

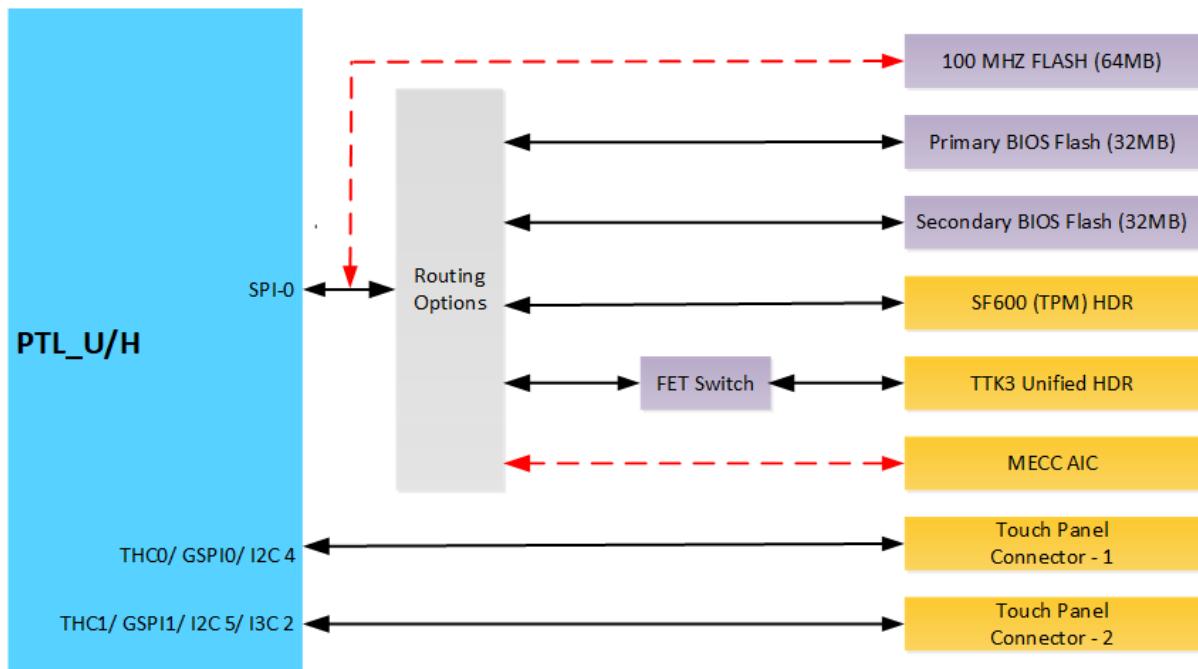
The SPI0 (CSME SPI) interface consists of 3 chip-select signals. It is allowing up to two flash memory devices (SPI0\_CS0# and SPI0\_CS1#) and one TPM device or TTK3 device (SPI0\_CS2#) to be connected to the SOC working in quad-mode. The SPI0 interfaces support 1.8V only.

A rework option would be provided for the 32MB SPI flash part working at 100MHz, 1 Load only on the SPI0 bus.

Legacy touch can be supported from GSPI. But since THC is POR for PTL, only THC based touch connections will be provided on RVP. GSPI based touch support is not provided.

The GSPIO interface is multiplexed with THC0, implementing one Chip Select signal (SPI0\_CS#) and is intended for integrated touch implementation, also working in quad-mode. GSPIO supports 1.8V only. THC/I2C/GSPI signals are all muxed internally in the PCH as a HID device port (there are 2 HID ports on PTL) and will be programmable through the BIOS GPIO Configuration (as alternate functions). For this requirement, no board reworks needed to switch among bus selection within the same HID port, HID port definition was introduced in ADP-LP.

Refer to the BIOS Flash Interface (SPI) section for detailed explanation on the Flash sharing mechanisms.



**Figure 61: PTL U/H RVP SPI & THC SPI Interface support**

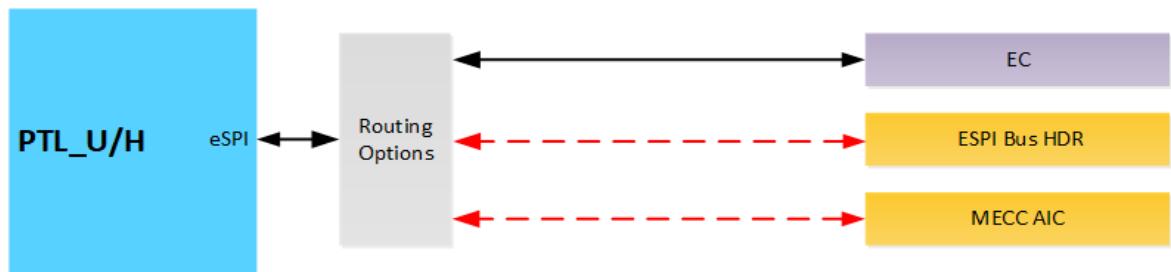
## 13.2 eSPI Port

The PCH eSPI (Enhanced SPI) controller supports the following features:

- Support for 20MHz, 25MHz, 33MHz and 50MHz bus operation.
- 1.8V support only
- Up to quad mode support with 2 Chip Select signals.
- In-band messages for communication between the SOC and slave device to eliminate side-band signals
- Real time SPI flash sharing, allowing real time operational access by the SOC and slave device.
- MAF & SAF modes
- PECl over eSPI

On PTL-U/H RVP, eSPI interface is for the communication between EC and SOC. This port can run at max of 50MHz and IO voltage is 1.8V. The eSPI pins will be routed to ESPI Bus Header with appropriate reworks.

eSPI also has an option, as illustrated in the figure below to be connected to the MECC connector for other EC support and eSPI bus header.



**Figure 62: PTL-U/H RVP eSPI Interface support**

### 13.3 SMBus & SMLink

SMBus Controller IP is SMBus 2.0 compliant and provides a mechanism for the SOC to initiate communications with the SMBus peripherals (slaves) or allows external attached peripherals to write or read to the SoC. SMBus controller supports 100 kHz, 400 kHz, 1 MHz operation.

On PTL\_U/H RVP, the SMBus is interfaced to PCIe Slot, Memory SPD (SODIMM), FRU EEPROM, ESPI Bus Header, SOC MIPI60 Connector, PM Side Band Header, TTK3 Header using a SMBUS Bus expander. Figure 66 gives the list of devices on the SMBUS.

SOC implements 2 SMLink controllers for the 3 SMLink interfaces, SMLink0, SMLink0B and SMLink1. The interfaces are intended for system management and are controlled by the Intel® ME. And they can run at frequencies up to 1MHz.

On PTL\_U/H SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.

SMLink0 is routed to Jacksonville, x1 PCIe Slot, Modular TCSS AIC and TBT Retimer. SMLink0B is muxed with ISH UART0 and default used as ISH UART0. SMLink1 is routed to PM Sideband Header, modular TCSS AIC and PD AIC

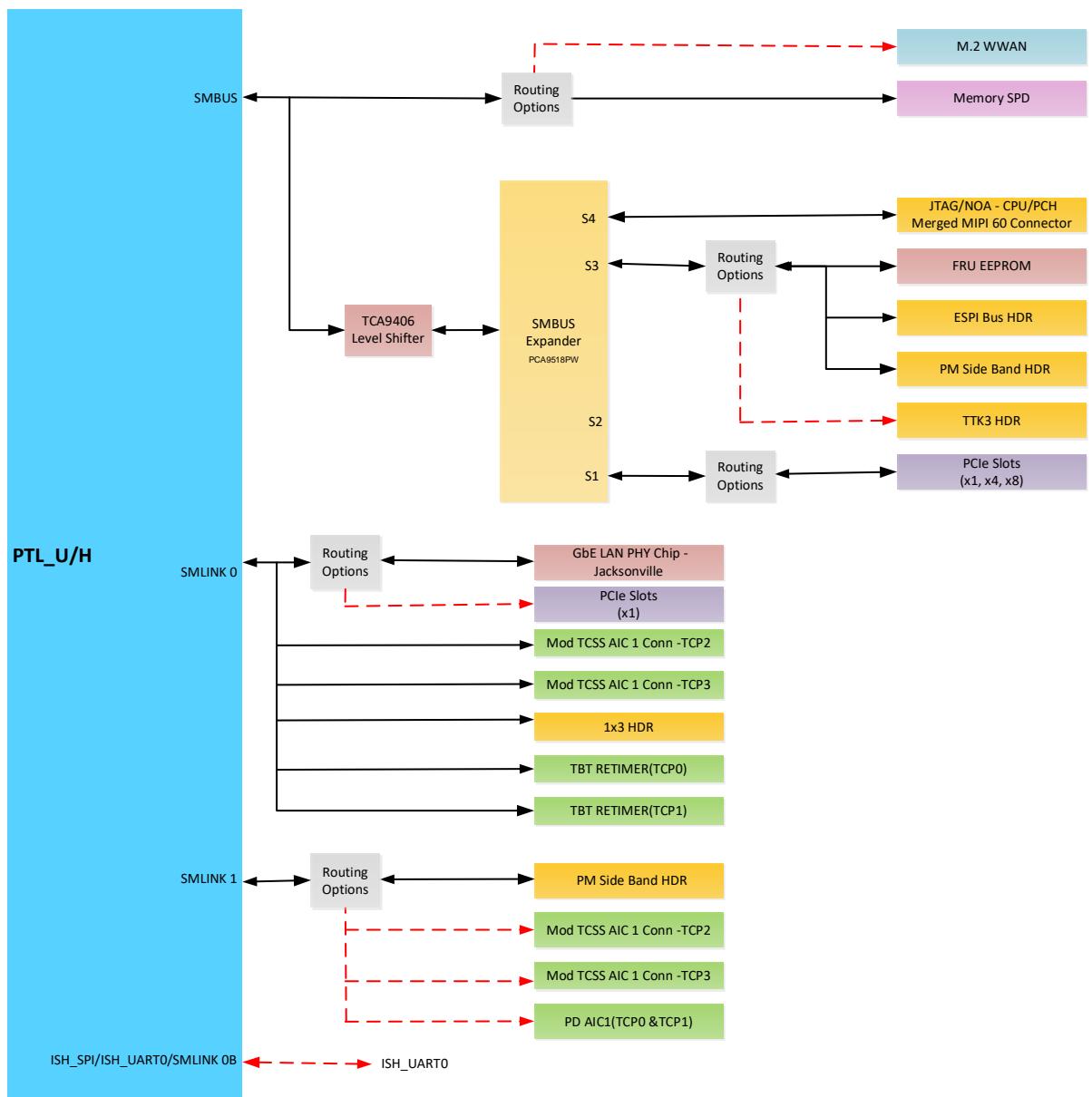


Figure 63: PTL-U/H RVP SMBus & SMLink support

## 13.4

## MLink / CLink

M-Link interface is the management communication link between the SOC and Intel Wireless cards. It enables Manageability to support low power interface of Intel WiFi network interfaces.

Supported in S0 and Sx power states. Single Clink controller to connect to external C-link device or as a internal C-link connection with CNVi.

Note: Clink has also been called Manageability link (MLink) in some documentation

The M.2 WLAN card Link Status can be monitored with help of C-Link signals from the M.2 Module. The signal routing option is provided through a tri-pad, to the WLAN module, 2x4 Header and SOC.

**Table 45: CLink Interface Signals**

Signal Name	Type	Description
CL_RST#	O	Wi-Fi* CLINK host bus reset for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK reset pin on the Intel® vPro™ Wi-Fi* module.
CL_DATA	I/O	Wi-Fi* CLINK host bus data for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.
CL_CLK	O	Wi-Fi* CLINK host bus clock for standard CNV with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

## 14 Embedded Controller

PTL-U/H RVP will support MEC1723 Microchip Embedded Controller (EC) onboard in windows SKU and MEC1727 in chrome SKU (both the parts are footprint compatible). MEC1723 and MEC1727 support eSPI mode of operation. LPC mode will not be supported in PTL. EC controls the preliminary platform power sequencing and does system and power management. EC is the platform thermal controller that monitors and throttles CPU or controls CPU Fan. The key functionalities of EC on the platform are illustrated in below figure.

**Note:** EC part (144-pin WFBGA package) used in PTL-U/P/H design is **MEC1723NB0-I/SZ (Windows SKU)** / **MEC1727N-B0-I/SZ-CHR0 (Chrome SKU)**.

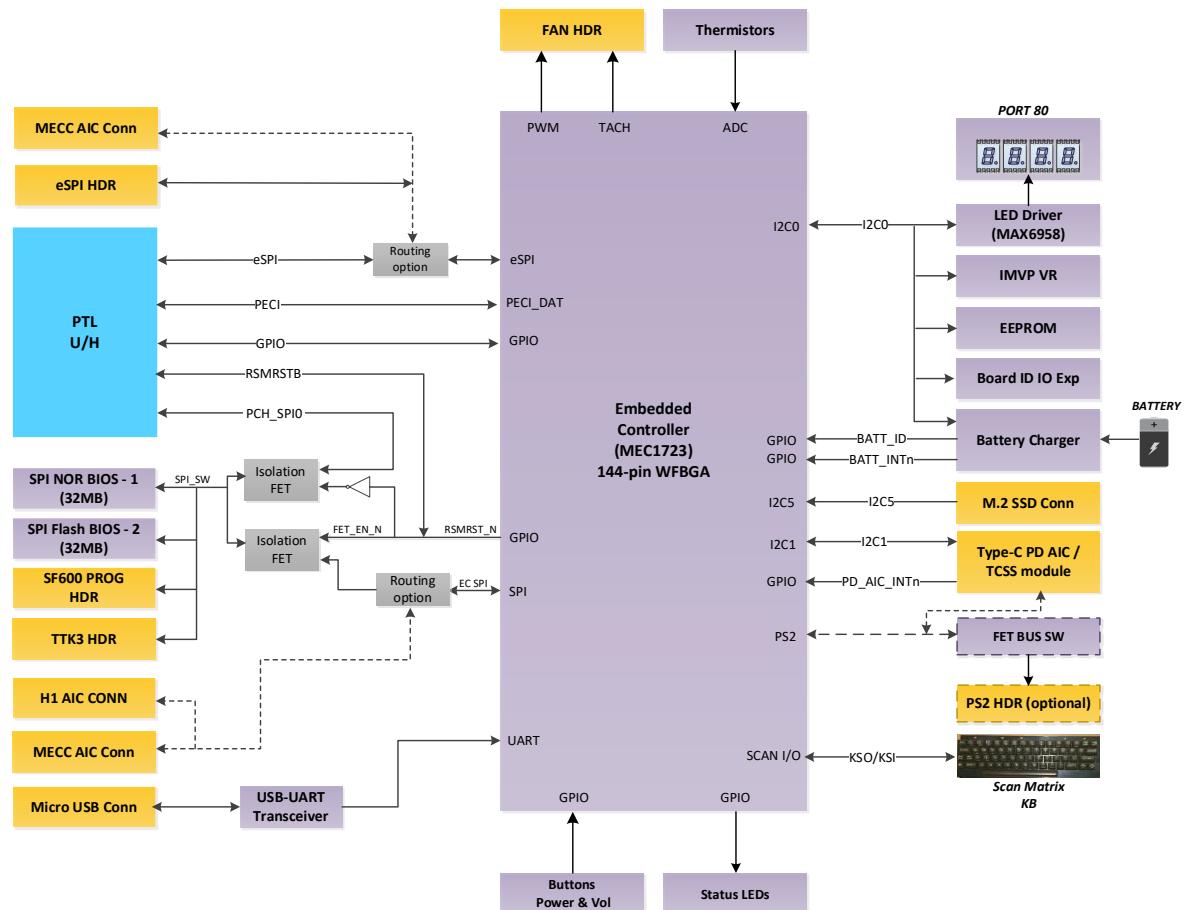


Figure 64: Embedded Controller Block Diagram

The EC subsystem consists of:

- Thermal Management functions like CPU Fan control, Chassis Fan control, PECL, DIMM temperature etc.
- Platform Power management like Power sequencing, Sx and Deep Sx entry/exits.
- Any CEC specific Modern Standby requirements to be implemented inside EC
- Handles the Board-ID, Fab-ID, BOM SKU-ID, messages to the BIOS.
- RVP design will support all three i.e., SAF, MAF, G3 Flash configuration, default will be MAF.
- 2x14 pin eSPI header will also be supported.
- Switching between MAF / SAF / G3 will be through resistors rework and switch settings change.
- Separate PMR resistors will be added for 1.8V and 3.3V rails going to EC.
- EC GPIO mapping has been shared with EC team.
- MECC connector will be supported only in RVP1 SKU of PTL-UH RVP for validating EC from different vendors on.

In PTL-UH RVP we had brought few changes/ optimizations as compared to previous RVP platforms in the EC and MECC sections to ease out the routings, reduce BOM cost, add extra features etc. The details are mentioned below.

- Only one PS2 header is supported (**BOM EMPTY option only**) over the PTL-UH RVP which is default configured as PS2 KB from EC. EC has only one PS2 IP which can be configured as PS2 KB/ PS2 mouse at any given point of time. This PS2 KB header is only supported in RVP1 SKU of PTL-UH RVP.
- The LDO to generate the VREF ADC rail has been removed from PTL-UH RVP. So, this is generated from 3.3VA KBC EC rail in current design (same as VTR\_PLL rail, as recommended in EC datasheet).
- We have additional 3 thermistors in PTL-UH RVP getting mapped to the EC for energy telemetry application.
- EC EEPROM is removed from PTL-UH RVP as deep Sx state is not supported in none of the SKUs.
- Few signals are removed from the on-board EC due to lack of functionality to ease out the routing (EC SMI signal, HB NVDC SEL, EC SLP S0 CS, INT from board ID IO expander, Aux adapter detect, EC SML CLK/ DATA).
- There has been changes done to latest MECC specifications as per platform requirements after discussion in EC WG, kindly refer to MECC section for more details.

The windows EC GPIO mapping sheet is shared over [Link](#).

The chrome EC GPIO mapping sheet is shared over [Link](#).

The RVP supports LED for CAPSLOCK, NUMLOCK and SCROLL LOCK. The EC error code table with on-board LED status is given below.

**Table 46: EC error code indication**

Error type	Error code	Caps Lock LED	Scroll Lock LED	Num Lock LED
No Error	0	Off	Off	Off
RSMRST#_PWRGD	1	Off	Off	Flash
PM_SLP_S5#	2	Off	Flash	Off
PM_SLP_S4#	3	Off	Flash	Flash
PM_SLP_S3#	4	Flash	Off	Off
PM_SLP_A#	5	Flash	Off	Flash
ALL_SYS_PW_RGD	6	Flash	Flash	Off
PLTRST#	7	Flash	Flash	Flash

It is to be noted that,

- KSC Thermal Shutdown is indicated by flashing of Num\_Lock and Caps\_Lock LEDs alternatively.
- The above errors are displayed by EC on Port80 as EC 01 to EC 07. These errors are not EC errors, and these errors represent the platform status.

## 14.1 MECC AIC Support

MECC AIC connector(200-pin) is supported for windows ([only in RVP1 LP5x T3 MECC SKU, PTL -UH -15](#)) and chrome RVP for validating the external EC over AIC. Chrome BoM SKU is default supported through onboard Chrome AVL EC MEC1727N-B0-I/SZ-CHRO part.

Chrome SKU also supports the MECC AIC option. Chrome SKU uses H1 & Servo AIC same as MTL-P for Chrome SKU.

**Note:** [Along with Chrome SKU](#) MECC connector is supported only on RVP1 [LP5x T3 MECC SKU, PTL -UH -15](#) SKU. It is not supported on other RVP SKUs.

**Table 47: MECC Connector**

MFG	Mfg. Part Number	IPN Number
Amphenol	84535-191LF	N15428-001

MECC connector pinout details are shared over [Link](#).

## 14.2 Flash Sharing

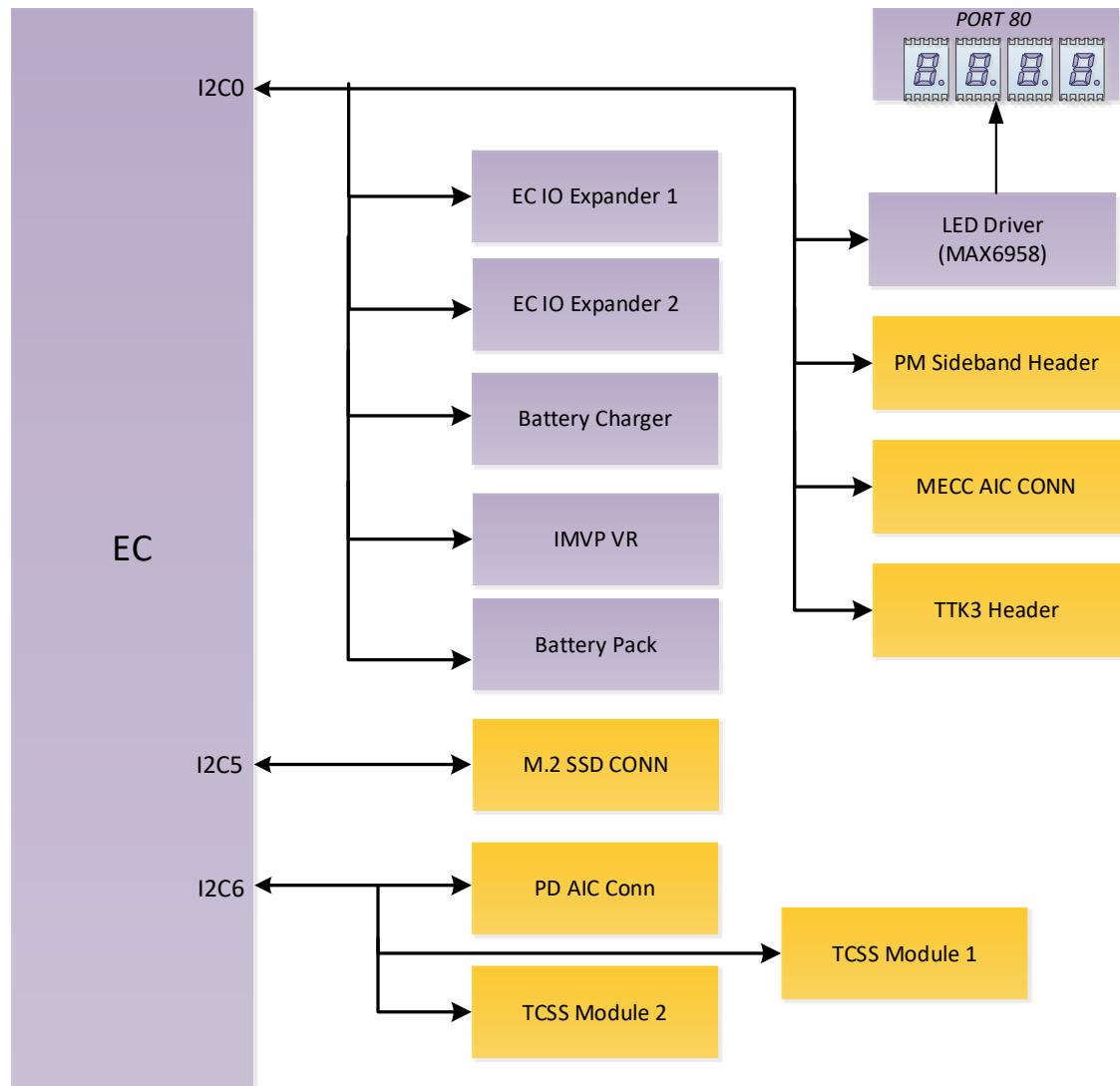
PTL-U/H RVP supports both MAF, SAF and G3 flashing configuration. There is no dedicated Flash to EC. SOC GPIO is used for flash selection strap pin refer Pin strap section for more details.

EC shared flash (SOC SPI NOR).

- Shared SPI Flash: Currently a Composite image. Update is done by BIOS. Top swap allows recovery.
- Slave Attached EC Flash. Lot of security features in EC.

## 14.3 EC – I2C IO Expander

I2C based IO expanders are provided to handle Board-ID, Fab-ID, BOM SKU-ID and some IO requirement. EC I2C mapping is provided in the below table.



**Figure 65: EC- I2C Block Diagram**

## 14.4

### EC – Headers

Below sections includes connector and pinout details of the connectors used in EC section.

#### 14.4.1

##### eSPI Sideband Header

**Table 48: eSPI Sideband Header and Pinout**

MFG	Mfg. Part Number	IPN Number
Samtec	ASP-175166-01	H46981-001

Signal Name	Pin #	Pin #	Signal Name
ESPI_CLK_HDR	1	2	GND
ESPI_CS0_HDR_N	3	4	NO PIN
SHM_TRIG_PLT_RST_R	5	6	+V5A_VAL
ESPI_IO3_HDR	7	8	ESPI_IO2_HDR
+V3P3A_VAL	9	10	ESPI_IO1_HDR
ESPI_IO0_HDR	11	12	GND
SMB_CLK_S3	13	14	SMB_DATA_S3
+V3.3A_1.8A_R1 TPM	15	16	ESPI_CS1_HDR_N
GND	17	18	ESPI_CS2_HDR_N
ESPI_RST_HDR_N	19	20	ESPI_ALERT0_HDR_N
NO PIN	21	22	NO PIN
ESPI_ALERT1_HDR_N	23	24	ESPI_CS3_HDR_N
TP_GPP_A8_CLKRUN_R_N	25	26	ESPI_ALERT3_HDR_N
+V5A_VAL	27	28	ESPI_ALERT2_HDR_N

#### 14.4.2

##### PS2 KB HEADER

In PTL-UH RVP, only one PS2 header (Empty option) is supported which is configured as PS2 KB from EC.

**Table 49: PS2 KB Header and Pinout**

MFG	Mfg. Part Number	IPN Number
SAMTEC/ Weison	TSM-105-01-L-SV-P-TR/ AC2100-0009-070-HH	J47721-001

Pin #	Signal Name
1	PS2_KB_CLK_FB
2	+V5_PS2
3	GND
4	GND
5	PS2_KB_DATA_FB

#### 14.4.3 PS2 Mouse HEADER (Removed from PTL-UH RVP)

There is no PS2 mouse header on PTL-UH RVP.

#### 14.4.4 Scan Matrix Keyboard Header

Table 50: Scan Matrix Header and Pinout

MFG	Mfg. Part Number	IPN Number
Ipex	20542-028E-01	H24635-001

Pin #	Signal Name
1	KBC_SCANIN<6>
2	KBC_SCANIN<0>
3	KBC_SCANIN<1>
4	KBC_SCANOUT<6>
5	KBC_SCANIN<3>
6	KBC_SCANIN<2>
7	KBC_SCANOUT<15>
8	KBC_SCANIN<5>
9	KBC_SCANIN<4>
10	KBC_SCANOUT<10>
11	KBC_SCANOUT<14>
12	KBC_SCANIN<7>
13	KBC_SCANOUT<13>
14	KBC_SCANOUT<11>
15	KBC_SCANOUT<8>
16	KBC_SCANOUT<7>
17	KBC_SCANOUT<9>
18	KBC_SCANOUT<12>
19	KBC_SCANOUT<3>
20	KBC_SCANOUT<2>
21	KBC_SCANOUT<1>
22	KBC_SCANOUT<4>
23	KBC_SCANOUT<5>

24	KBC_SCANOUT<0>
25	LED_NUMLOCK
26	LED_CAPSLOCK
27	+V3.3A_KBC
28	NC

#### 14.4.5 Keyboard Backlight Header

**Table 51: KB Backlight Header and Pinout**

MFG	Mfg. Part Number	IPN Number
Ipex	20542-006E-01	H24575-001

Pin #	Signal Name
1	+V5S_KBD_BKLT
2	+V5S_KBD_BKLT
3	NC
4	NC
5	KBD_BKLT_CTRL_FET
6	KBD_BKLT_CTRL_FET

#### 14.4.6 Fan Header

**Table 52: Fan Header and Pinout**

MFG	Mfg. Part Number	IPN Number
Molex	53398-0471	K97577-001

Pin #	Signal Name
1	FAN_CONN_PWM_IN
2	CPU_TACHO_R_FAN
3	GND
4	+V5_FAN_SUPPLY

## 14.5 Front Panel Header

**Table 53: Front Panel Header and Pinout**

MFG	Mfg. Part Number	IPN Number
WIESON TECHNOLOGIES CO., LTD	AC2100-0009-042-HH	K96810-001

Signal Name	Pin #	Pin #	Signal Name
FRONT1(Pull up to 5V)	1	2	FRONT2 (Pull up to 5V)
TP_SATA_LED_N	3	4	GND
GND	5	6	PWR_CONN_D
RST_PUSH_N_D	7	8	GND
+V5A_VAL	9	10	No Pin
NC	11	12	GND
GND	13	14	No Pin
BC_ACOK_DSW	15	16	+V5A_VAL

## 14.6 PM Sideband Header

**Table 54: PM Sideband Header**

MFG	Mfg. Part Number	IPN Number
Molex	87832-4020	C12536-002

Signal Name	Pin#	Pin #	Signal Name
PM_PWRBTN_N	1	2	ALL_SYS_PWRGD
PM_RSMRST_N	3	4	SMB_BS_DATA_PORT80_R
PM_SLP_S5_N	5	6	SMB_BS_CLK_PORT80_R
PM_BATLOW_N	7	8	NC
PM_SLP_S3_N	9	10	SIDEBAND_TIME_SYNC_0
PM_SLP_S4_N	11	12	SML1_DATA_R
+V3P3A	13	14	SML1_CLK_R
EDM_SOC_IOE_PM_HDR	15	16	GND
RTC_RST_N	17	18	EDM_BASE_PM_HDR
SMC_WAKE_SCI_N	19	20	EDM_GCD_PM_HDR
NC	21	22	BC_ACOK_EC_IN
PS_ON_SW_N	23	24	PM_SLP_A_N
M2_SSD_EC_I2C05_CLK	25	26	PM_PCH_PWROK
M2_SSD_EC_I2C05_DATA	27	28	SRTC_RST_N
RECVRY_INDICATOR_N	29	30	RSMRST_PWRGD_N

PM_SYSRST_N	31	32	PM_SLP_SO_N
+V1P8A	33	34	BUF_PLT_RST_N
SMB_DATA_S3_J	35	36	SYS_PWROK
SMB_CLK_S3_J	37	38	EDM_CORE_PM_HDR
+V3P3S_VAL_J	39	40	+V3P3S_VAL_J

## 15 BIOS Flash Interface (SPI)

PTL-U/H RVP supports native SPI interfaces SPI0. The SPI0 is for used for flash and TPM while THC SPI1 and THC SPI2 are used for Touch interface.

PTL-U/H RVP supports 1.8V 64MB flash on SPI0 interface. Windows RVP will use 1x 64MB parts default and Chrome RVP will use 64MB default (dedicated 100 MHz 64MB flash for fast boot validation). To validate CS1 of SoC, only RVP 2 will be provided with second flash device as rework option. When CS1 device is stuffed in RVP2, both flash 0 and 1 will operate at reduced speed of 50MHz. The 100MHz flash device will not be provided RVP2 (LPCAMM SKU).

TPM AIC should be plugged into the same header used for BIOS flashing on SPI0.

PTL-U/H RVP will support 1.8V SPI devices for MAF/ SAF and G3 modes. SPI devices will support 80MHz clock rates. No 3.3V SPI support from PTL-U/H SOC.

Default Device supported on RVP will be 64MB 1.8V with RPNC. Jumper for Flash Descriptor Override will be supported. Also, RVP allows to boot the platform while Dediprog SF600/SF100 programmer is connected to the platform. Certain customers will be booting RVP using SPI device emulator connected to TPM connector or TTK connector. While doing this, the onboard SPI Flash will be isolated.

The SPI0 interface of SOC is shown in below diagram,

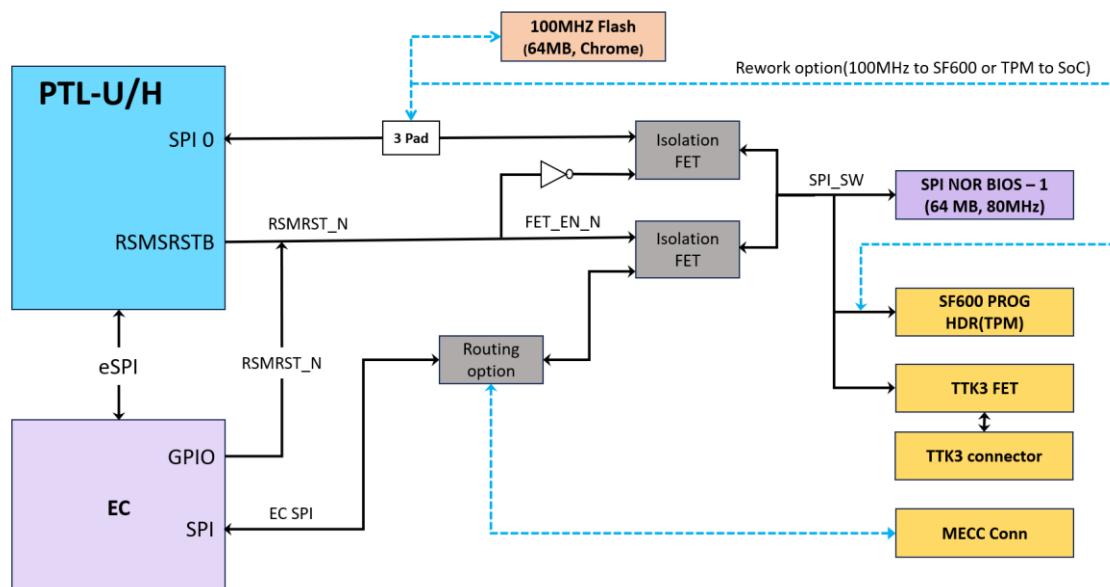


Figure 66: BIOS Flash interface for RVP1, RVP3, and RVP4

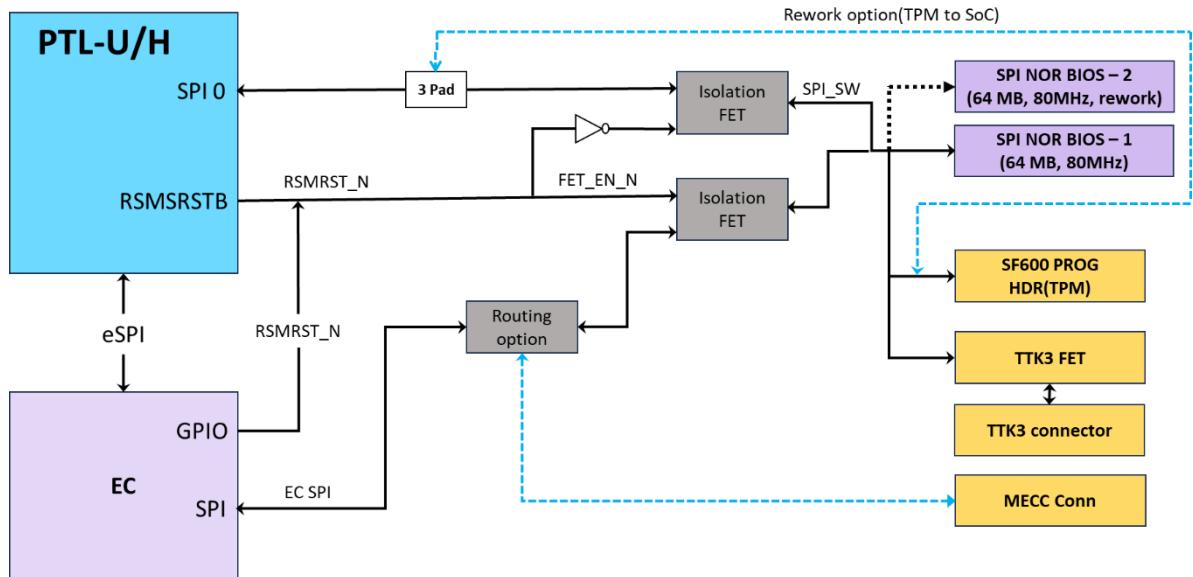


Figure 67 : BIOS Flash interface for RVP2

## 15.1

### EC Flash Topology

EC FW image is stored in either external SPINOR or embedded flash. The embedded flash should have enough space to store the entire FW and any Non-Volatile data. ECs without embedded flash requires an external SPI flash, either dedicated or shared with SOC. Three types of flash sharing mechanisms shall be supported on PTL-U/H RVP designs.

- G3 flash sharing
- MAF - Master attached flash sharing **<default option for platform default>**
- SAF - Slave attached flash sharing.

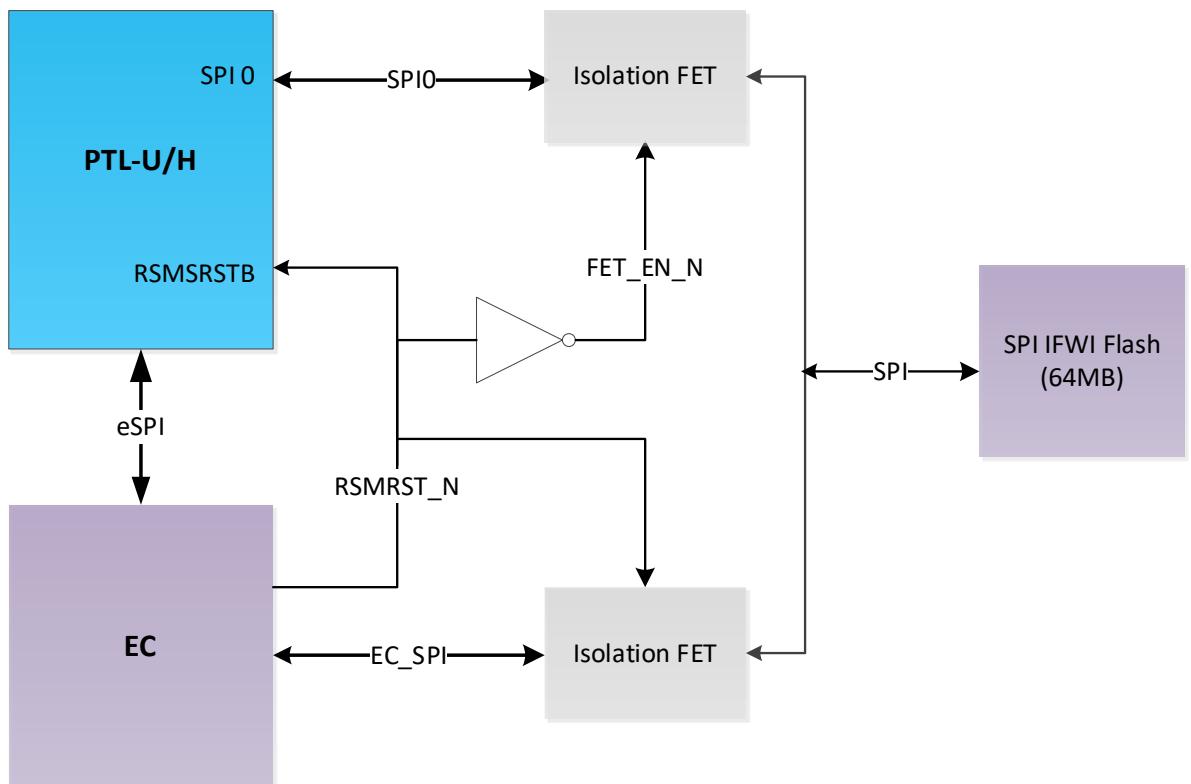
PTL-U/P/H RVPs shall support all the flash sharing mechanisms. Reworks required change into SAF or G3 from MAF is minimized comparing to previous platforms.

#### 15.1.1

##### G3 Flash Sharing

In this mechanism, the SPI lines from flash part are connected to both SOC and EC either directly or switch. Due to security concerns and flash access limitation, this is the least recommended option in all the flash sharing mechanisms.

- The **RSMRST#** from EC is used for controlling the flash access and switched only once during G3 exit.
- EC accesses the SPINOR only when **RSMRST#** is asserted and tri-states the SPI lines on de-assertion.
- On G3 exit (with **RSMRST#** asserted) EC loads the entire image in its internal SRAM and releases **RSMRST#** for SOC to access the flash. This doesn't require eSPI to be operational.
- Some isolation FETs required if SOC doesn't tristate the lines when **RSMRST#** is asserted.



**Figure 68 : G3 Flash Sharing high level block diagram**

#### 15.1.1.1 Flash update

- Requires host to update the EC region in shared SPINOR without EC involvement.
- Update is like any other OEM regions like BIOS.
- Host can support Full image update or EC region update.
- UEFI Capsule update is the minimum requirement with BIOS signature verification.
- FW recovery
  - Intel SOC is not responsible for EC FW recovery.
  - OEMs may support through alternate options
    - Use other interface that is active in S5 (typically used in service center)
    - Implement non updatable block (ROM) in EC that brings up the system to SO for flash update.

#### 15.1.2 Master Attached Flash Sharing (MAF)

MAF is one of the Flash sharing mechanisms where SOC is the master which access flash over SOC SPIO Controller and EC sharing the same flash will access over eSPI. MAF will be default the configuration for the PTL UH.

Here the SPI flash is connected to SOC and EC accesses the flash over eSPI.

- Requires eSPI interface to be up and initialized by both SOC and EC.

- On G3 exit, EC de-asserts RSMRST#(GPIO055), initializes eSPI, reads its image from SPINOR over eSPI, loads into its internal SRAM and notifies PCH. This is handled by the ROM in EC chip before giving control to the downloaded FW image.
- The downloaded flash image continues the power sequencing until SOC is out of reset and BIOS starts executing.
- This flash sharing mechanism also allows access during runtime which is handled by the downloaded EC FW image.
- Soft strap in descriptor to restrict EC to access EC FW region only.
- EC image Offset 1000H.

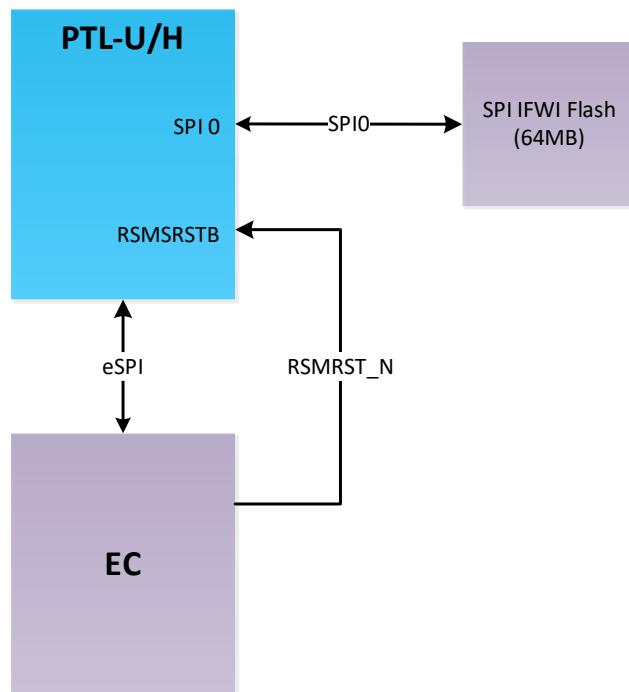


Figure 69 : MAF high level block diagram

#### 15.1.3

#### Slave Attached Flash Sharing (SAF)

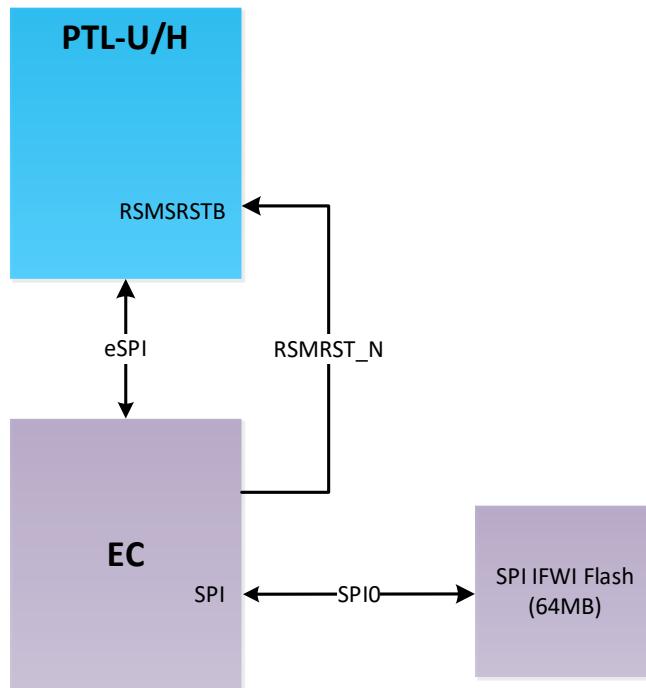
SAF is one of the Flash sharing Mechanism where EC is the master which access flash over its SPI Controller and PCH sharing the same flash will access over eSPI. MEC1723 Microchip Embedded Controller can support SAF mode flashing. Rework is required on RVP to support SAF.

PTL SOC is allocated dedicated regions (for each of the supported masters) within the eSPI slave-attached flash devices. SOC has read, write, and erase access to these regions, as well as any other regions that maybe permitted by the region protections set in the Flash Descriptor. The Slave will optionally perform additional checking on SOC provided address. In case of an error due to incorrect address or any other issues it will synthesize an unsuccessful completion back to the eSPI Master.

The SAF supports Flash Read, Write and Erase operations. It also supports the RPNC, Read SFDP and Read JEDEC ID commands.

In this topology, the SPI flash is connected to EC and SOC accesses the flash over eSPI.

- On G3 exit, EC loads its entire image into its internal SRAM, verifies the image (if supported as root of trust), and then de-asserts RSMRST# for PCH/SOC to access flash over eSPI.
- EC must meet the timing requirements for the SAF to avoid FW access latencies to avoid any impact to responsiveness or boot time.
- EC should enable the access to regions based on soft straps in the descriptor.



**Figure 70 : SAF high level block diagram**

## 16 Low Power Sub Systems (LPSS)

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Initial allocation of each port is given in the block diagram of the respective sub-sections.

**Disclaimer:** The LPSS architecture is yet to be finalized. There are changes expected, and same will be updated.

**Notes:**

1. For probing these signals, testpoints will be provided by opening the via masks on the SOC side. For the device side, series resistors or pull ups close to the device will be used for probing. If there are no components available near the end device for probing, then the test points will be provided closest to the device. However, if the testpoints are adding additional vias and violate the SI guidelines, then testpoints will not be provided.
2. For all the serial interfaces, for only one of the ports, A dummy test structure consisting on VCC pull up resistor (empty), load capacitor to ground(empty) and 0- ohm series resistor(populated) sharing pads as close as possible to SOC side and device side will be implemented.
3. Following options are not provided on RVP for any of the LPSS / ISH / Serial interfaces:  
TLA footprint, midbus probes, Beagle headers, Aardwark support.
4. The mapping of ports and GPIOs will be same for all the RVP SKUs to ease software effort.  
Deviations will be mentioned in the specific sections.

### 16.1 I2C/I3C

The SOC implements 6 I2C controllers for 6 I2C interfaces (I2C0-I2C5), capable of maximum bit rate of 3.4 Mbps (High-speed mode). Each interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock (SCL). The following are the constraints considered for I2C mapping:

1. Camera sensors and touch screen / touch pad cannot be on the same I2C bus.
2. Each camera connector needs a separate I2C bus to avoid address conflict since all the camera sensors have same I2C address. In older platforms the address conflict is resolved by doing a rework and a software work around. But on PTL this needs to be fixed. Hence allocating one I2C per camera connector in PTL RVP.

Each I2C interface can support the following Speed & power options:

- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- Fast mode plus (up to 1 Mbps)
- High speed mode (up to 3.4 Mbps)
- 1.8V support only

PTL supports 3- I3C interfaces and I3C interface.

- Support backward compatibility for Fast Mode and Fast Mode Plus. Slave device clock
- stretching is not supported.
- Single Data Rate (SDR) 12.5 Mbps, Dual Data Rate (DDR) 25 Mbps
- Support In-band Interrupt (IBI)
- Support Hammock Harbor time synchronization

**Table 55: I2C/I3C device mapping**

Bus	Device Mapping
I3C (Debug BPK I3C)	Modular TCSS TCP0 I3C Debug, I3C 1X4 HDR
I2C 0/ I3C 0	1X4 HDR, MECC AIC, SPD as I3C0
I2C 1/ I3C 1	CRD1 - UF RGB/IR Camera as I2C1
I2C 2/ MFUART 2	CRD2- WF RGB/ Macro Camera as I2C 2
I2C 3/ UART1/ ISH UART1A	Track PAD/ Audio/ PSS/ Power meter as I2C3
I3C 3A/ Display Sideband	Display sideband GPIO
I2C 4/ THC0_SPI1/THC_I2C0	Touch Panel Con 1 (THC_I2C0 & THC0_SPI1 mode)
I2C 4A/ ISH I2C 2/ MFUART0	Sensor Header (ISH_I2C2)
I2C 5/ THC1_SPI2/THC_I2C1	Touch Panel Con 2 and Touch PAD (THC_I2C1 & THC1_SPI2 mode)
I2C 5A/ MFUART 0/ ISH GP	ISH GPIO's

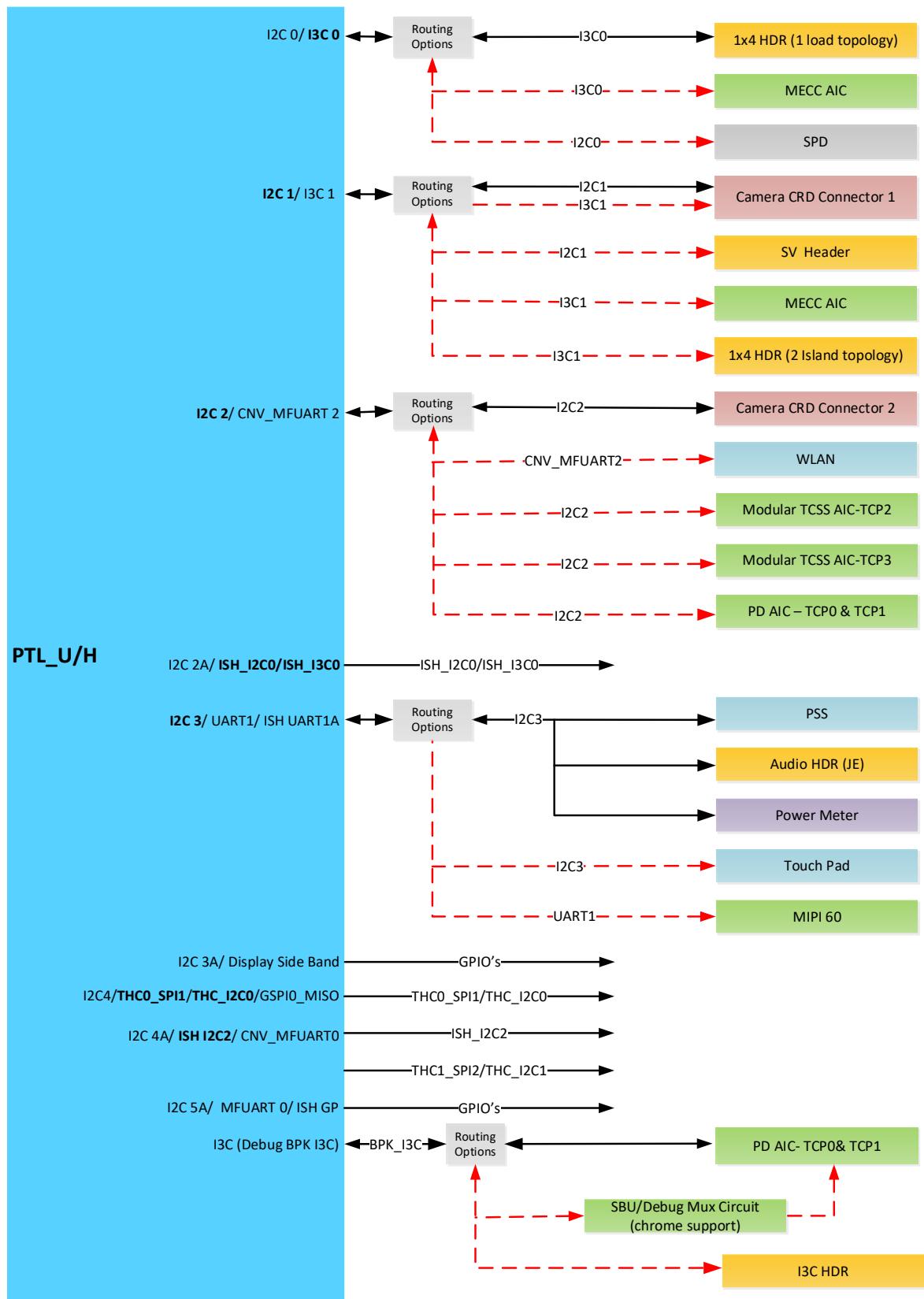


Figure 71: LPSS I2C/I3C high level Block Diagram

### 16.1.1

### I2C Device Details

The table below provides the devices connected to the LPSS I2C/I3C subsystem.

**Table 56: I2C/I3C device details**

Device	Speed	7 Bit address Set	7 Bit Address Options	I2C IO Voltage
Touch Pad	400KHz/1MHz	0x2C	0x2C	3.3V
Touch Panel-2	400KHz/ 1MHz	0x5C (General Study)	0x5C	1.8V
Touch Panel-1	400KHz/ 1MHz	0x5C (General Study)	0x5C	1.8V
Cam_Connector-1	400KHz	0x4D	0x4D	1.8V
Cam_Connector-2	400KHz	0x49	0x49	1.8V
PSS	400KHz	0x6E	0X68 or 0x6A or 0X6C or 0X6E	1.8V
Power meter Chip#1	100KHz/ 400KHz/ 1MHz ( FM+)	0x18	Configurable through resistor	1.8V
Power meter Chip#2	100KHz/ 400KHz/ 1MHz ( FM+)	0x12	Configurable through resistor	1.8V
Power meter Chip#3	100KHz/ 400KHz/ 1MHz ( FM+)	0x1E	Configurable through resistor	1.8V
Power meter Chip#4	100KHz/ 400KHz/1MHz ( FM+)	0x1D	Configurable through resistor	1.8V
Power meter Chip#5	100KHz/ 400KHz/1MHz ( FM+)	0x11	Configurable through resistor	1.8V
Power meter Chip#6	100KHz/ 400KHz/1MHz ( FM+)	0x15	Configurable through resistor	1.8V
Power meter Chip#7	100KHz/ 400KHz/1MHz ( FM+)	0x19	Configurable through resistor	1.8V
Power meter Chip#8	100KHz/ 400KHz/1MHz ( FM+)	0x14	Configurable through resistor	1.8V
Power meter Chip#9	100KHz/ 400KHz/1MHz ( FM+)	0x17	Configurable through resistor	1.8V
FRU EEPROM	100KHz/400KHz	0xAD(Read), 0xAC (Write)	Configurable through resistor	3.3V

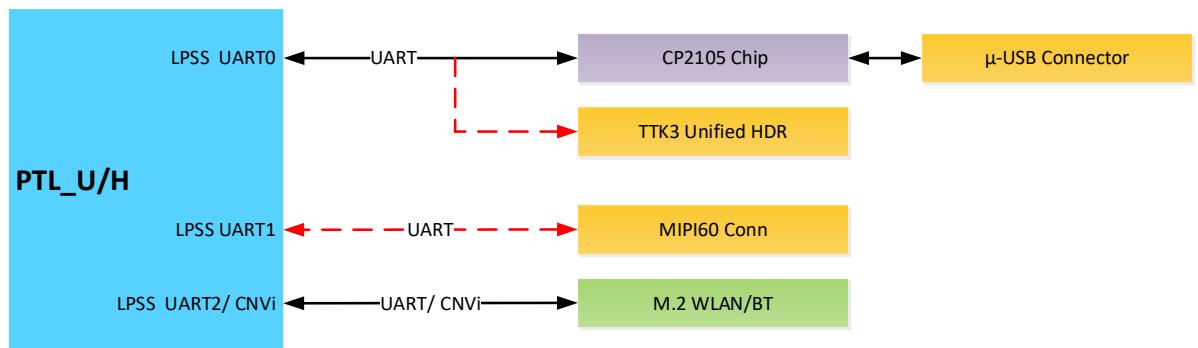
### 16.2

### UART

The LPSS Subsystem includes 3 UART ports. The UART ports communicate with serial data port devices compatible with the RS-232 interface protocol. The device map for the LPSS-UART interfaces on PTL\_U/H are as shown below.

**Table 57: UART Device details**

Bus	Device Mapping
UART 0	Serial Debug Port /TTK3
UART 1/ ISH UART 1A/ I2C 3	Track PAD/ Audio/PSS/ Power meter/MIPI60 as I2C3
UART 2/ CNVi	M.2 BT module CNVi

**Figure 72: LPSS UART Block Diagram**

## 16.3 GSPI

There is no dedicated header in PTL RVP for GSPI. The GSPI signals are Multiplexed with THC SPI. Since THC is POR for PTL, only THC based touch connections will be provided on RVP. GSPI based touch support is not provided.

# 17 Imaging – CSI Camera

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## 17.1 CSI Camera

For PTL-U/H, CSI data and clock lanes originate from SOC. The SOC has 3 CLKOUTs for the camera.

PTL-UH RVP will have two CRD-60 connectors, CRD1 connected with CSI x4 ports and CRD2 with CSI x2 ports. The PTL PHY supports CSI-2 D PHY v2.1 and CSI-2 C PHY v2.0. The Camera sensors may be connected through CSI-2 over C-PHY or CSI-2 over D-PHY conduit options. Platform allows for a flexible configuration allowing each of the camera modules to use X1, X2, or X4 CSI-2 over D-PHY port, or T1, T2, T3 (Trios) CSI-2 over C-PHY port. Different RVP SKUs were provided to validate C-PHY as well as D-PHY due to routing differences.

The customer coverage is more for D-PHY than C-PHY and C-PHY is focused on premium segments. Hence C-PHY is supported on one SKU - RVP3 and rest all RVP SKUs supports D-PHY. Also, PPV team looks for both C-PHY and D-PHY validation on single RVP. The D-PHY can be run over C-PHY routing. So T4 RVP3 SKU will be having C-PHY pinout on both CRD connectors

Apart from this, the Connector CRD1 also have 3PE Altek AON ULP Vision AIC support.

PTL-UH supports CRD1 and CRD G3 AICs. No support for CRD G4 due to the unavailability of extra clock from the silicon.

A new C-PHY AIC design is under development which is similar to CRD-D1 but with C-PHY routing. This card will be used in RVP3 C-PHY Board for C-PHY module validation.

### Changes in PTL with respect to MTL

To accommodate the G3 functionality, the **placement** of CRD1 and CRD2 connector has been swapped in PTL compared to MTL. In MTL, each CRD connector supports two x2 lanes whereas PTL have this two x2 support on one CRD connector. The other CRD connector have only one x2 lanes.

**Table 58: CSI Port and Connector Mapping with G3 AIC**

PTL CRD	MTL CRD	CRD G3
CRD Conn 1 (Port A & B)	CRD Conn 2 (Port E & F)	J4 (UF & IR)
CRD Conn 2 (Port C)	CRD Conn 1 (Port A & B)	J3 (WF)

Table 59: Configuration support each PTL U/H RVP

CRD CONNECTOR	RVP3: T4 PCB LP5 MD SKU	Rest all SKUs: RVP1, RVP 1a, RVP2, RVP4
CRD Connector 1	CSI C-Phy 3T (D-PHY support TBD)	CSI D-PHY x4
CRD Connector 2	CSI C-PHY 2T (D-PHY support TBD)	CSI D-PHY x2
ULP Vision support	No support for Altek ULP Vision	Altek AL8100 / Synaptics Sabre AON (Always ON). Muxed with CRD1 Conn.

**Note:** PPV team have enabled Chimera AIC & adapter board to support validation of DPHY IP over C-PHY CRD Connector in RVP3

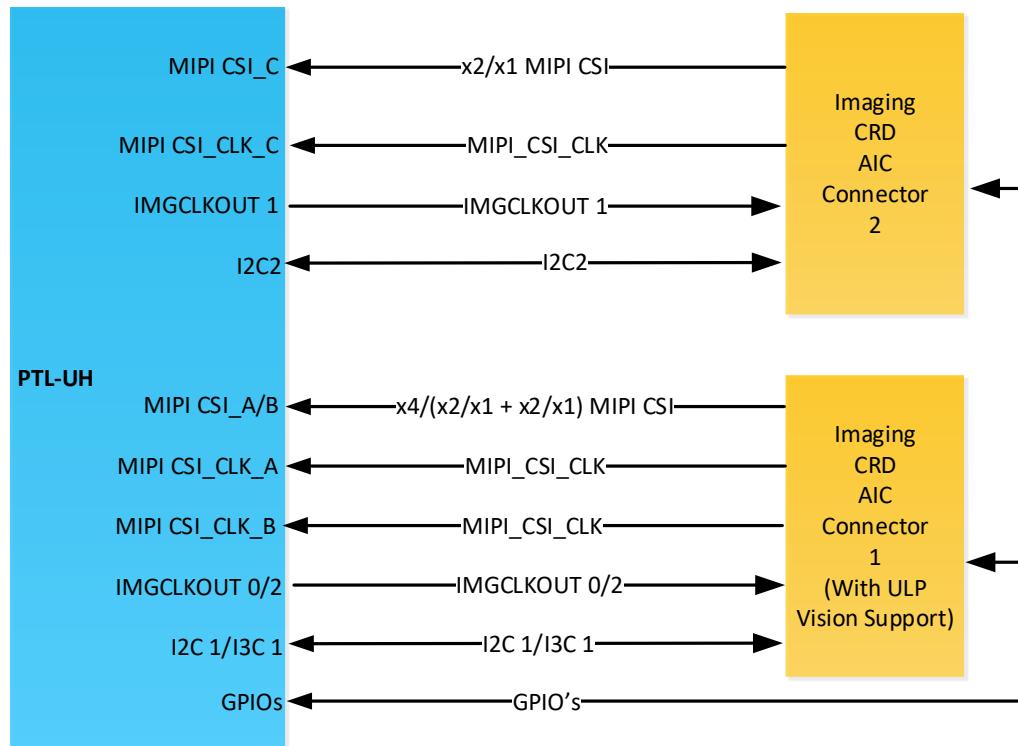


Figure 73: PTL-U/H CSI D-PHY imaging support high level block diagram

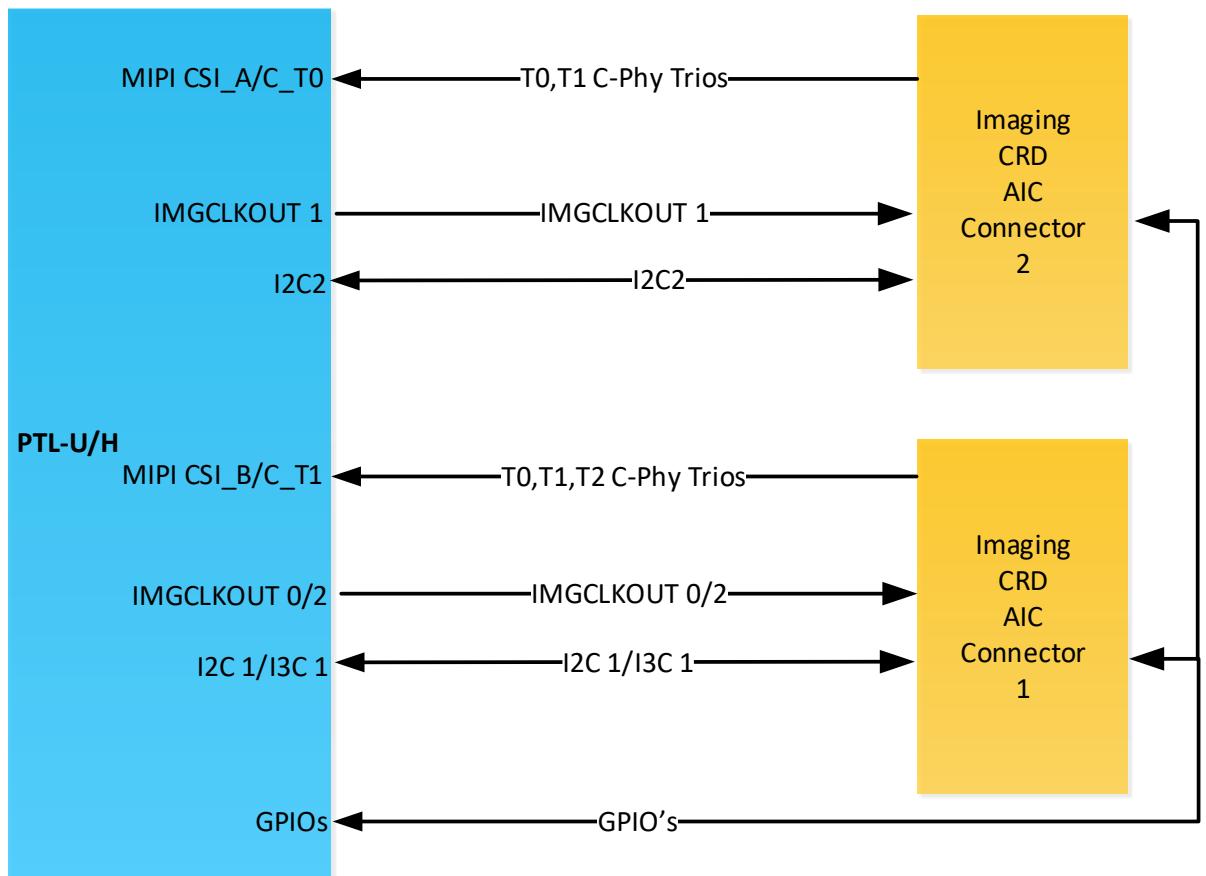


Figure 74: PTL-U/H CSI C-PHY imaging support high level block diagram

The camera configurations for PTL U/H are as below.

**Table 60: CRD connector supported configurations**

Lanes	RVP Connector	RVP Camera Configurations		
		D-PHY		C-PHY
CSI_A_D0_A0_P	CRD Conn 1	x2	x4	T0, T1, T2
CSI_A_D0_B0_N				
CSI_A_CK_C0_P				
CSI_A_CK_C1_N				
CSI_A_D1_A1_P				
CSI_A_D1_B1_N		x2	x2	T0, T1
CSI_B_D0_A0_P				
CSI_B_D0_B0_N				
CSI_B_CK_C0_P				
CSI_B_CK_C1_N				
CSI_B_D1_A1_P	CRD Conn 2	x2	x2	T0, T1
CSI_B_D1_B1_N				
CSI_C_D0_A0_P				
CSI_C_D0_B0_N				
CSI_C_CK_C0_P				
CSI_C_CK_C1_N				
CSI_C_D1_A1_P		x2	x2	T0, T1
CSI_C_D1_B1_N				

## 17.2

## CRD- 60 Connector Pinout

Given below is the CRD-60 connector pinout that will be used for PTL-U/H.

**Table 61: CRD-60 Connector pinout (D-PHY)**

RVP CRD Conn Pin Number	Pin Functionality	RVP CRD Conn Pin Number	Pin Functionality
60	GND	59	V3.3S Flash supply
58	CSI_LANE1_DP	57	V3.3S Flash supply
56	CSI_LANE1_DN	55	V3.3S Flash supply
54	GND	53	GND
52	CSI_LANE2_DP	51	GND
50	CSI_LANE2_DN	49	GND
48	GND	47	NC
46	CSI_CLK1_DP	45	GND
44	CSI_CLK1_DN	43	1.8V Power supply (DOVDD)
42	GND	41	1.8V (Ungated Power supply 1.8S)
40	CSI_LANE3_DP	39	MCF_USB2_DP
38	CSI_LANE3_DN	37	GND
36	GND	35	MCF_USB2_DN
34	CSI_LANE4_DP	33	GND
32	CSI_LANE4_DN	31	Sync stereo OUT
30	GND	29	Sync stereo IN
28	CSI_CLK2_DP	27	CRD_I2C_CLK
26	CSI_CLK2_DN	25	CRD_I2C_DATA
24	GND	23	Flash Trigger /Strobe
22	NC	21	Power on GPIO
20	NC	19	CAM Reset/ CVS Reset
18	NC	17	Clock Enable GPIO
16	NC	15	Privacy LED/CVS HOST WAKE
14	GND	13	Imaging Ref clock1
12	ISH_I2C_SCL / ISH_I3C_SCL	11	GND
10	PMIC_A1	9	Imaging Ref clock2
8	PMIC_A0	7	Altek ISH Interrupt
6	NC	5	Secure CAM SW
4	NC	3	GND
2	+V5P0_BOOST	1	ISH_I2C_SDA / ISH_I3C_SDA

**Note:** ALTEK M1 Supported

Table 62: CRD-60 Connector pinout (C-PHY)

RVP CRD Conn Pin Number	Pin Functionality	RVP CRD Conn Pin Number	Pin Functionality
60	GND	59	V3.3S Flash supply
58	CSI_T0_A0	57	V3.3S Flash supply
56	GND	55	V3.3S Flash supply
54	CSI_T0_B0	53	GND
52	GND	51	GND
50	CSI_T0_C0	49	NC
48	GND	47	NC
46	CSI_T1_C1	45	GND
44	GND	43	1.8V Power supply (DOVDD)
42	CSI_T1_B1	41	1.8V (Ungated Power supply 1.8S)
40	GND	39	NC
38	CSI_T1_A1	37	NC
36	GND	35	NC
34	CSI_T2_A2	33	GND
32	GND	31	Sync stereo OUT
30	CSI_T2_B2	29	Sync stereo IN
28	GND	27	CRD_I2C_CLK
26	CSI_T2_C2	25	CRD_I2C_DATA
24	GND	23	Flash Trigger /Strobe
22	CSI_T3_C3	21	Power on GPIO
20	GND	19	CAM Reset/ CVF Reset
18	CSI_T3_B3	17	Clock Enable GPIO
16	GND	15	Privacy LED/CVF HOST WAKE
14	CSI_T3_A3	13	Imaging Ref clock1
12	GND	11	GND
10	PMIC_A1	9	Imaging Ref clock2
8	PMIC_A0	7	NC
6	NC	5	NC
4	NC	3	GND
2	+V5P0_BOOST	1	NC

**Note:** Change from D-PHY is highlighted in RED (Altek /Synaptics is not supported)

## 17.3

### ALTEK M1 AIC Support (AON ULP VISION) / Synaptics Sabre AIC

Even though MCF is Zbbbed, the platform still supports AON ULP Vision sensing through 3PE AIC.

Altek AIC which uses AL8100 chip (aka SUNNY M1) is used to serve the purpose. Few signals which were used for MCF support is repurposed here for Altek AIC. Rest of the signals were removed from the CRD connector.

The platform also supports USB aggregation through CRD connector. The sideband signals can be aggregated and sent it to the silicon as USB signals. La Jolla cove USB adapter card is used for the same. This card can be directly plugged into the CRD connector.

**Note:** Despite RVP's support for Altek M1 AIC, the POR was switched to Synaptics Sabre AIC due to low customer adoption of Altek. Please contact CVS team for latest update and Block Diagram.

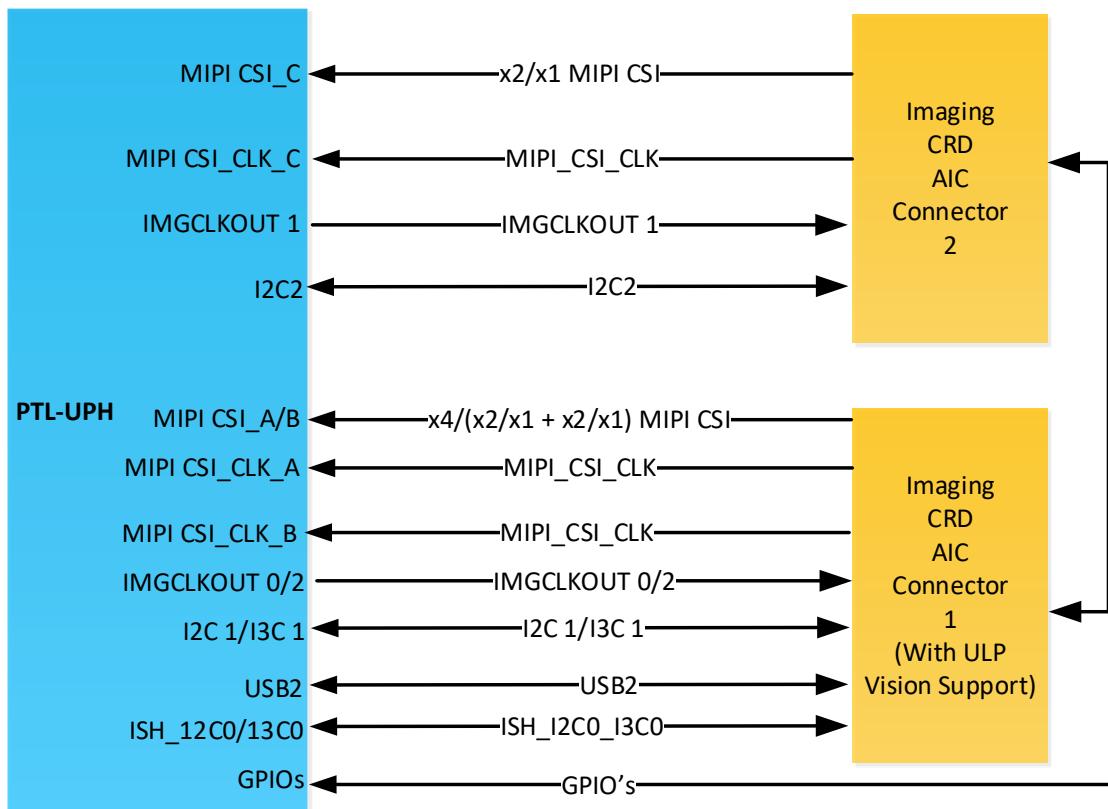


Figure 75 :Altek / Synaptics AIC support high level block diagram

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*USB2 interface over CRD AIC is mandatory for Synaptic Sabre AIC & for Altek M1 AIC it can be connected from Type-A port to D21 card.*

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**Table 63: Altek Pin Definition on CRD-60 Connector**

RVP CRD Conn Pin Number	Pin Functionality	RVP CRD Conn Pin Number	Pin Functionality
60	GND	59	V3.3S Flash supply
58	CSI_LANE1_DP	57	V3.3S Flash supply
56	CSI_LANE1_DN	55	V3.3S Flash supply
54	GND	53	GND
52	CSI_LANE2_DP	51	GND
50	CSI_LANE2_DN	49	GND
48	GND	47	NC
46	CSI_CLK1_DP	45	GND
44	CSI_CLK1_DN	43	1.8V Power supply (DOVDD)
42	GND	41	1.8V (Ungated Power supply 1.8S)
40	CSI_LANE3_DP	39	Sabre_USB2_DP*
38	CSI_LANE3_DN	37	GND
36	GND	35	Sabre_USB2_DN*
34	CSI_LANE4_DP	33	GND
32	CSI_LANE4_DN	31	Sync stereo OUT
30	GND	29	Sync stereo IN
28	CSI_CLK2_DP	27	CRD_I2C_CLK
26	CSI_CLK2_DN	25	CRD_I2C_DATA
24	GND	23	Flash Trigger /IR LED Strobe
22	NC	21	CRD PWREN
20	NC	19	CAM RST / CVS RST
18	NC	17	CAM CLK EN
16	NC	15	Altek Host Wake
14	GND	13	Imaging Ref clock1
12	ISH_I2C_SCL / ISH_I3C_SCL	11	GND
10	PMIC_A1	9	Imaging Ref clock2
8	PMIC_A0	7	CVS ISH Interrupt
6	NC	5	Secure CAM SW
4	NC	3	GND
2	+V5P0_BOOST	1	ISH_I2C_SDA / ISH_I3C_SDA

**Note:**

1. Grey colored signals are not applicable to Altek Vision
2. USB2 interface over CRD AIC is mandatory for Synaptic Sabre AIC & for Altek M1 AIC it can be connected from Type-A port to D21 card.

## 17.4

### POR Camera List

Below are the current set of POR camera sensor/Modules defined for PTL U/H, which are subject to change. Please refer to the platform BOM in section, Platform HW BOM for more details on the supported Camera Sensor list.

**Table 64: PTL U/H Camera Sensor list**

Vendor	Module Part Number	Details
OmniVision	OV13B10	WF\UF RGB – 13MP 2D Camera
OmniVision	OV01A1s (via SB2.5a)	RGB-IR: Legacy from previous project
OmniVision	OG0VA1B	UF IR Camera

**Note:** POR camera sensor/Modules are subject to change. Design of Transfer cards or imaging kits for the mentioned Camera sensors is not in the scope of RVP team.

# 18 Integrated Sensor Hub (ISH)

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## 18.1 ISH Sensors

Following sensors are selected for validation on PTL U/H and will be hosted on the MoSAIC Gen 2 card. The details of ISH and MoSAIC Gen 2 card are discussed in subsequent sections.

*Note: PTL uses exactly same sensors which is used in LNL*

**Table 65: List of Sensors and Kit details on PTL RVP**

Sensors	BOM1	BOM2
3-axis Accelerometer	Bosch BMI323	ST LSM6DSV16
3-axis Magnetometer	Memsic MMC5603NJ	AKM AK9919C
3-axis Gyroscope		ST LSM6DSV16
Barometer/Altimeter		ST LPS22DF
ALS	Vishay VCNL4030	ST VD6283
RGB/XYZ	-	ST VD6283
SAR - Proximity	Semtech SX9331	Semtech SX9331
Short Proximity	Vishay VCNL4030	
IR		ST VD6283
UV		
2nd Accelerometer	Bosch BMA422	ST LIS2DW12
Humidity		
Temperature		
HAL switch	Rohm BU52072GWZ	Rohm BU52072GWZ
Heart rate/Sp02		
Shock		ST LSM6DSV32
ECG		
Human Presence	ST VL53L7	Infineon BGT60TR13C
User temperature		
	Extender MoSAIC	Extender MoSAIC
	Extender Sensor	Extender Sensor
	Extender Beagle	Extender Beagle
	Samtec cable	Samtec cable
	Extender cable	Extender cable

**Note:**

- Samtec Cable: HQCD-030-12.00-TBL-SBR-1
- Extender Cable: 10-pin 2x5 Socket-Socket 1.27mm IDC (SWD) Cable (<https://www.adafruit.com/product/1675>)
- Uses same sensor BOM from LNL
- \* Supported by 3<sup>rd</sup> party vendor.

## 18.2

### Integrated Sensor Hub

The Integrated Sensor Hub (ISH) is a Soft IP that serves primarily as the connection point for the sensors on a platform. ISH is designed for the “Always-On, Always-Sensing” goal. PTL-U/H supports Integrated Sensor Hub (ISH 6.0). It contains the following interface to the sensors namely: I2C, I3C, SPI, UART, GPIO. It provides the following functions to support this goal.

- Acquisition / sampling of sensor data in all platform states including Sx and S0.
- Ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS/Applications.
- Low power operation through clock and power gating of the ISH blocks, including SRAMs, together with the ability to manage the power state of the external sensors
- The ability to operate independently when the host platform is in a low power state
- Compatibility with various operating systems,
- Ability to provide sensor-related data to other subsystems within the SOC, such as the CSME, Camera subsystem, Audio subsystem, etc.

ISH contains the following interface to the sensors namely: I2C, I3C, SPI, UART, GPIO.

- **ISH I2C:** ISH contains up to 3 I2C Ports capable of High-Speed Mode up to 1 Mbps.
- **ISH I3C:** ISH contains up to 2 I3C Port with HDR/DDR up to 24Mbps.
- **ISH SPI:** ISH contains 1 SPI port supporting speed up to 25 Mbps.
- **ISH UART:** ISH supports 2 UART ports capable of supporting operating speeds up to 4 Mbps.
- **ISH GPIOs:** ISH GPIOs are typically used for enabling the power to the sensor, detecting the interrupts from sensors etc. External pull ups will be provided for ISH GPIOs.

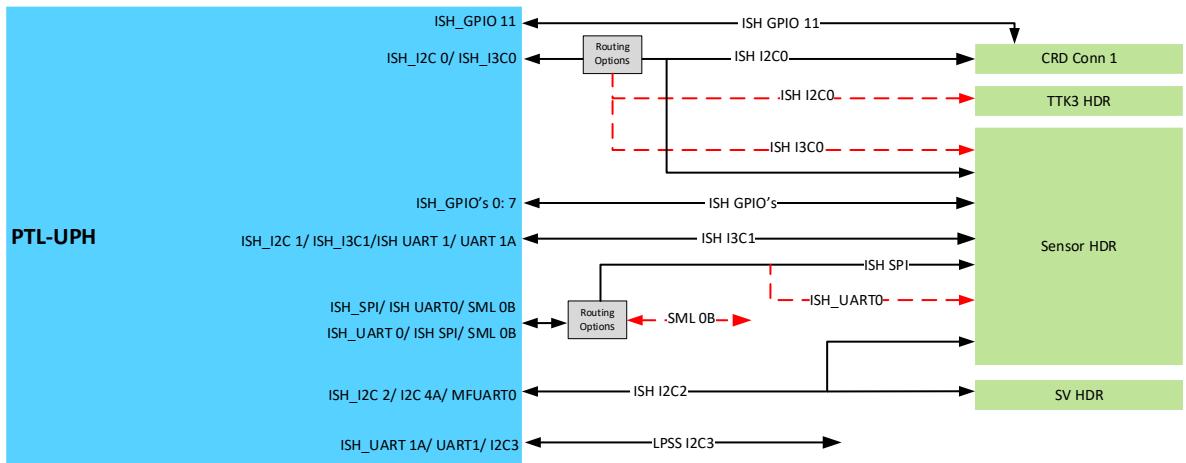


Figure 76: ISH Sensor Header high level block diagram

### 18.2.1 ISH I2C/I3C

The ISH supports three I2C controllers capable of operating at speeds up to 1 Mbps each. The I2C controllers are completely independent of each other: they do not share any pins, memory spaces, or interrupts.

The ISH's I2C host controllers also share the same general I2C port specifications:

- Master Mode Only (all peripherals must be slave devices)
- Support for the following operating speeds:
  - Standard mode: 100kbps
  - Fast Mode: 400kbps
  - Fast Mode Plus: 1Mbps
- Support 7-bit addressing formats on the I2C bus.
- FIFO of 64 bytes with programmable watermarks/thresholds

ISH I3C signal is muxed with ISH I2C.

Table 66: ISH I2C device mapping

Bus	Device Mapping
ISH_I2C 0/ ISH_I3C0	CRD Conn1 & Sensor HDR as ISH I2C 0/ I3C 0
ISH_I2C 1/ISH_I3C1/ ISH UART 1/ UART 1A	Sensor HDR / SV HDR as ISH I3C 1
ISH_I2C 2/ I2C 4A/ MFUART0	SNSR HDR / SV HDR as ISH I2C2

### 18.2.2 ISH UART

ISH supports 2 UART ports capable of supporting operating speeds up to 4 Mbps. ISH UARTs is used to generally connect the sensors related to GNSS (Global Navigation Satellite Systems) Ex: GPS. All the signals are routed to the sensor header.

**Table 67: ISH UART device mapping**

Bus	Device Mapping
ISH_UART 0/ ISH SPI/ SML 0B	Sensor HDR/MECC as ISH UART0
ISH_UART 1/ ISH I2C 1/ISH I3C1 UART 1A	Sensor HDR as ISH I3C1
ISH_UART 1A/ UART1/ I2C3	Track PAD/ Audio/ PSS/ TTK3/ MECC AIC as I2C3

### 18.2.3 ISH SPI

The ISH supports one SPI controller comprises of four-wired interface connecting the ISH to external sensor devices and port is routed to sensor header.

The SPI controller includes:

- Master Mode Only
- Single Chip Select
- Half Duplex Operation only
- Programmable SPI clock frequency range with maximum rate of 24 Mbps
- FIFO of 64 bytes with programmable threshold.

**Table 68: ISH SPI device mapping**

Bus	Device Mapping
ISH_SPI/ ISH UART0/ SML 0B	Sensor HDR as ISH SPI

### 18.2.4 ISH GPIOs

ISH GPIO's are typically used for enabling the power to the sensor, detecting the interrupts from sensors etc. External pull ups will be provided for ISH GPIOs. Up to 11 dedicated GPIOs can be used from ISH.

### 18.2.5 ISH Header

PTL-UH will use the MoSAIC Gen2 board. Modular Sensor Add-In-Card (MoSAIC) Gen 2 is an add-in card to enabling connecting different sensors to sensor-enabled platforms. Its main purpose is to connect sensors to ISH (Integrated Sensor Hub aka ISS, Intel Sensors Solution), but it can be used with other sensor solutions as well. MoSAIC Gen2 is a carrier card which means that no sensors are installed on MoSAIC itself. Instead, the MoSAIC Gen 2 card provides 15 DIP sockets, into each a 1-sensor card with one or more sensors can be plugged. Several switches soldered on the MoSAIC Gen2 board are used to route the sensor signals (I2C/SPI/UART/GPIO) to relevant platform (ISH) pins.

Please note that, the pullup voltage provided by the PTL RVP on pin 1 and 3 is 1.8V only. There is no support for 3.3V on these pins.

**Table 69: ISH Header Connector Pinout**

Pin name	Pin No	Pin No	Pin name
V1.8S_1.8A_SNSR_HDR	1	2	V3.3A_SNSR_HDR
V1.8S_1.8A_SNSR_HDR	3	4	V3.3A_SNSR_HDR
GND	5	6	V3.3A_SNSR_HDR
GSPI2_CS1_N_SNSR_HDR	7	8	GND
ISH_GP_7_SNSR_HDR	9	10	ISH_I2C1_SDA_SNSR_HDR
NC	11	12	ISH_I2C1_SCL_SNSR_HDR
GND	13	14	GND
NC	15	16	ISH_GP_1_SNSR_HDR
NC	17	18	ISH_GP_0_SNSR_HDR
GND	19	20	ISH_GP_6_SNSR_HDR
ISH_GP_3_SNSR_HDR	21	22	NC
ISH_I2C2_SCL_SNSR_HDR	23	24	NC
ISH_I2C2_SDA_SNSR_HDR	25	26	GND
GND	27	28	GND
GND	29	30	GND
NC	31	32	NC
NC	33	34	SAR_NIRQ_R
NC	35	36	ISH_GP_5_SNSR_HDR
V3.3A_WWAN_SAR	37	38	ISH_SPI_CS_N_SNSR_HDR
GND	39	40	NC
ISH_SPI_MOSI	41	42	ISH_GP_4_SNSR_HDR
ISH_SPI_MISO	43	44	ISH_SPI_CLK_SNSR_HDR
GND	45	46	HDD_PROT
NC	47	48	NC
GND	49	50	NC
NC	51	52	NC
NC	53	54	ISH_UART0_RTS_N
ISH_I2C0_SCL_SNSR_HDR	55	56	ISH_UART0_CTS_N
ISH_I2C0_SDA_SNSR_HDR	57	58	ISH_UART0_TXD
ISH_GP_2_SNSR_HDR	59	60	ISH_UART0_RXD

# 19 Touchscreen & Touchpad

## 19.1 Touchscreen

PTL U/H RVP will support 2 touch panels (1 per port) to support two 1x20 Headers on board that are not backward compatible to ADL RVP. These panel will support dual screen in as you can connect two screens to one RVP and have touch and pen work for both panels.

PTL U/H RVP shall support SPI based touch screen by default on Touch Panel Connector - 1 and it will support I2C based touch with reworks. Similar like LNL, Touch Panel Connector – 2 in PTL is by default connected to Touch-Pad connector as THC I2C. Therefore, Rework is required to enable the touch panel on Touch-Panel connector-2 (SPI or I2C). The configuration above is the desire BKC Default, which shall be configured in BIOS. Starting in MTL/ARL, there will be an internal Muxing of the PCH to switch between I2C/GSPI/THC on the HID Port. Therefore, the ability to switch these ports shall be supported in BIOS and configuration can be changed by user preference.

**NOTE:** Maximum on-board THC-SPI trace length is maintained as 8.2inch

The default power gating option is not provided for the POR touch panel as idle power requirement is on the low.

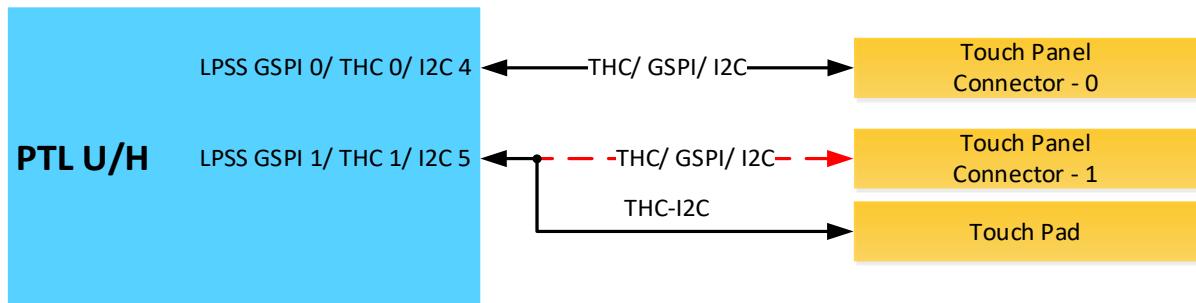


Figure 77 : Touch Panel high level block diagram

### 19.1.1 Touchscreen SPI / I2C header

The Pinout Details for the Touchscreen Header are provided below. Touch panel connector is different from ADL-P RVP Touch Panel connector but same as MTL connector.

Table 70: Touch Screen Header Pin-Out Details

Pin No	Functionality	Pin Description
1	THC SPI IO0	SPI MOSI (SPI signals)
2	I2C SCL	I2C based touch panel - I2C clock
3	THC SPI IO1	SPI MISO (SPI signals)
4	I2C SDA	I2C based touch panel - I2C data

5	THC SPI INT_N/I2C INT	Interrupt
6	THC SPI RST_N/I2C RST	Reset
7	GND	
8	THC SPI CLK	SPI signals
9	THC SPI CS	SPI signals
10	THC SPI IO2	SPI signals
11	THC SPI IO3	SPI signals
12	THC VDD PWR EN GPIO in	Loop back for RVP usage. Other usage is VISA
13	THC VDD PWR EN GPIO out	
14	VDD_3.3V	VDD - Power input to Touch controller
15	GND	
16	VDDSPI_1.8V	VDDSPI - SPI Power input to Touch Controller
17	Touch Pause Scan	Input to Touch panel to pause the scan
18	RESERVE	
19	I2C SPI MODE SEL	I2C/SPI Selection pin
20	HOOK[0] (CLTAP_PWRGOOD)	RSMRSTB

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*Note: Touch panel power header (1x4) will be removed from the RVP. This is because, 1.8V pins are allocated in the touch panel connector itself. So, switching between 3.3V and 1.8V power is no longer required.*

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### 19.1.2 Touchscreen Interrupt & Reset Mapping

For POR the default interface is 1.8V SPI interface and following signals from SOC/PCH are used as reset and interrupt.

**Table 71: Pin map for Reset & Interrupt for Integrated Touch Panel**

PCH GPIO	Function	Description	Voltage
TCH_PNL_RESET	Reset	<b>HIGH:</b> Out of Reset <b>LOW:</b> In Reset	PCH I/O voltage (No board level shifting)
TCH_PNL_INT	Interrupt	<b>HIGH:</b> No interrupt <b>LOW:</b> Interrupt	PCH I/O voltage (No board level shifting)

## 19.2 TouchPad

PTL U/H RVP provides a 1x12 pin header to interface the THAT based click pad. The Touchpad is interfaced to THC-I2C1 port at 3.3V through the level shifter on board. A rework option is provided from LPSS I2C-3 when THC-I2C1 port functions as Touch Panel.

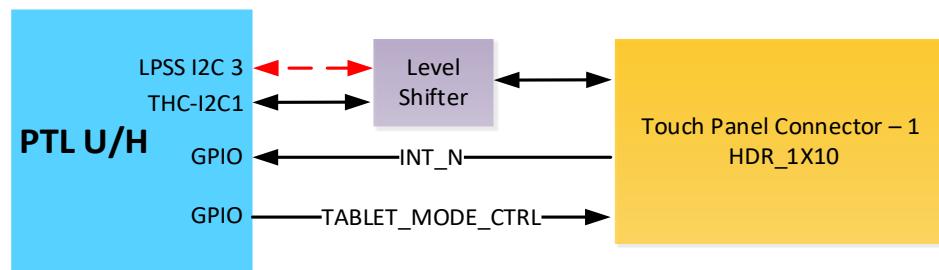


Figure 78: Touchpad high level block diagram

## 19.2.1

## Touchpad I2C Header

Table 72: 1x12 Header Pinout for Touchpad Interface

Pin No	Signal Name
1	+3.3V
2	+3.3V
3	+1.8V
4	I2C_SDA
5	TABLET_MODE_CTRL
6	I2C_SCL
7	GND
8	TP
9	TP
10	GND
11	GND
12	INT_N

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Note : The 5V will be removed from Touchpad connector. This is no longer used in latest touch pad. So pin 8 and 9 will NC in PTL

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# 20 Security

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Trusted Platform Module (TPM) is a Trusted Computing Group (TCG) low cost security solution to increase confidence on system security. The TPM is a device that resides on the motherboard and is connected to SOC/PCH using Serial Peripheral Interface (SPI) bus to communicate with the rest of the platform.

The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPM's are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a TPM provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions, and communication more trustworthy.

The PTL-UH RVP supports only SPI based TPM AIC. It doesn't support eSPI based TPM as no such device exists. LPC based TPM as LPC interface is no longer supported.

## 20.1 SPI based TPM

The PTL-UH RVP supports the discrete SPI TPM AIC over the primary SPIO interface that connects the SOC/PCH and the BIOS flash memory.

The SPI based TPM AIC should be plugged into the traditional 20pin BIOS flash header. The IPN of the 2x10 header is G25403-002 with pin definition given in below table.

**Table 73: Pinout Details for SPI based TPM**

Signal Name	Pin No	Pin No	Signal Name
KEYING	1	2	CHIP_SELECT_0
RSMRST	3	4	CHIP_SELECT_1
GND	5	6	+3.3A OR +1.8A
SPI_CLK	7	8	DQ2
DQ3	9	10	SPI_MISO
HOLD	11	12	SPI_MOSI
CHIP_SELECT_2	13	14	GND
WRITE_PROTECT	15	16	TP_SERIAL_IRQ
SPI TPM INT_N	17	18	+3.3A OR +1.8A
PLTRST	19	20	RSVD

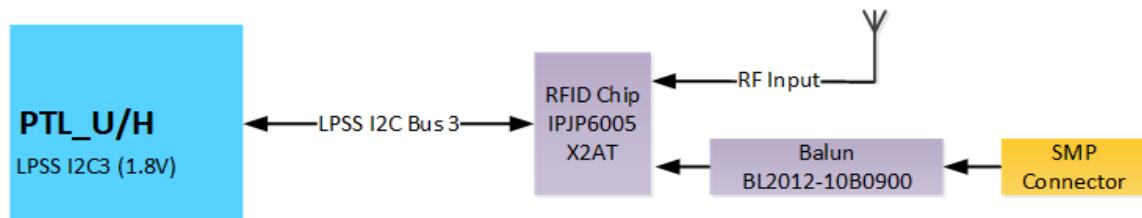
SPI TPM AIC hosts the SLB9670Tx chip from Infineon. It supports an SPI interface with a transfer rate of up to 43MHz. Its power management is handled internally; no explicit power-down or standby mode is required. The device automatically enters a low-power state after each successful command/response transaction. If a transaction is started on the SPI bus from the host platform, the device will wake immediately and will return to the low-power mode after the transaction has been finished.

## 21 PSS

PSS is Processor Secured Storage interface that is primarily intended for tracking the platform specific information in a factory like environment. The PSS interface enables platform specific information to be stored on the On-board memory (EEPROM) and access the stored information by either I2C or RFID reader. The information can be uploaded to a Central Database which will then be accessible by internal labs for the purpose of tracking and proactively reviewing current hardware and software status. Information like reworks implemented on the specific platform can be stored in the PSS EEPROM chip.

PSS interface design is a standard implementation on all Intel RVP boards and PTL-U/P/H RVP shall follow the same circuit and design as its predecessors.

The PSS chip should be able to be read by an external reader at a distance greater than 1 meter from the Platform that contains the PSS chip in an open environment.



**Figure 79: PSS Circuit high level block diagram**

The PTL-U/P/H RVP supports 8K memory size RFID chip with options for I2C connection from SOC.

The RVP supports both on board PCB Dipole antenna as well as the external Antenna options. The external antenna path will have the on board BL2012 series Balun chip from ACX. The PSS shall have the properties mentioned in the table below.

**Table 74: PSS Properties on MTL-M/P & ARL-P RVP**

Description	Value
<b>Memory Size</b>	<b>8kbit</b>
<b>Memory Configuration</b>	<b>12 x 128 NVM / OTP</b>
<b>I2C Interface</b>	<b>Device Driver-OS</b>
<b>Reader Communication</b>	<b>Gen2 RFID Commands</b>
<b>Antenna Bandwidth</b>	<b>900MHz</b>
<b>Antenna Type</b>	<b>Dipole, Monopole</b>

The SOC General Purpose Input/output (GPIO) signals are grouped into multiple groups (such as GPP\_A, GPP\_B, and so on) and are powered by the SOC/PCH Primary well. Many GPIO signals are multiplexed with other native functions.

The high-level features of GPIO:

- **Support 1.8V GPIO only**
- GPIO Serial Expansion (GSX) bus mux on existing GPIO pins
- All GP Input are capable of generating an IRQ interrupt based on software configured level or edge-triggered event
- All GP Input are capable of generating SCI
- All GP Input are capable of generating wake event
- Selective GP Input are capable of generating NMI or SMI#
- GPIO supports glitch free during power sequencing, and when switching mode of operation (see GPIO spreadsheet for pins with exception)
- Supports software configured GP Input polarity
- Supports GPIO mode input sensing (Rx) disable
- Supports GPIO mode internal weak pull configured for pullup, pulldown or none
- Support RCOMP for all GPIO pins (LP)
- Support Virtual GPIO for internal on-die connection between CNVi and LPSS, ACE, PCIe CLKREQ, and OC Virtual wire support

**Table 75: GPIO Power group mapping**

Power Group	Number of Pins	Remarks
GPP_A	16	
GPP_B	26	
GPP_C	24	
GPP_D	26	
GPP_E	21	
GPP_F	23	
GPP_H	21	
GPP_S	8	
GPP_V	18	

PTL-UH GPIO mapping document for all RVP SKU shall be captured in sharepoint [link](#).

All the SOC/PCH GPIO pins will be routed through resistor which will help in debugging.

## 22.1 RCOMPs

RCOMP's in PTL-U/P/H platform are listed below.

**Table 76: RCOMP Resistor Values**

Pin Name	Description	Termination
<b>DDI_RCOMP</b>	eDP PHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>SOC_REFRCOMP_ISCLK</b>	Connected to an external precision resistor for XCLK bias voltage generation	180 ohms 1%
<b>TYPEC_RCOMP</b>		200 ohms 1%
<b>PCIE4A_RCOMP</b>	analog connection point for an external bias resistor to ground	200 ohms 1%
<b>PCIE4B_RCOMP</b>	analog connection point for an external bias resistor to ground	200 ohms 1%
<b>USB3_RCOMP</b>	USB3 MPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>CSI_RCOMP</b>	CSI DPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>USB2A_RCOMP</b>	USB Resistor Bias, analog connection points for an external resistor to ground.	200 ohms 1%
<b>USB2B_RCOMP</b>		200 ohms 1%
<b>CNV_RCOMP</b>	WiFi DPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>SNDW_RCOMP</b>	SoundWire buffer RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>UFS_RCOMP</b>	UFS MPHY RCOMP, analog connection point for an external bias resistor to ground	200 ohms 1%
<b>DDR_RCOMP</b>		100 ohms 1%
<b>PCIE5_RCOMP</b>		200 ohms 1%
<b>PCIE5A_RCOMP</b>		200 ohms 1%

## 23 On board Hardware Straps

The PTL-U/P/H RVP takes care of the default hardware strap configuration for both CPU and PCH to ensure normal functionality. PTL-U/P/H RVP will provide on-board Pull-up/Pull-down resistor stuffing options for each strap. The strap configuration options along with default setting is given in below tables.

### 23.1 SOC Hardware Straps

SOC straps are mentioned in the table below.

**Table 77: PCH Hardware Strap Options**

GPIO #	When Sampled	Termination	HVM Strap	Pin Strap Usage	Polarity
<b>xxgpp_b_4</b>	RSMRSTB	20K PD	No	Flash descriptor security override (commonly referred as FDO strap)	Security measures defined in the Flash Descriptor is overriden if sampled high
<b>xxgpp_b_14</b>	PCH_PWROK	20K PD	No	Top swap override	Top Swap is enabled if sampled high
<b>xxgpp_b_23</b>	RSMRSTB	20K PD	No	"RTC" PLL (POR) or XTAL	Default RTC PLL distribution source 1 = 38.4MHz XTAL (Survivability usage only) 0 = "RTC" PLL @76.8MHz. This is the POR, and the default. *This pin strap is for survivability usage only, and expected to be further qualified with the "Personality Strap" aka "A0 only Strap" outside of GPIO prior to being used by iSclk.
<b>xxgpp_c_2</b>	RSMRSTB	20K PD	No	TLS Confidentiality Enable	TLS conf enabled if sampled high
<b>xxgpp_c_5</b>	RSMRSTB	20K PD	No	eSPI Disabled (previously called "EC-less Platform")	eSPI is disabled if sampled high
<b>xxgpp_c_15</b>	RSMRSTB	20K PD	No	XTAL Input Mode [0]	XTAL input mode 0: XTAL attached - <b>default</b> 1: Single-ended crystal input HVM/BI testing to pull-up this strap to select Single-Ended
<b>xxgpp_d_12</b>	PCH_PWROK	20K PD	No	No Reboot	No reboot if sampled high
<b>xxgpp_e_6</b>	RSMRSTB	20K PU	No	JTAG ODT Disable	JTAG ODT is disabled if sampled low
<b>xxgpp_e_9</b>	RSMRSTB	None	<b>Yes</b>	RTCPPLL Pre Divider Enable (HVM use only)	RTCPPLL Pre Divider Enable 0 – Bypass pre-divider (functional; 32.768KHz input) 1 – Enable /125 pre-divider (HVM; 4MHz input) *This strap is qualified by DFXTESTMODE

<b>xxgpp_e_10</b>	RSMRSTB	None	Yes	XTAL Input Frequency *HVM/BI mode only	Single-ended reference clock divider select 0 – Divider Bypass (functional) - <b>default</b> 1 – Divide by 4 (100MHz HVM mode) *This strap is qualified by DFXTESTMODE
<b>xxgpp_f_2</b>	RSMRSTB	20K PU	No	M.2 CNV modes / Integrated CNV Enable/Disable	M.2 CNV modes 0 = Integrated CNV enable 1 = Integrated CNV disable
<b>xxgpp_f_19</b>	RSMRSTB	20K PD	No	Skip RTC Clock Stabilization Delay (IOTG Boot Time Reduction)	Skip RTC Clock Stabilization Delay (IOTG Boot Time Reduction) 0 = No bypass (default) 1= Bypass/Skip 95ms RTC clock stabilization delay
<b>xxgpp_h_0</b>	RSMRSTB	20K PD	No	eSPI Flash Sharing Mode	Master attached flash sharing (MAFS) if sampled low, else slave attached flash sharing (SAFS)
<b>xxgpp_h_1</b>	RSMRSTB	20K PD	No	Enable/Disable SPI Flash Descriptor Recovery	Flash Descriptor Recovery for NIST SP800-193 0 - Flash descriptor recovery disable - <b>default</b> 1 - Flash descriptor recovery enable
<b>xxgpp_h_2</b>	RSMRSTB	20K PD	No	SPI Flash Descriptor Recovery Source - Internal/External	Flash Descriptor Recovery Source for NIST SP800-193 0 - Flash descriptor recovery internal source - <b>default</b> 1 - Flash descriptor recovery external source
<b>xxspi0_io_2</b>	RSMRSTB	20K PU	No	Consent Strap	Consent strap is enabled if sampled low
<b>xxspi0_io_3</b>	RSMRSTB	20K PU	No	Personality Strap (A0 only, disabled by RevID)	Personality strap is enabled if sampled low
<b>xxdbg_pmode</b>	RSMRSTB	20K PU	No	DFXTESTMODE active	Assert DFXTESTMODE to enable other straps to take effect if sampled low

## 23.2

## CPU Hardware Straps

No NOA signals from PTL-UH SOC.

## 24 Debug and Validation Hooks

A system could be debugged either via one of below methods:

- Open Chassis debug – this includes XDP, MIPI60 (LTB) with only one MIPI60 header on PTL RVP
- Closed chassis debug – USB debug (USB2/USB3/OOB/I3C)

This section of RVP HAS shall cover the overview of SoC debug architecture followed by debug interfaces of SoC that are supported in the RVP. It shall also list down various SoC validation hooks and cover all the validation interfaces that are supported in this PTL-UH RVP for users to debug the Silicon.

### 24.1 SoC Debug architecture - Introduction

PTL-UH SoC Architecture overview here.

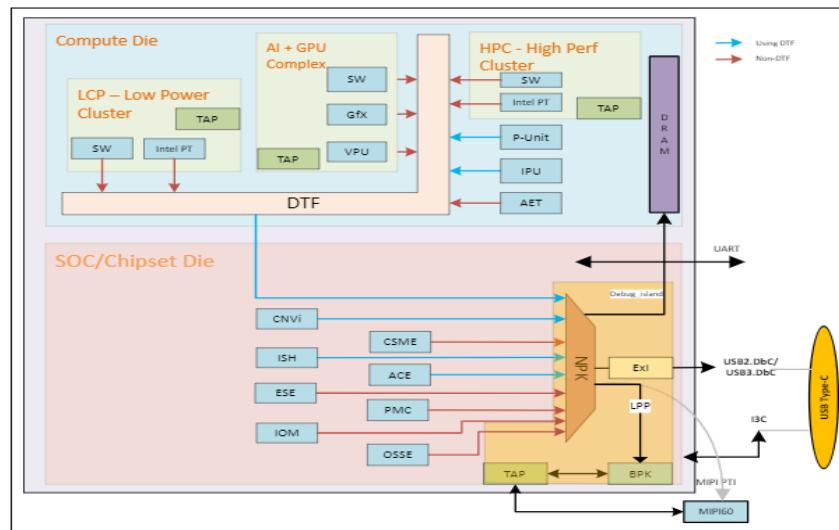


Figure 80: PTL-UH Debug Architectural Overview

PTL-UH has one High performance CPU, an Atom core cluster for efficient computing and an AI-GPU complex on the compute die. The VPU has been moved to the AI & GPU cluster.

The SoC/Chipset Die consists of NorthPeak (NPK) debug island and supports multiple debug interfaces like the USB/MIPI60/JTAG etc.

Debug Trace Fabric (DTF) is considered default bus to carry traces to NorthPeak (NPK). However, not all the trace sources support writing to DTF and their connection to NPK is shown in different colors.

## 24.2

## Boot flow debug

Boot flow debug is one of the most important debug scenarios to support. In general, boot flow referring to the period where power is supplied to the system, until first instruction fetches from CPU. Specifically, for PTL PCD, this period referring to RSMRST# de-asserted until PLTRST# de-asserted.

For PTL platform, boot flow is divided into 3 boot phases: Boot phase1 (Early boot phase), Boot phase2, and Boot Phase3. Boot phase1 is also call early boot phase. Refer to Fig : 70 for general boot flow.

To support boot flow debug, debug interface needs to be available to connect early enough in boot flow and has ability to temporary stop the boot flow for unlock and debug.

There are a few intercept points that a debug interface can halt the boot flow. These are "Platform Boot Stall", "CSE Boot Stall", "CPU Boot Stall", and IA main core reset break.

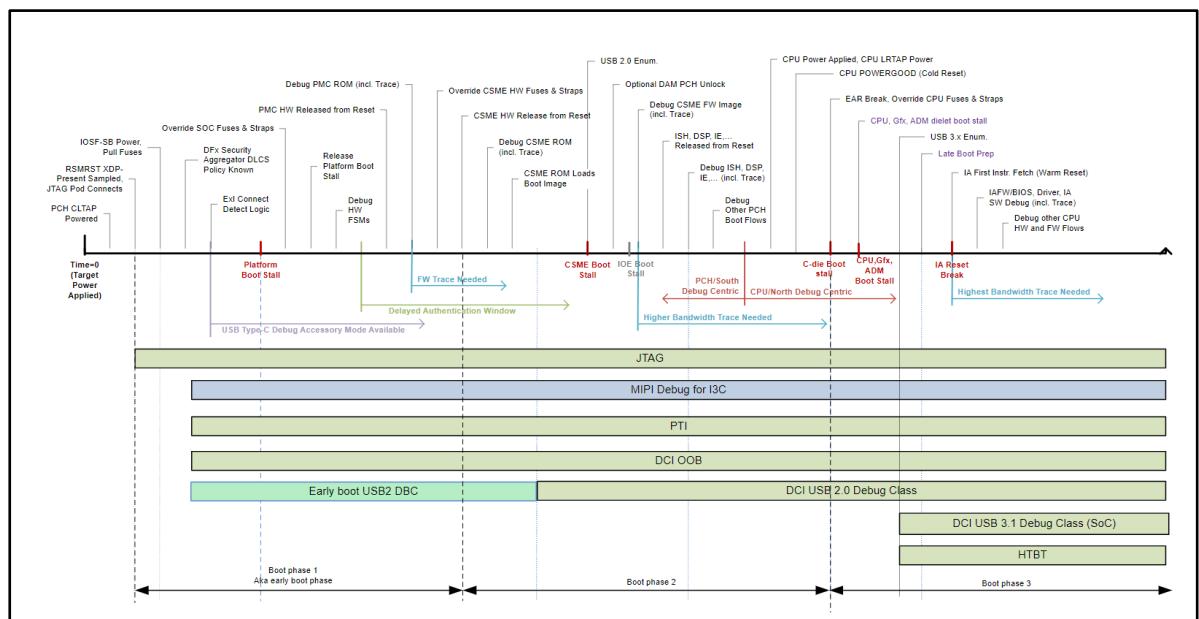


Figure 81: PTL-UH boot flow debug

Early boot phase is the earliest a debug interface may intercept PTL PCD in boot flow. This is known as platform boot stall. A few debug interfaces are required to support boot flow during early boot phase. There are external MIPI60 Debug Port connector, I3C debug and early boot USB2 DBC.

"CSE Boot Stall" is the next point where debug interface can intercept. As the name suggested, CSE Boot Stall happen when CSE is booting. However, per definition, CSE boot stall does not happen right from the beginning of CSE ROM starts, but instead, CSE Boot Stall happen during CSE RBE execution. All external MIPI60 Debug Port connector, and USB2 DbC supports CSE Boot Stall. Note that I3C Debug does not support CSE Boot Stall.

"CPU Boot Stall" are the same as previous client platform with CPU-PCH architecture.

After "CPU Boot Stall", PMC will continue the boot flow to bring up Host IP and Compute die. The "CPU Boot Stall" is equal to Phase-1a when Break signal asserted.

Following table show the debug interface and its earliest connection time w.r.t. boot flow.

**Table 78 : Boot Flow Debug vs. Debug Interface**

Support	MIPI60 connector	I3C Debug (SBU)	USB2 DbC	USB3 DbC
Platform Boot stall	Yes	Yes	Yes	No
CSE Boot stall	No	No	Yes	No
CPU Boot stall	Yes	Yes	Yes	No
IA main core reset break	Yes	Yes	Yes	No

## 24.3 Debug interfaces supported by SoC

**Table 79: PTL-UH RVP Debug Support**

Type	Interface Name	Supported in PTL-UH RVP
Open Chassis	JTAG (over MIPI60)	Yes
	MIPI-PTI (over MIPI60)	Yes
Closed Chassis	USB2 DbC (over Type C)	Yes
	USB2 DbC (over USB2 port)	Yes
	*OOB 2 wire (over Type C)	No*
	I3C Debug (over Type C)	Yes
	USB3 DbC (over Type C/Std-A)	Yes (Type-A & Type-C)

### 24.3.1

### SMP Mapping of Validation Hooks

Only one signal at a time can be connected to SMP connector after resistor stuffing rework.

**List of SMP signals mapped in T3 sku's (RVP1, RVP2 & RVP4):**

SoC pin name	RVP Signal Name	Connector
PCIE5_REF_PAD_CLK_P	PCIE_GEN5_REF_PAD_CLK_DP	SMP1
JTAG_PCD_MBPB_2	JTAG_PCD_MBPB_2_SMP	
VIEWPWR_1	VAL_VIEWPWR_1	
OBS0MON_ISCLK	VAL_OBS0MON_ISCLK	SMP2
GCD_VIEW_DIG_OUT_1	VAL_GCD_VIEW_DIG_OUT_1	
PCIE5_REF_PAD_CLK_N	PCIE_GEN5_REF_PAD_CLK_DN	SMP3
VIEWPWR_0	VAL_VIEWPWR_0	
GCD_VIEW_DIG_OUT_2	VAL_GCD_VIEW_DIG_OUT_2	
OBS1MON_ISCLK	VAL_OBS1MON_ISCLK	SMP4
GCD_HVM_CLK	VAL_GCD_HVM_CLK	
USB2_ID	USB2_ID	
XTAL_IN	XTAL_PCH_38P4M_IN	SMP5
XTAL_OUT	XTAL_PCH_38P4M_OUT	
DDR_VIEW[0]	VAL_DDR_VIEW_0	SMP6
JTAG_PCD_MBPB_0	JTAG_PCD_MBPB_0_SMP	
DDR_VIEW[1]	VAL_DDR_VIEW_1	SMP7
JTAG_PCD_MBPB_1	JTAG_PCD_MBPB_1_SMP	
DDR_ANA_VIEW	VAL_DDR_ANA_VIEW	SMP8
DLVR_PDMON0	VAL_DLVR_PDMON0	
HVMBCLK	VAL_HVMBCLK	
GCD_VIEW_DIG_OUT_0	VAL_GCD_VIEW_DIG_OUT_0	SMP9
JTAG_PCD_MBPB_3	JTAG_PCD_MBPB_3_SMP	
DLVR_PDMON1	VAL_DLVR_PDMON1	
VTARGET_0	VAL_VTARGET_0	SMP10
VIEWCLK_1	VAL_VIEWCLK_1	
VIEWCLK_0	VAL_VIEWCLK_0	SMP11
VTARGET_1	VAL_VTARGET_1	

**List of SMP signals mapped in RVP3 – T4 sku:**

SoC pin name	RVP Signal Name	Connector
PCIE5_REF_PAD_CLK_P	PCIE_GEN5_REF_PAD_CLK_DP	SMP1
JTAG_PCD_MBPB_2	JTAG_PCD_MBPB_2_SMP	
VIEWPWR_1	VAL_VIEWPWR_1	
GCD_VIEW_ANA_OUT_0	VAL_GCD_VIEW_ANA_OUT_0	
<hr/>		
OBS0MON_ISCLK	VAL_OBS0MON_ISCLK	SMP2
GCD_VIEW_DIG_OUT_1	VAL_GCD_VIEW_DIG_OUT_1	
<hr/>		
PCIE5_REF_PAD_CLK_N	PCIE_GEN5_REF_PAD_CLK_DN	SMP3
VIEWPWR_0	VAL_VIEWPWR_0	
GCD_VIEW_DIG_OUT_2	VAL_GCD_VIEW_DIG_OUT_2	
<hr/>		
OBS1MON_ISCLK	VAL_OBS1MON_ISCLK	SMP4
GCD_HVM_CLK	VAL_GCD_HVM_CLK	
USB2_ID	USB2_ID	
GCD_VIEW_ANA_OUT_1	VAL_GCD_VIEW_ANA_OUT_1	
<hr/>		
XTAL_IN	XTAL_PCH_38P4M_IN	SMP5
XTAL_OUT	XTAL_PCH_38P4M_OUT	
<hr/>		
DDR_VIEW[0]	VAL_DDR_VIEW_0	SMP6
JTAG_PCD_MBPB_0	JTAG_PCD_MBPB_0_SMP	
GCD_VIEW_ANA_IN_0	VAL_GCD_VIEW_ANA_IN_0	
<hr/>		
DDR_VIEW[1]	VAL_DDR_VIEW_1	SMP7
JTAG_PCD_MBPB_1	JTAG_PCD_MBPB_1_SMP	
GCD_BGR_VIEWANA_1	VAL_GCD_BGR_VIEWANA_1	
<hr/>		
DDR_ANA_VIEW	VAL_DDR_ANA_VIEW	SMP8
DLVR_PDMONO	VAL_DLVR_PDMONO	
HVMBCLK	VAL_HVMBCLK	
GCD_BGR_VIEWANA_0	VAL_GCD_BGR_VIEWANA_0	
<hr/>		
GCD_VIEW_DIG_OUT_0	VAL_GCD_VIEW_DIG_OUT_0	SMP9
JTAG_PCD_MBPB_3	JTAG_PCD_MBPB_3_SMP	
DLVR_PDMON1	VAL_DLVR_PDMON1	
GCD_BGR_TRIM_REF	VAL_GCD_BGR_TRIM_REF	
<hr/>		
VTARGET_0	VAL_VTARGET_0	SMP10
VIEWCLK_1	VAL_VIEWCLK_1	
GCD_VIEW_ANA_IN_2	VAL_GCD_VIEW_ANA_IN_2	
<hr/>		
VIEWCLK_0	VAL_VIEWCLK_0	SMP11
VTARGET_1	VAL_VTARGET_1	
GCD_VIEW_ANA_IN_1	VAL_GCD_VIEW_ANA_IN_1	

## 24.4 Generic RVP debug features

### 24.4.1 Open Chassis Debug

Debug used for interfaces that are not placed inside a closed system is referred to as Open Chassis Debug.

Types of Open Chassis:

- MIPI PTI
- JTAG

The MIPI PTI & JTAG signals are over the MIPI 60 Connector.



**Figure 82: MIPI60 Debug Port (Samtec QSH-030-01 series)**

The MIPI 60 Debug Port Interface enables communication between the Target System and Debug Tools. The MIPI 60 connector has power pins, JTAG, UART, I2C clock & data signals and different active low signals like POWER\_BUTTON\_N, CPU\_EARLY\_BREAK\_N, PLATFORM\_BOOT\_STALL\_N, Single RESET\_N, RESET\_BUTTON\_N to initiate a target system cold boot, to stall the CPU boot sequence at the earliest CPU stall point to perform pre-boot configurations to Intel CPU's, to stall the platform boot sequence at the earliest stall point to perform pre-boot configurations to Intel PCH's and SoC's, to determine various Reset and Power states on the Target System, to initiate a Target System warm-reset without cycling power cycles respectively.

#### 24.4.1.1 MIPI60 Debug Connector

PTL supports 4 channel VISA debug capability. Channel 3 & 4 VISA signals will be routed to MIPI 60 connector. Whereas Channel 1 & 2 VISA signals are muxed with Touch signals & will be routed to new Touch connector.

PTL RVP will support a single MIPI 60 connector for debug. PTL does not have NOA signals.

The PTL-UH RVPs will have support for MIPI 60 debug port with optional SOC/PCH –VISA only signals routed to a MIPI 60 connector & Touch connector.

Note- SOC/PCH JTAG will be routed to MIPI-60 Debug connector.

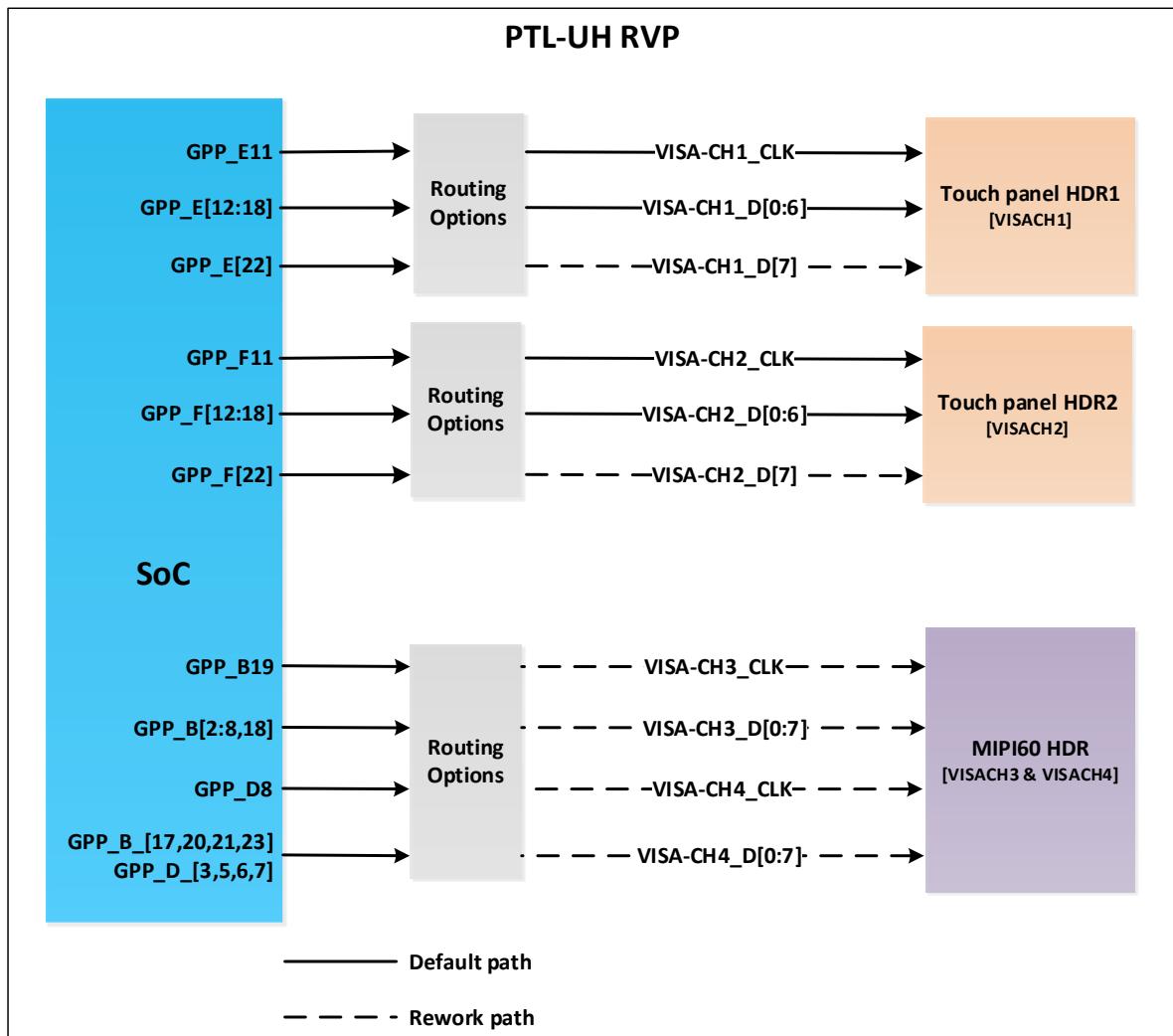


Figure 83: PTL-UH RVP VISA connections

Table 80: SoC VISA MIPI60 Connector Pinout

MIPI60 Pin#	Intel DPS Generic Signal name	PTL-UH Target Signal Name
3	TCK0	JTAG_PCD_TCK
51	TCK1	Res OE pull-down to GND
9	TRST_N	JTAG_PCD_TRST_B
2	TMS	JTAG_PCD_TMS
5	TDI	JTAG_PCD_TDI
4	TDO	JTAG_PCD_TDO
10	PREQ_N	PREQ_B
11	PRDY_N	PRDY_B
8	TRST_PD	Defensive pull-down
42	HOOK[0] (CLTAP_PWRGOOD)	RSMRST_B
36	HOOK[3] (BOOT_HALTI_N)	BOOTHALT_B

7	HOOK[6] (PMODE)	DBG_PMODE
38	HOOK[2] (EAR_N strap)	Test point
15	POD_PRESENT1_N (SOC)	SPI0_IO_2 (Strap)
17	POD_PRESENT2_N (PCH DEBUG_CONSENT_N Strap)	Defensive pull-down
40	HOOK[1] (POWER_BTN_N)	Power_button_n
6	HOOK[7] / nReset (RESET_BTN_N)	Reset_button_n
34	RSVD[1]	No Connect
55	HOOK[8]	JTAG_PCD_MBPB_0
53	HOOK[9]	JTAG_PCD_MBPB_1
13	PTI_0_CLK	GPP_B_19
19..33 odd	PTI_0_DATA[0..7]	GPP_B_[2:8,18]
59	PTI_3_CLK	GPP_D_8
35..49 odd	PTI_0_DATA[8..15] / PTI_3_DATA[0..7]	GPP_B_[17,20,21,23] GPP_D_[3,5,6,7]
14	PTI_1_CLK	GND
18..32 even	PTI_1_DATA[0..7]	No Connect
60	PTI_2_CLK	GND
44,46	RSVD[2..3]	No Connect
52	RSVD4	+V3P3A_VAL
54	DBG_UART_TX	UART1_TXD
56	DBG_UART_RX	UART1_RXD
48	I2C_SCL	SMB_CLK_S4
50	I2C_SDA	SMB_DATA_S4
1	VREF_DEBUG	+VCCIO_TERM_V1P25
12	VREF_TRACE	V1P8A
16	GND	GND
57	GND	GND
58	GND	GND

#### 24.4.2

#### Closed Chassis Debug

Debug using functional connections available in the complete, closed, form-factor system is referred to as Closed Chassis Debug.

Types of Closed Chassis:

- Debug over USB 2.0
- Debug over USB 3.0
- Intel 2W DCI
- Debug for I3C

#### 24.4.2.1

#### Debug over USB 2.0

The Debug Class over USB 2.0 is supported on all USB 2.0 ports and uses the native USB protocol to transmit. USB2.0 debug class does require the use of the TS functional xHCI controller.

USB2 DBC Port 1 has enhanced capabilities beyond other USB2 ports and should be connected to an easily accessible USB Type-C port so these new features can be utilized. These features are enabled because USB2 DBC Port 1 is in “Debug Island”. The features include:

- Able to connect very early in the boot sequence to support Connect First/Authorized Debug unlocks

- Able to remain connected and active during low power events (Sx and S0iX)

- Connection does not affect device going to low power.

- Since the Intel Trace Hub is also instantiated in Debug Island, traces can seamlessly transition over power cycling events

- Supports all other traditional connection and debug capability

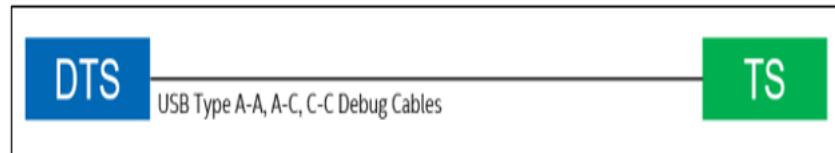
For the Debug Class over USB 2.0 to operate, the TS must have debug enabled and the TS USB port used must be in the UFP role. The Type C is configured to UFP role when the PD controller detects Debug Accessory Mode. DTS is in the DFP role and TS is in the UFP role. The Std-A port must have the USB2 port manually configured to the UFP role in the FW straps using the mFIT tool and can't be used as functional port when it's configured for debug.

#### 24.4.2.2

#### Debug over USB 3.0

The Debug Class over USB 3 is supported on all of the USB 3 ports from the PCH and CPU and uses the native USB protocol to transmit. USB 3 Debug Class does require the use of the functional controller. The Debug Class over USB 3 works over both Type A and Type C. However, Dfx is not supported on USB3 connection to the CPU. Only USB3.1 connection to the SOC supports Dfx.

The Debug Class over USB 3 is only available during the S0 power state. Debug Class over USB 3.1 is first available after the platform reset de-assertion and when the CPU is running. The Debug Class over USB 3 does not survive through Sx power state transitions and across warm and cold resets. When the Debug Class over USB 3.1 is connected, the system will not be able to exit the S0 power state into lower states.



**Figure 84: Illustrates the most basic connection between DTS and TS using just a USB Debug cable**

#### 24.4.2.3 Intel 2W DCI – (not supported in PTL)

Intel® DCI 2W DCI OOB uses the CCA adaptor combined with the “2W DCI OOB UART Adaptor” to convert USB signaling from the DTS to UART signaling to the TS. The Intel® 2W DCI OOB port is instantiated in the “Debug Island” power well which enables operation during early boot and through low power state transitions. 2W Intel® DCI OOB functions at low bandwidth, which supports Intel® JTAG Probe Mode like commands, Platform Boot Stall and run control but is too low for typical trace bandwidth. Intel® DCI 2W DCI OOB is a mature technology which is being replaced by the new platform debug connection called “Debug for I3C.”



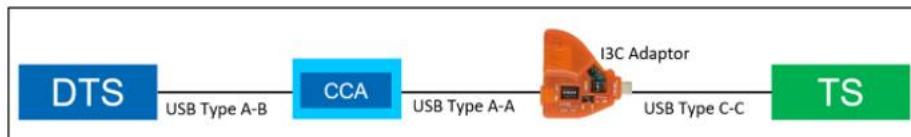
**Figure 85: 2W DCI OOB Connection**

Fig 72. illustrates the connection between the DTS and TS using 2W DCI.OOB. The DTS connects with the CCA device which converts the USB transport signaling into proprietary OOB (out of band) signaling. The CCA device passes these proprietary signals through the 2W DCI.OOB UART Adaptor which level shifts them and multiplexes them onto the SBU pins for presenting to the Target System.

#### 24.4.2.4 Debug for I3C

I3C is a new open standard protocol being used for inter-device communication. It extends traditional I2C by adding multi-mastering, higher speeds, and security protections. The MIPI I3C Debug Standard allows the I3C transport to send debug commands and have them intercepted and used to drive debug functionality. The primary use case is using a single I3C bus to interconnect all platform components to this debug transport. This allows a single connection to debug Intel’s SOC, Intel’s Discrete Graphic solution, and other compatible third-party devices. Since the MIPI I3C Debug Standard is public and scalable, third-party tool and device providers can freely use it to support platform debug.

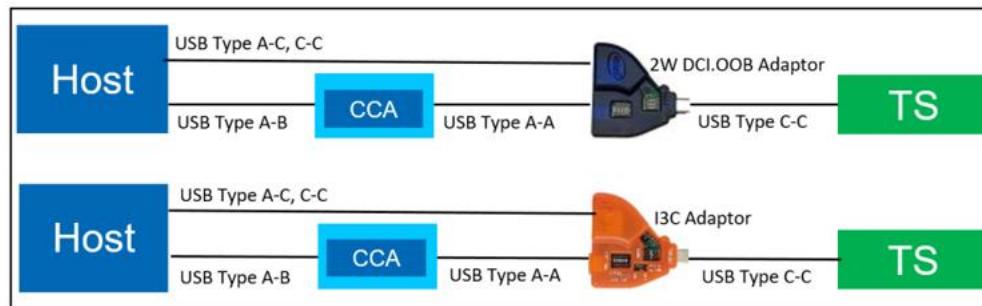
A big advantage of using “Debug for I3C” is Hot Connect. The “Debug for I3C” port can reliably connect upon fail and extract some triage information. If **DAM** is preset, then the system can be unlocked by Intel and more extensive debug performed.



**Figure 86: “Debug for I3C” Connection**

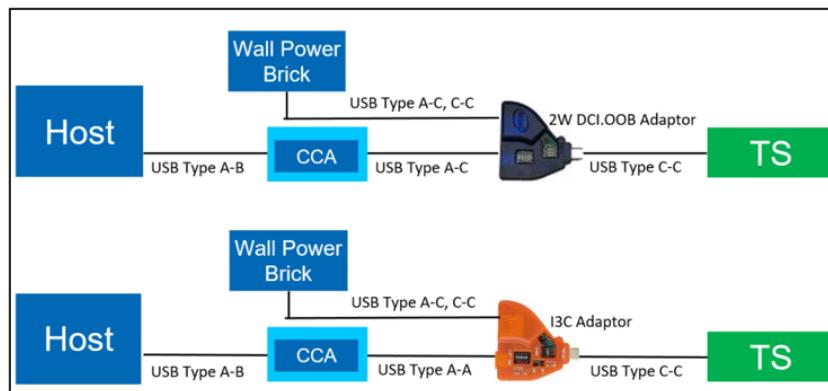
Fig 73. illustrates the connection between the DTS and TS using the “Debug for I3C” transport. The DTS connects with the CCA device which converts the USB transport signaling into proprietary OOB

(out of band) signaling. The CCA device passes these proprietary signals through the I3C Adaptor which converts them and multiplexes them onto the SBU pins for presenting to the Target System.



**Figure 87: Extending 2W DCI.OOB and Debug for I3C with USB DbC**

It is possible to multiplex USB3 DBC and USB2 DBC transports with either the 2W DCI.OOB or the “Debug for I3C” debug connections by routing a second USB port through the convertor. Fig 4 illustrates adding the additional connection. Caution, the TS USB port is set to Debug Accessory Mode, so the USB2 port is changed to an Upper Facing Port (UFP).



**Figure 88: Charging the TS while Debugging using 2W DCI OOB or Debug for I3C**

It is possible to power the USB port used for debug by plugging in a USB charging brick to the second port of the adaptors. Figure 5 shows some possible configurations.

#### 24.4.3

#### Debug features supported in RVP

**Table 81: Table depicting different debug interface supported in PTL**

Debug Feature	Description	Details
SINAII2	SINAII2 is used for voltage & current sensing, current pump channels and GPIO manipulations.	<a href="#">SINAII2/NEVO</a>
InTEC	InTEC is Integrated Thermal Environment Controller used for PECL and thermal monitoring of CPU and PCH thru the external InTEC AIC.	<a href="#">INTEC Header</a>
PM sideband header	Most of the power sequencing related signals are terminated on this header, which can be used for	<a href="#">PM Sideband Header</a>

	debugging purpose. This header now being used by the RVP DAC AIC card which helps to enable remote debugging.	
Port80 Display Output	The PTL-UH RVP supports the 4 digit 7-Segment LED display for Port80 debug messages	<a href="#">PORT80 Display Output</a>
Serial Debug Console	Serial debug console over a micro-AB USB 2.0 receptacle port	<a href="#">Serial Debug Console</a>
LED	LED indications for system states/status/errors.	<a href="#">LEDs</a>
RVP Health DAC	A novel way to access remote hardware & accelerate debug	<a href="#">RVP Health DAC</a>
UCP-SQUID	Low cost, Multi-Protocol and Remote programming solution	<a href="#">UCP-SQUID</a>
RVP NEST	RVP NEST is a remote access farm hosted and maintained by RVP Team	<a href="#">RVP NEST</a>
Box Stress Test	BST is an AIO integrated solution used for Voltage measurements, Voltage drive/margining, GPIO's manipulations, I2C master controller and Thermal Diodes measurements capabilities	<a href="#">Box Stress Tool</a>

#### 24.4.3.1 SINAII2/NEVO

SINAII2 is used for voltage & current sensing, current pump channels and GPIO manipulations. SINAII (believed to be the name of mountain where the Ten Commandments were given to Moses by God) is just an internal project name and does not have an acronym. The primary platform interface for SINAII2 is a 2x50, 100pin connector (IPN: D10221-001) for voltage margining and current sensing.

Sinai2 connectors has following types of pins:

1. GPIO: General purpose IOs. Can be configured as input or output and be configured as Open drain or CMOS.
2. GPIO-Fixed: IOs which should be routed to specific signals on the platform or stayed unconnected (if the feature is not needed). These have special topology which matches the relevant functionality.
3. DC3V3IO: General purpose IOs. Can be used to drive 3.3V signals. Good for stable signals (DC) like mux controls & straps. Currently only work as outputs.
4. ISNS [P/N]: Differential pair for sensing current through shunt resistors. Supports up to 160mV.
5. VSNS [P/N]: Differential pair for sensing voltage. Supports up to 3.2V in normal mode and 6.4V in extended mode.
6. IDRIV: Current pumps output for voltage margining. Can drive/sink up to 14mA.
7. SPCL: Special purpose pins, which are used for power/GND or other maintenance functions in Sinai2. They must be connected as stated in the pin map.

SINAII2 special pins:

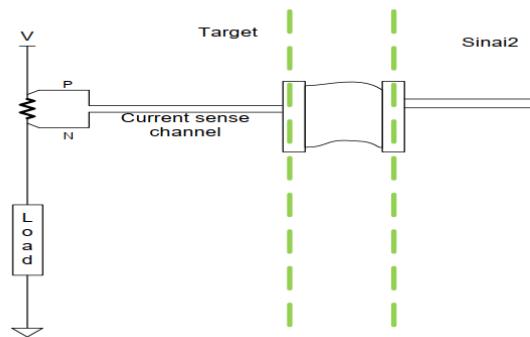
1. GND – should be connected to reference GND of the platform.

2. VCCST – should be connected to VCCST plane (normally 1.05V) for reference of SVID bus)
3. VCCIO – should be connected to VCCIO plane (normally 0.95V) for reference of MBP and all other GPIOs.
4. Setup done (pin 100 in sideband) – indicates that Sinai2 configuration is done and that the GPIOs are in programmed state. A good practice would be to connect this indication to the power sequence of the platform to prevent race between Sinai2 and other devices. Normally this signal is asserted ~900mS before CPU\_POWERGOOD (if powered from the same power supply)

The actual utilization of the Vsense, Isense, Idrive & GPIO channels of Sinai2 is platform dependent. The pinout and channel allocation of SINAI2 interface will be finalized after reviewing the requirements from VFT representative. Multiple options would be supported using optional resistors. Resistor based stuff/unstuff option must be included in any GPIO and Isense path to Nevo connector.

#### 24.4.3.1.1 Current Sensing Signals

Sinai2 senses current for measurement through the Sideband connector. Like in voltage sensing, the accuracy required from Sinai2 is very high. Moreover, in current sensing, Sinai2 is actually sensing low voltage levels (0-160mV) on a shunt resistor and errors and bPTL routed traces will result in wrong current reading. Max bus voltage is 3.2V (common mode voltage). P/N traces to be taken from phase sense resistor (P/N) similar to PnP HDR routing.



**Figure 89: Current Sense Implementation**

#### 24.4.3.1.2 Sense resistor selection

It is important to note that the sense resistor selected for this circuitry should enable Sinai2 to measure the entire (or the desired) range of current to the load. For that, the voltage on that resistor in maximum current condition should not exceed 160mV. For example, if the maximum current expected from a plane is 15A, then a good practice would be to select a 10mΩ sense resistor (Vishay WSK2512-0.010-1%-R86E3 can be used for this purpose). A larger resistor will

cause a cutoff in the range of sampling while a smaller resistor will cause degradation of the granularity and accuracy of the sampling.

#### 24.4.3.1.3 Routing Guidelines for Sense Signals

Sinai2 senses voltage rails for measurement through AVMC connector. The accuracy required from Sinai2 sensing is very high (less than 1mV), thus, the routing of the sense traces should get special attention. The Routing of AVMC sense signals will follow below guidelines:

- The Voltage sense traces should be routed as differential pair on the platform from the sensing point to the AVMC connector.
- The traces differential impedance should be 80-100 Ω.
- If the negative trace (the \*\_N trace) is to be connected to GND, then it should be connected to the GND plane as close as possible to the sensing point (e.g. the CPU) and routed differential with the positive trace (\*\_P).
- It is preferred that the traces will be routed directly to the connector, but if there is a need to place series resistors on the voltage sense traces, the resistance of these resistors should not be bigger than 100 Ω.
- The traces should be routed in internal layers as far as possible from noisy parts (coils, oscillators, high frequency signals etc.)

#### 24.4.3.1.4 SVID Signals to SINAI

SVID to SINAI2 connections are not part in any RVP SKUs of PTL-UH since no team using SVID VR margining or validation over SINAI2 connector

**Table 82: SINAI2 Connector pinout**

Pin #	Pin Name (Option1 / Option2)	Type	Pin #	Pin Name (Option1 / Option2)	Type
1	VSENSE_P<0>	VSNSP	51	GPIO3	GPIO
2	VSENSE_P<1>	VSNSP	52	BCLKP	GPIO - FIXED
3	VSENSE_N<0>	VSNSN	53	GND	SPCL
4	VSENSE_N<1>	VSNSN	54	GND	SPCL
5	VSENSE_P<2>	VSNSP	55	ISense5N	ISNSN

6	VSENSE_P<3>	VSNSP	56	VSENSE_P<11> / I2C_Slave_SCL	VSNSP/GPIOFIXED
7	VSENSE_N<2>	VSNSN	57	ISense5P	ISNSP
8	VSENSE_N<>	VSNSN	58	VSENSE_N<11> / I2C_Slave_SDA	VSNSN/ GPIO - FIXED
9	VSENSE_P<4>	VSNSP	59	ISense6N	ISNSN
10	VSENSE_P<5>	VSNSP	60	VSENSE_P<12>	VSNSP
11	VSENSE_N<4>	VSNSN	61	ISense6P	ISNSP
12	VSENSE_N<5>	VSNSN	62	VSENSE_N<12>	VSNSN
13	GPIO0	GPIO	63	I2C_Master_SCL	GPIO - FIXED
14	GPIO1	GPIO	64	I2C_Master_SDA	GPIO - FIXED
15	GND	SPCL	65	GND	SPCL
16	GND	SPCL	66	GND	SPCL
17	VSENSE_P<6> / SPI-MISO	VSNSP/ GPIO - FIXED	67	ISense7N	ISNSN
18	VSENSE_P<7> / SPI-MOSI	VSNSP/ GPIO - FIXED	68	ISense8N	ISNSN
19	VSENSE_N<6> / SPI-CLK	VSNSN/ GPIO - FIXED	69	ISense7P	ISNSP
20	VSENSE_N<7> / SPI-CS	VSNSN/ GPIO - FIXED	70	ISense8P	ISNSP
21	VSENSE_P<8>	VSNSP	71	GPIO4	GPIO

22	ISense0N	ISNSN	72	GPIO5 / PECI_MUX_CTRL	GPIO - FIXED
23	VSENSE_N<8>	VSNSN	73	CPU_PWRGD	GPIO - FIXED
24	ISense0P	ISNSP	74	PLT_RESETN	GPIO - FIXED
25	VSENSE_P<9>	VSNSP	75	GPIO6	GPIO
26	ISense1N	ISNSN	76	PLT_RESTARTN	GPIO - FIXED
27	VSENSE_N<9>	VSNSN	77	GND	SPCL
28	ISense1P	ISNSP	78	GND	SPCL
29	VSENSE_P<10> / PMSYNC	VSNSP/ GPIO - FIXED	79	ISense9N	ISNSN
30	CPU_SVID_OUT	GPIO - FIXED	80	ISense10N	ISNSN
31	VSENSE_N<10> / PECI_MON	VSNSN/ GPIO - FIXED	81	ISense9P	ISNSP
32	CPU_SVID_CLK	GPIO - FIXED	82	ISense10P	ISNSP
33	GND	SPCL	83	PROCHOT(Drive)	GPIO - FIXED
34	GND	SPCL	84	VSENSE_P<13>	VSNSP
35	CATERR	GPIO - FIXED	85	VSENSE_N<13>	VSNSN
36	CPU_SVID_ALRT	GPIO - FIXED	86	VSENSE_P<14>	VSNSP
37	PROCHOT	GPIO - FIXED	87	VSENSE_N<14>	VSNSN
38	THERMTRIP	GPIO - FIXED	88	GPIO7	GPIO

39	ISense2N	ISNSN	89	VCCST	SPCL
40	VRM_SVID_OUT	GPIO - FIXED	90	VCCST	SPCL
41	ISense2P	ISNSP	91	GPIO8 / IDRIVE9	GPIO/IDRV
42	VRM_SVID_CLK	GPIO - FIXED	92	IDRIVE0	IDRV
43	ISense3N	ISNSN	93	IDRIVE1	IDRV
44	GND	SPCL	94	IDRIVE2	IDRV
45	ISense3P	ISNSP	95	IDRIVE3	IDRV
46	VRM_SVID_ALRT	GPIO - FIXED	96	IDRIVE4	IDRV
47	ISense4N	ISNSN	97	IDRIVE5	IDRV
48	PECI	GPIO - FIXED	98	IDRIVE6	IDRV
49	ISense4P	ISNSP	99	IDRIVE7	IDRV
50	BCLKN	GPIO - FIXED	100	IDRIVE8 / PLT_SETUP_DONE	IDRV/SPCL

#### 24.4.3.2 INTEC Header

InTEC is Integrated Thermal Environment Controller used for PECL and thermal monitoring of CPU and PCH thru the external InTEC AIC. The platforms signals that enable the thermal control and monitoring are thermal DIODE signals and PECL signals from CPU and PCH. The platform connector part details are given in below table. Test points will be provided for PECL, FORCEPR# & THERMTRIP#, and CATERR# signals.

MFG	Mfg. Part Number	IPN
Molex	501190-3027	G94240-001
Molex	501190-3017	G24701-002

Figure 90: INTEC Connector PN

The RVP supports G94240-001 part by default. The design details are given below.

**Table 83: Platform Design Recommendations for InTEC signals**

pin#	InTEC signal name	RVP Signal Connection	Comments
1	THERMDA0_Sense	VAL_THERMDA0_S	Thermal Diode 1
2	THERMDC0_Sense	VAL_THERMDC0_S	
3	THERMDC0_Force	VAL_THERMDC0_F	
4	THERMDA0_Force	VAL_THERMDA0_F	
5	PROCHOT0	PROCHOT_MONO_INTEC_N	PROCHOT Copy (LVTTL)
6	GND	GND	
7	THERMDA1_Sense	VAL_GCD_THERM_DA_S	GCD Die Thermal Diode 2
8	THERMDC1_Sense	VAL_GCD_THERM_DC_S	
9	THERMDC1_Force	VAL_GCD_THERM_DC_F	
10	THERMDA1_Force	VAL_GCD_THERM_DA_F	
11	PROCHOT1_PECI Trigger	NC	
12	GND	GND	
13	THERMDA2_Sense	VAL_SOC_THERM_DA_S	SOC Die Thermal Diode
14	THERMDC2_Sense	VAL_SOC_THERM_DC_S	
15	THERMDC2_Force	VAL_SOC_THERM_DC_F	
16	THERMDA2_Force	VAL_SOC_THERM_DA_F	
17	PROCHOT2	NC	
18	GND	GND	
19	THERMDA3_Sense	VAL_THERMDA1_S	Thermal Diode 2
20	THERMDC3_Sense	VAL_THERMDC1_S	
21	THERMDC3_Force	VAL_THERMDC1_F	
22	THERMDA3_Force	VAL_THERMDA1_F	
23	PROCHOT3	NC	
24	GND	GND	
25	PECIO	CPU_PECI	PECI Interface
26	GND	GND	
27	VTTO	+VCCIO_TERM_V1P25_INTEC	
28	PECIO_Mux_Ctrl	*PECI Mux Ctrl	
29	PECI_Copy	**PECI PROBING	
30	GND	GND	

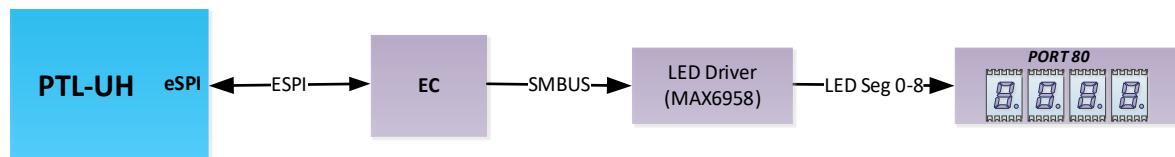
#### 24.4.3.2.1 PECI Signal

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components such as Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Assured Power (cTDP), and Memory Throttling Control

mechanisms and many other services. PECL is used for platform thermal management and real-time control and configuration of processor features and performance. PECL support eSPI is POR for PTL-UH. Refer [SINAL to CPU sideband optimization](#) section for PECL implementation in PTL-UH RVP.

#### 24.4.3.3 PORT80 Display Output

The PTL-UH RVP supports the 4 digit 7-Segment LED display for Port80 debug messages like all other previous generation RVPs. The Port80 LED driver will be SMBus based connected to the Embedded Controller (EC) on-board. The EC gets the port80 messages from PCH over the eSPI interface depending on the platform configuration.



**Figure 91: Port80 Functional Diagram**

A 2x8 16-pin header 2.54mm pitch provided on the RVP design to bring the Port80 LED signals to front panel for validation purpose.

**Table 84: SAS Header and Pinout**

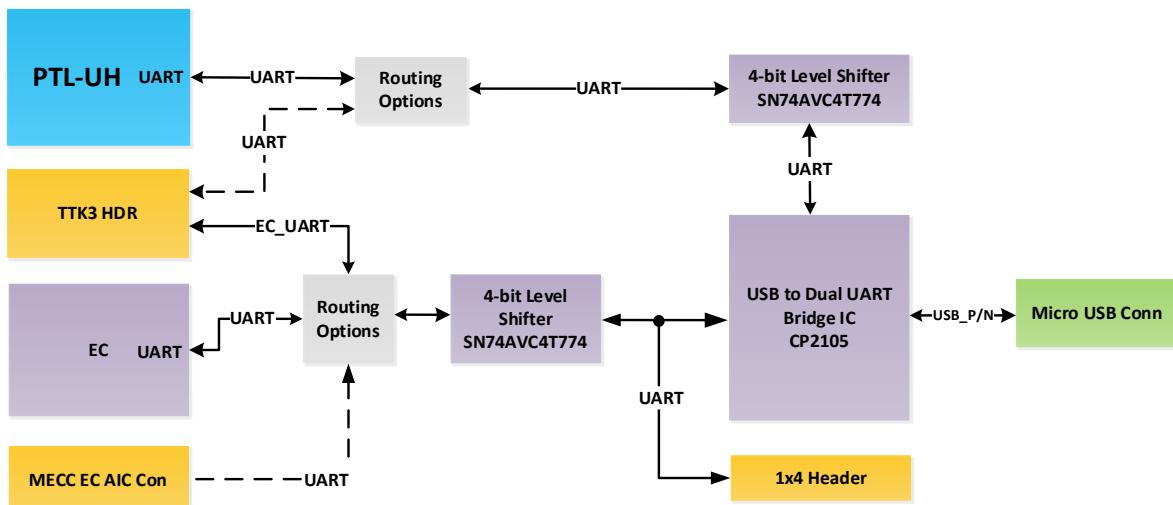
MFG	Mfg. Part Number	IPN Number
WIESON TECHNOLOGIES CO., LTD	AC2100-0009-005-HH	K92628-001

Signal Name	Pin #	Pin #	Signal Name
+V3P3A_R_VAL	1	2	LED_SEG8
GND	3	4	LED_SEG7
NO PIN	5	6	LED_SEG6
NC	7	8	LED_SEG5
NC	9	10	LED_SEG4
NC	11	12	LED_SEG3
RSVD_LED_SEG9	13	14	LED_SEG2
LED_SEGO	15	16	LED_SEG1

#### 24.4.3.4 Serial Debug Console

The PTL-UH RVP supports Serial debug console over a micro-AB USB 2.0 receptacle port. The RVP uses CP2105 Dual USB UART / FIFO IC for UART to USB2.0 conversion. The RVP will have option for EC and SOC/PCH connectivity for TX and RX signals while the CTS and RTS signals would be available from the SOC/PCH.V

Debug UART signals from EC shall be connected to mECC AIC connector and TTK3 connector as option in the design.



**Figure 92: Serial debug console high level block diagram**

**Table 85: Micro USB connector and Pinout**

MFG	Mfg. Part Number	IPN Number
Hirose	ZX62RD-AB-5P8(30)	E10610-003

Pin #	Signal Name
1	+V_VCC_USB_UART
2	USB_C_DEBUG_DM
3	USB_C_DEBUG_DP
4	NC
5	GND

#### 24.4.3.5 LEDs

The PTL-UH RVPs supports the following list of LEDs with their description given in below table

**Table 86: RVP LEDs & Function**

LED Name	Functional Description	LED Color
CAPSLOCK	Driven by EC to indicate the CAPSLOCK condition	GREEN
NUMLOCK	Driven by EC to indicate the NUMLOCK condition	GREEN
S0_LED_DRV	Indicates system entering state - S0	GREEN

S3_LED_DRV	Indicates system entering state – S3	GREEN
S4_LED_DRV	Indicates system entering state – S4	GREEN
S5_LED_DRV	Indicates system entering state – S5	GREEN
SUS_LED_DRV	Indicates system sleep state	GREEN
ME_LED_DRV	When asserted, INTEL ME is off	GREEN
CATERR	On board LED to indicate catastrophic event driven by CPU.	RED
M.2_WLAN_LED1	Indicates WLAN Module availability	GREEN
M.2_WWAN_LED	Indicates WWAN Module availability	GREEN
M.2_BT_LED2	Indicates BT Module availability	GREEN
PM_PWRBTN_LED	Driven by EC	GREEN
CHGR_LED_GATE_LED1	Driven By EC – Charging status	YELLOW
CHGR_LED_GATE_LED2	Driven By EC – Charging status	GREEN
CS_INDICATE_LED	Indicates whether system is in Connected Standby(CS)	GREEN
C10_GATE_LED	Indicated C10	GREEN
PCIE_LINK_DOWN	Indicates PCIe link down and will be routed to LED and to header	AMBER

**Table 87: PTL RVPs support following press buttons on board**

Button	Function
Volume UP	Volume increase input to EC (Provided over header)
Volume DOWN	Volume decrease input to EC (Provided over header)
Power	External Power button input to the PCH and EC
Reset	External Reset button input to the PCH

Power and Reset signals will be routed to Front Panel Header and PM Side band header.

In general, for debug connectors, Refdes and pin numbering will be provided. Silkscreen for signal names can't be supported. Also, default power on from G3 state (i.e., no need to press power button) will be supported.

## 24.5 Programming capabilities:

Devices programmable in RVP

- BIOS SPI Flash
- EEPROMs
- PD AIC
- Retimer Flash
- TTK3

- EC Flash
- Dediprog

## 24.6

### Details of debug tools

Debug support	Tool Description	Features
open chassis	Lauterbach Trace32 is used as the open chassis debug tool and connected via MIPI-60. The primary DTS is the CombiProbe v2 supporting merged JTAG and MIPI PTI.	<ul style="list-style-type: none"> <li>• Run-control</li> <li>• Trace extraction and analysis</li> <li>• Streaming trace via MIPI PTI (Intel Processor Trace)</li> <li>• CrashLog extraction and analysis</li> <li>• Custom Scripts(CScripts)</li> </ul>
closed chassis	Intel System Studio is the main debug tool for closed-chassis debug over USB and for tracing.	<ul style="list-style-type: none"> <li>• Run-control</li> <li>• Trace extraction and analysis</li> <li>• CrashLog extraction and analysis</li> <li>• Custom Scripts (CScripts)</li> </ul>

Source : [PantherLake Debug SAS \(intel.com\)](#)

Below table shows a list of probes, their associated cables and adapters dependencies. For more information refer to wiki link.

Tool	Description	Wiki link
XDP - Extensible Debug Port	The XDP, also known as XDP3, XDP3b, XDP3br, Pod, ITP Blue Box is a JTAG debug adapter	<a href="#">XDP - Extensible Debug Port - Debug Tools Support - Intel Enterprise Wiki</a>
CCA - Closed Chassis Adapter	CCA (Closed-Chassis Adapter) is one of the two ways of connecting the host and the target in the DCI (Direct Connect Interface) topology.	<a href="#">CCA - Closed Chassis Adapter - Debug Tools Support - Intel Enterprise Wiki</a>
DbC - Debug Cable	DbC (Debug Cable) is one of the two ways of connecting the host and the target in the DCI (Direct Connect Interface) topology	<a href="#">DbC - Debug Cable - Debug Tools Support - Intel Enterprise Wiki</a>
LCP - Low Cost Probe	The LCP - Low Cost Probe, is a probe manufactured by Lauterbach for Intel. It is similar in function to the Combi-Probe, but it has functional limitations built in which make it suitable for automation only, and not usable for regular debug.	<a href="#">LCP - Low Cost Probe - Debug Tools Support - Intel Enterprise Wiki</a>

LTB - Lauterbach Combiprobe	The Combiprobe is a third-party developed JTAG probe built by Lauterbach (LTB) that can be used with Intel or Lauterbach's proprietary software; Trace32 and Powertrace.lt connects to a MIPI60 JTAG connector or to a USB DCI connection via an adapter.	<a href="#">LTB - Lauterbach Combiprobe - Debug Tools Support - Intel Enterprise Wiki</a>
UTAG - USB JTAG Probe	The UTAG4, is a JTAG debug adapter that works with PVT/OpenIPC. In simple terms, it acts as a bridge between a host system and a target platform. It is a very low-cost alternative to most of the other JTAG probes, but does have some limited capability.	<a href="#">UTAG - USB JTAG Probe - Debug Tools Support - Intel Enterprise Wiki</a>

### 25.1.1

### Box Stress Tool

BST is an AIO integrated solution used for Voltage measurements, Voltage drive/margining, GPIO's manipulations, I2C master controller and Thermal Diodes measurements capabilities.

#### NTB FAB B (Nevo to BST Adapter)

BST hooks on to RVP 100pin Nevo connector with use of NTB adapter for ADC, DAC,GPIO's,ISENSE and I2C Controller functions.

For SoC Thermal Diodes measurements and BST onboard VR's auxiliary use case, dedicated cables are available as part of BST Kit.



**Figure 93: Nevo to BST Adapter**

Note: Users who want to use Nevo will need an Adapter card and extension cable. Cable and extension adapter are part of Nevo demand call catalog which open every Quarter, kindly look at info below.

## Nevo Extender Adapter – J34397-100



## Extension cable – H82412-001



**Figure 94: Nevo Extension Cable**

### 25.1.1.1.1 Interface

BST hooks on to RVP 100pin Nevo connector with use of NTB adapter for ADC, DAC, GPIO's and I2C Master functions.

For SoC Thermal Diodes measurements and BST onboard VR's auxiliary use case, dedicated cables will be available as part of BST Kit.

### 25.1.1.1.2 Power Supply

For standard operation of ADC, DAC, GPIO's, I2C Master and Thermal diodes measurements the BST is powered from an USB Type-A to uUSB (5V from Host PC to BST).

For BST auxiliary use case a standard ATX with 12V/5V connector is required.

## 25.2 SINAL to CPU sideband optimization

PECI Circuit in RVP has remained legacy and not changed much over many RVP generation.

Refer [Existing Implementation](#)

Current Status:

- PECL hardware signal is only an internal validation used by thermal teams (INTEC)
- OOB PECL is not POR and inband **PECL over eSPI** is POR from SOC to EC.
- EC & SINAL no longer needed PECL dedicated pin connection. InTEC is the only load on the PECL bus.

Proposal ([Implementation in PTL](#)):

- Retain the 3pin 100mil header & remove the PECL MUX circuit completely.

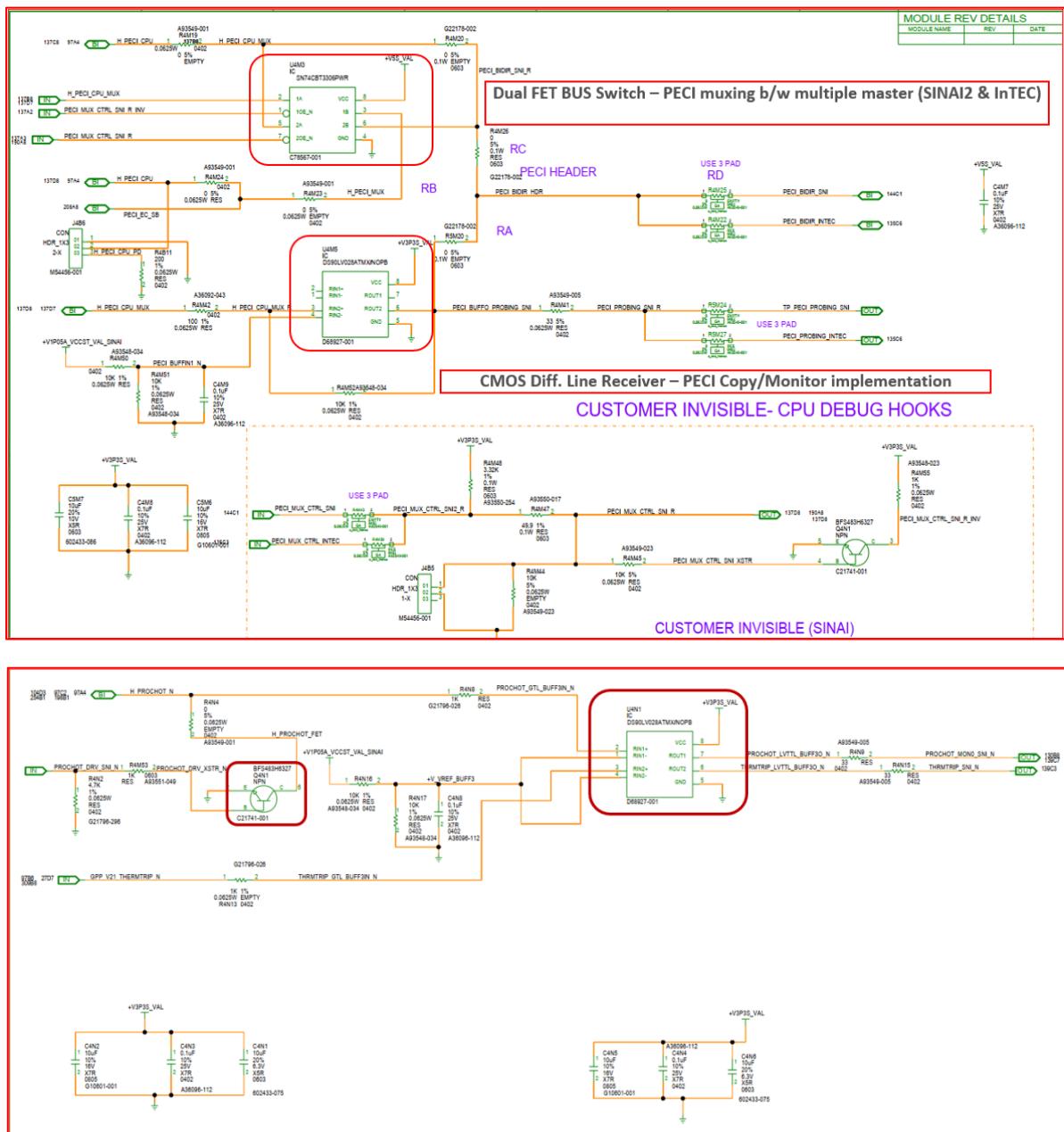
- Default SoC PECL connection should be pull-down, InTEC users must remove the jumper while validating using InTEC tool.
- Unstuff the PECL copy/probing circuit as this is not used currently per INTEC users.
- Retain EC connection to 3 pin header using resistor STUFF option to support any use-case.
- PECL probing circuit is currently UNSTUFF in PTL and it can be removed from next program onwards, if no use-case is identified from any of the users.
- SINAL connector will have 3V3 level of SoC FORCEPR and THERMTRIP signal.

Teams aligned:

- Kravtsov, Alex1; Ziserson, Alexander (iVE); Littrell, Jeremy D (PPV); Dayan, Rami (QnR)

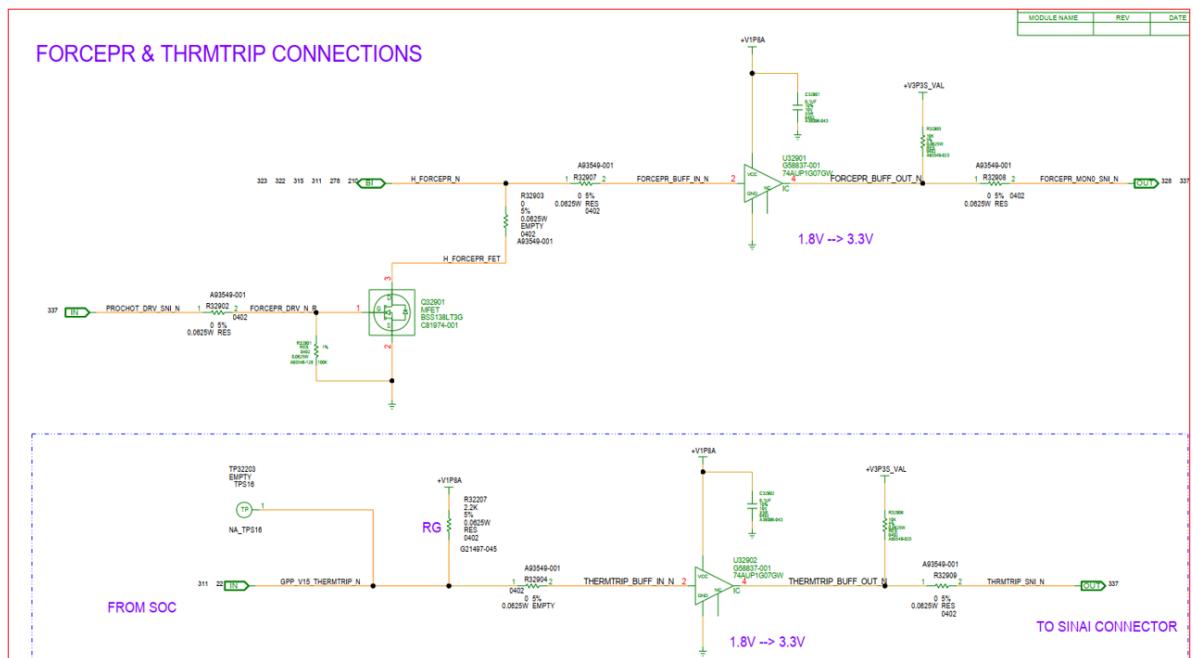
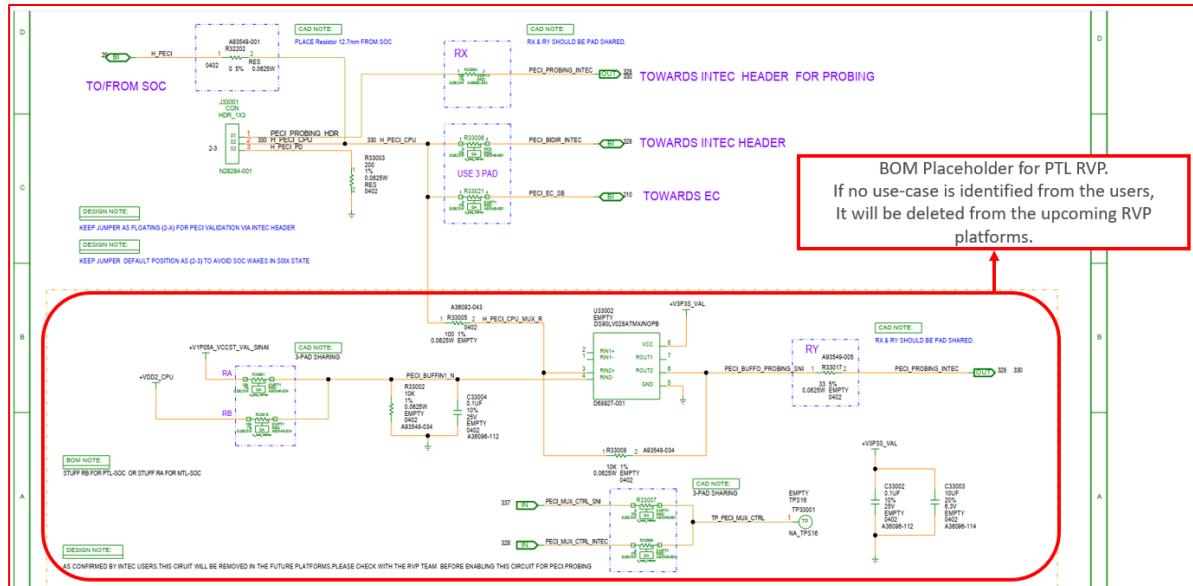
## 25.2.1

## Existing Implementation [SINAI to CPU sideband]



## 25.2.2

## Proposal [SINAI to CPU sideband]



## 26

## Power Delivery & Sequencing

In this section, all the PTL U/H power delivery implementation details (with respect to energy management, rest of the platform power delivery, IMVP9.3, power sequencing, power measurement, voltage margining, power accumulator and PnP requirement) would be covered. High level SoC Power schemes with different DRAM configurations for PTL U/H are shown below. Figure 95 have same pin map between U15, H28 and H45 silicon skus, all the RVP skus designed to support super-set of power requirements among U15W, H28W and H45W so that all three skus can be validated on RVP board.

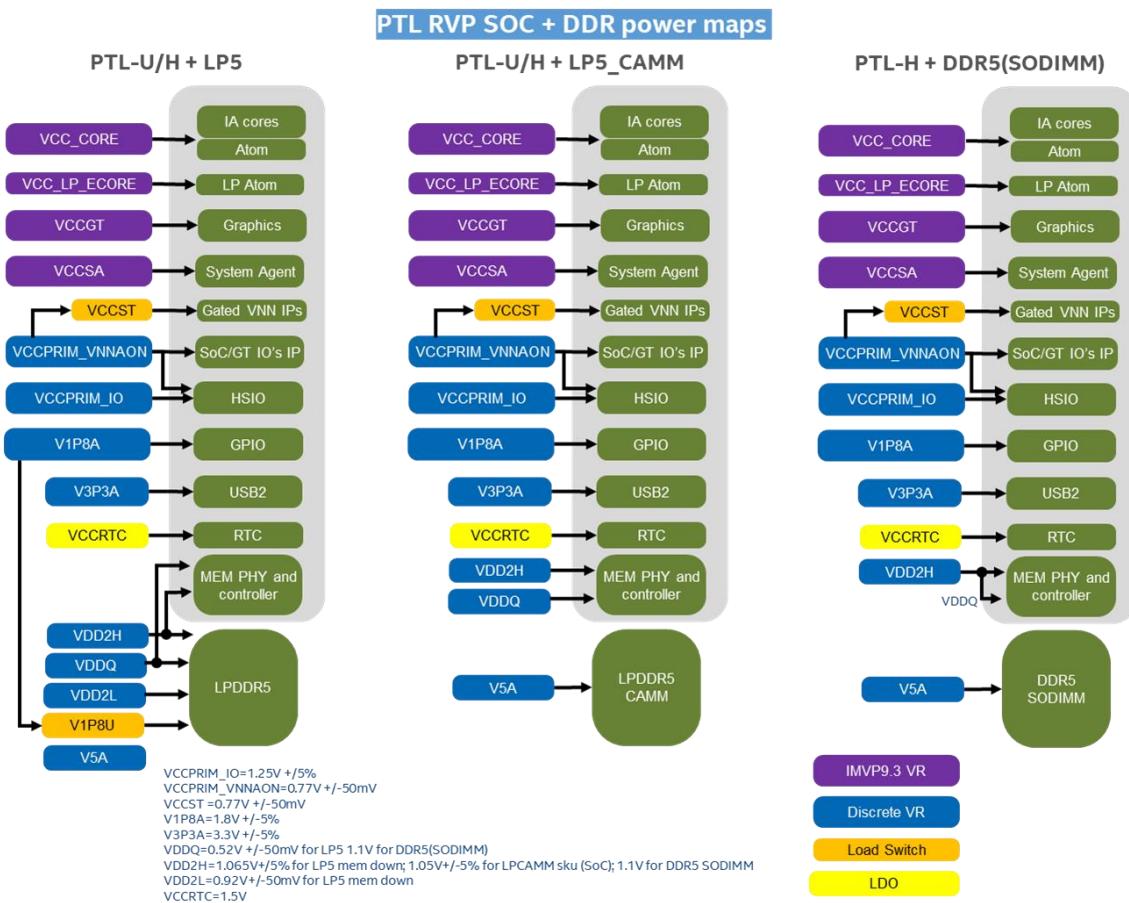


Figure 95: PTL U/H High Level SoC Power Scheme

## 26.1

### Power Sources

PTL U/H can be powered through a standard AC adapter, a Type C power Adapter, or a Battery pack. To support PL4 power number of H28/H45W silicons without battery, use auxiliary AC adapter along with standard AC adapter. PTL U/H can be powered through a standard AC adapter, a Type C power Adapter, or a Battery pack.

#### 26.1.1

##### Standard AC adapter

A 230W adapter is being selected for the PTL U/H RVP and is one of the three power sources which can be used for powering the RVP.

Standard AC adapter alone cannot support PTL H PL4 power number, both battery pack and AC adapter is required to support PTL-H (28W/45W) SKU PL4 performance power number.

Standard AC adapter IPN: J82210-001

Description: AC/DC ADAPTER, 100V-240V Input, 50-60HZ, 19.5V/11.8A Output

#### 26.1.2

##### Type C Adapter

There are four USB-C ports supported on PTL U/H RVP, all ports are USB-C PD 3.1 compatible and can be used for plugging in the Type C adapter. On board type-c ports supports EPR voltages up to 48V and type-c port on TCSS module supports SPR mode Only.

*Note: For dead battery boot with type-c adapter, greater than 3xTDP W adapter is required to boot the PTL-U/H RVP.*

#### 26.1.3

##### Battery Pack

A 3S3P battery pack is being selected for PTL U/H RVP with maximum capacity of 99Whr.

3S3P battery pack **IPN:** K71137-001

**Recommendation:** For all the validation except Performance, the recommendation is to use standard AC adapter. Use Type C adapter or battery pack on need basis.

#### 26.1.4

##### Auxiliary Adapter

Auxiliary adapter is required for supporting PL4 current number along with standard/main AC adapter in PTL H in the absence of battery pack while performing performance related validation. This adapter is same as the standard adapter (IPN: J82210-001). Auxiliary AC adapter powers all four of the CPU rails during its operation i.e., VCCCORE, VCCGT, VCCSA and VCC\_LP\_ECORE.

Platform will not boot with auxiliary adapter alone. When using auxiliary AC adapter, it is recommended to plug main ac adapter first and then auxiliary adapter.

**Table 88: Power Sources & Priority on PTL U/H RVPs**

Available Sources	Priority Given To
<b>Standard AC Brick Adapter + Auxiliary AC Adapter + Battery Pack</b>	<b>Not recommended to use</b>
<b>Standard AC Adapter + Battery Pack</b>	<b>Standard AC Adapter</b>
<b>Type C Adapter + Battery Pack</b>	<b>Type C Adapter</b>
<b>Standard AC Adapter + Type C Adapter</b>	<b>Standard AC Adapter</b>
<b>Standard AC Adapter + Type C Adapter + Battery Pack</b>	<b>Standard AC Adapter</b>
<b>SPR Type-C Adapter + EPR Type-C Adapter + Battery Pack</b>	<b>EPR Type-C Adapter</b>
<b>EPR1 Type-C Adapter + EPR2 Type-C Adapter</b>	<b>Whichever is having higher power output</b>

**Note:** Smooth/seamless transition from Type-C adapter to AC adapter and vice versa is not supported if battery is not connected.

**Note:** When dual Adapters are used, All the IMVP Soc rails are powered with this Auxiliary adapter and ROP rails are powered with the Standard adapter. PSYS measurement is available only for the main power path i.e. Single Adapter + Battery. However, with Dual adapter configuration, the power consumed by the IMVP rails are not included in PSYS measurements and needs to be measured separately at +VBATA\_IMVP power net.

## 26.2 Key Power Delivery Subsystems

The platform power delivery has three key sub-systems which are Energy management, Rest of the platform (RoP) power delivery and CPU power Delivery (including IMVP9.3).

### 26.2.1 Energy Management Sub-System

Battery charger and USB power delivery comes under the energy management sub-system. A buck-Boost NVDC charger is used to charge the battery pack and to power the system with the input voltages from standard AC adapter and Type-C adapters. Battery charger PROCHOT# signal is connected to the SOC PROCHOT signal.

### 26.2.2 Rest of the Platform Power Delivery

Discrete voltage regulators are required for powering the CPU (non SVID), PCH and platform components, power sequencing and load switches form the RoP power delivery sub-system. The RoP power delivery circuitry is down on the mother board.

## 26.2.3

**IMVP9.3 Sub-system**

PTL U/H CPU requires four different SVID rails (VCC\_CORE, VCCGT, VCCSA and VCC\_LP\_ECORE). VCC\_LP\_ECORE is new VR compared to MTL-U/P/H. An IMVP9.3 compliant controller is used for generating these rails.

**Note:** The power delivery sub-systems are on the motherboard.

Required phase count for difference processor line (U15 W/H 28W/H 45W) is show in Table 89.

PTL U/H RVPs will be design for super set configuration (H 45W) to support U15/H28/H45 silicons.

For needed teams, configuring platform like customer config with 1x heatsink, Phase configuration adjustment across silicon's is through switch settings and IMVP programming.

For tuning load line other than POR targets, reworks on board or IMVP FW change, or both may be required.

**Table 89: Processor Line Vs. Phase Count**

Processor Line	Phase Count Required (VCCCORE+VCCGT+VCCSA+VCCLP CORE)
Processor Base Power – U 15W	Baseline and Performance PD: 2+1+1+1
Processor Base Power – H 28W	Baseline PD: 2+1+1+1 Performance PD: 3+2+1+1
Processor Base Power – H 45W	Baseline PD: 3+1+1+1 Performance PD: 4+1+1+1
RVP platform PD U/P/H 45W	Performance PD: 4+2+1+1

Iccmax, TDC and load line targets for different processor line is shown in Table 90

**Table 90: Processor Line Power Specifications**

	U 15W (4P+0E+4e)			H 28W (4P+8E+4e)			H45W (4P+8E+4e)		
Rail Name	Icc_max / Iccmax.app	I_PL2/I_TDC	LL mΩ	Icc_max / Iccmax.app	I_PL2/I_TDC	LL mΩ	Icc_max / Iccmax.app	I_PL2/I_TDC	LL mΩ
VCC_CORE	80A/60A	39A	3.3	140A/105A	51A	3.3	140A/105A	67A	3.3
VCCGT	52A/31A	22A	0	80A/61A	32A	0	52A/31A	22A	0

VCC_LP_ECORE	35A/21A	11A	5.8	35A/24A	12A	5.8	35A/24A	13A	5.8
VCCSA	40A/35A	26A	5.5	40A/35A	26A	5.5	40A/35A	26A	5.5

## 26.3

### Critical Rails and Default Voltage Levels

The below table for all the critical rails and the default regulated voltages.

**Table 91: Critical Voltage Rails with default regulated voltage**

Voltage Regulator	Default Voltage	Comments
+VCC_CORE	0V (Boot Voltage) 0.52-1.52V	CPU adjusts the output voltage through SVID.
+VCCGT	0V (Boot Voltage) 0.52V-1.52V	CPU adjusts the output voltage through SVID.
+VCCSA	0V (Boot Voltage) 0.52V-1.52V	CPU adjusts the output voltage through SVID.
+VCC_LP_ECORE	0V (Boot Voltage) 0.52V-1.52V	CPU adjusts the output voltage through SVID.
+VNNAON	0.77V	
+VCCST	0.77V	MB PG From VNNAON
+VDD2H	1.065V (LP5 Mem Down) 1.065V(LP5 CAMM) 1.1V (DDR5)	Shared rail (LP5x memory + CPU) in LP5x SKU SoC only in LP5x CAMM SKU SoC Only (DDR5)
+VDDQ	0.52V(LP5 Mem Down) 0.53V (LP5 CAMM) 1.1V Tied with +VDD2H	Shared rail (LP5x memory + CPU) in LP5x SKU SoC only in LP5x CAMM SKU SoC Only (DDR5)
+VDD2L	0.92V	Applicable for only LP5x memory (For DVFS support)
+VDD1	1.8V (LP5 Mem Down)	LP5x Only
+VCCIO	1.25V	
+V3.3A	3.3V	
+V5A	5.15V	
+V1.8A	1.8V	
DDR5 rail	5.15V	DRAM module only

**Table 92: Typical Voltage rail for different Memory technologies**

Memory Type	Supporting voltages on memory modules by RVP PD			
	VDD2H	VDD2L	VDD1	VDDQ
LPDDR5x	1.065V → SoC + LP5	0.92V	1.8 V	0.52 V
DDR5	1.1V → SoC 5V → DRAM Module	NA	NA	NA
LP5x CAMM*	1.065V → SoC 5V → CAMM Module	NA*	NA	0.53V

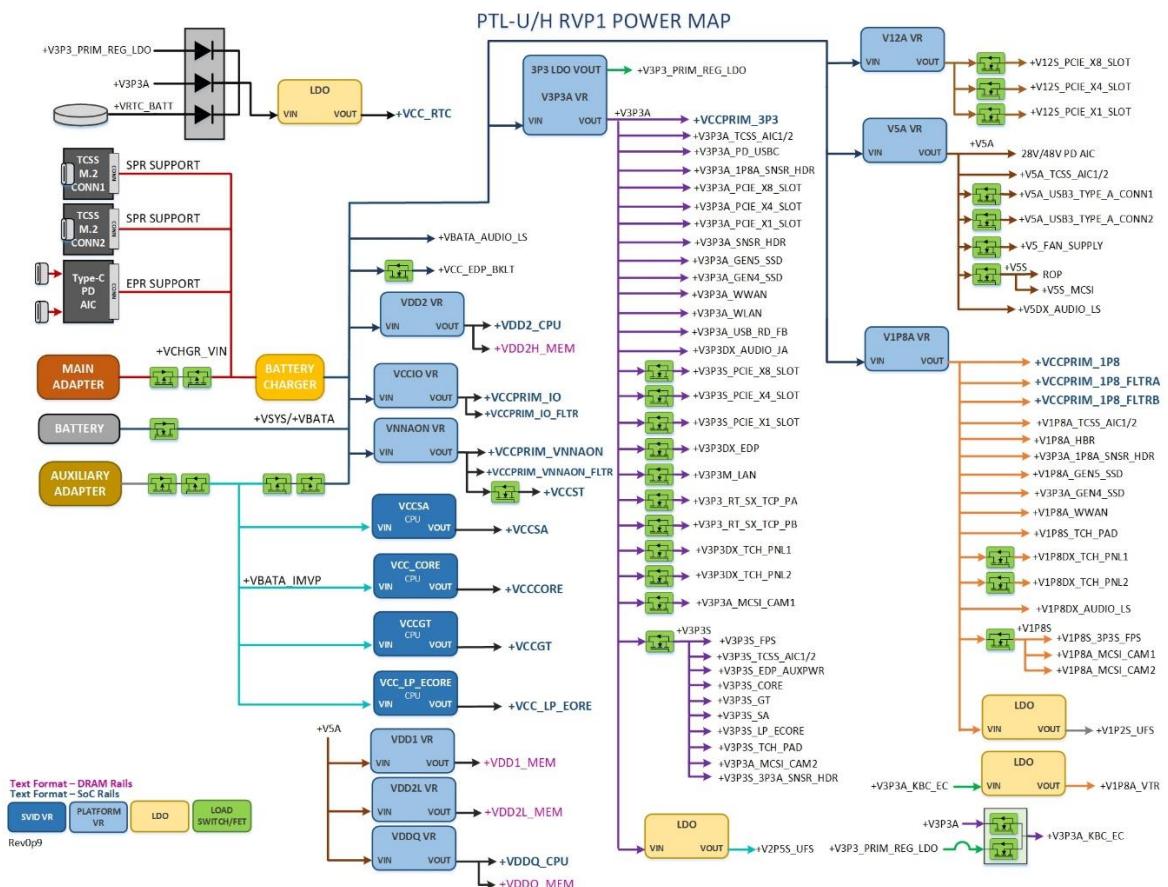
## Note:

\*LP5x CAMM module supports only VDD2H. i.e., VDD2L is merged with VDD2H on the CAMM module

26.4

## Power Map for PTL U/H

Updated PTL-U/H Power map would be placed in [LINK](#)



**Figure 96: PTL U/H RVP1 Power Delivery Block diagram**

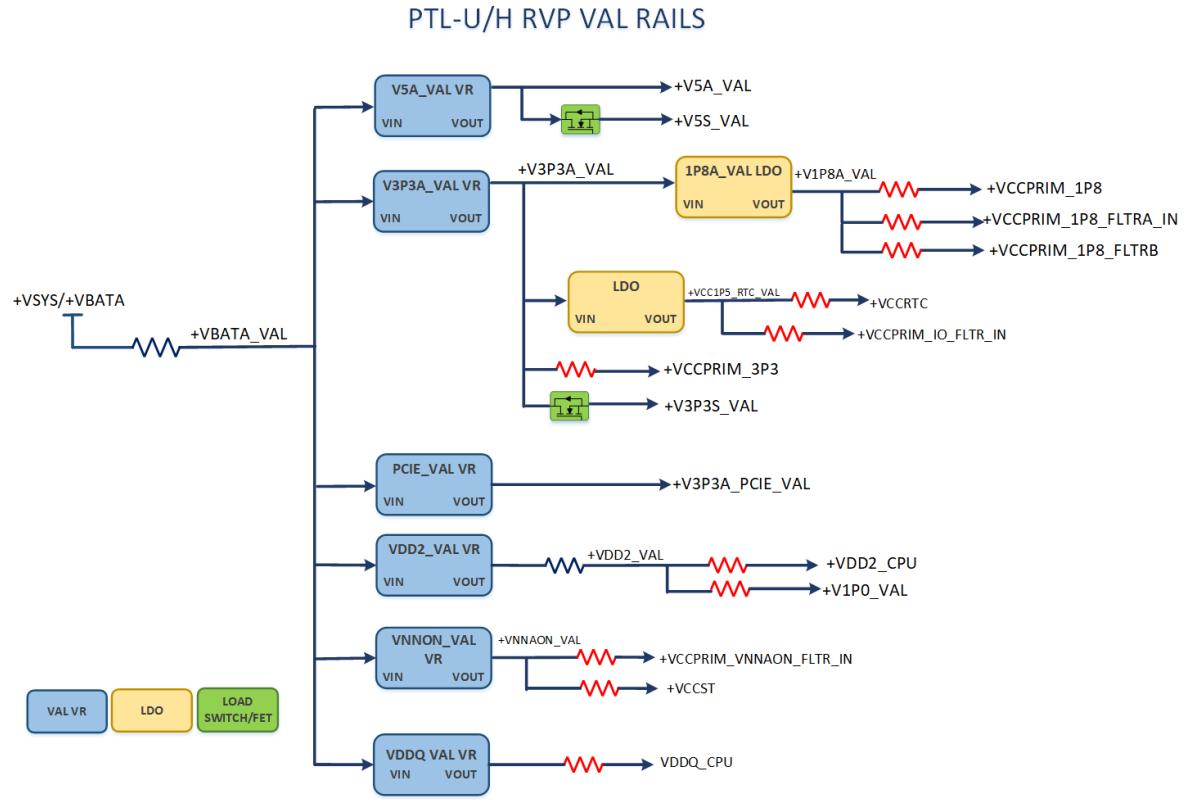


Figure 73: PTL U/H VAL Rails Power Block Diagram

## 26.5

### Power Sequencing

- PTL U/H requires Four IMVP9.3 rails
- IMVP9.3 voltage regulators are enabled by ALL\_SYS\_PWRGD signal which indicates all the platform rails are stable.
- VCC\_CORE, VCCGT, VCCSA and VCC\_LP\_ECORE IMVP9.3 VRs have Zero boot voltage requirement.
- SVID communication is required to change the voltage of IMVP9.3 VRs.
- PTL U/H platform supports Pseudo G3 state.

PTL U/H RVP Power sequencing diagram is available at [LINK](#)

# 27 Power n Performance

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## 27.1 PRD from PnP for power measurements

RVP team will follow all the requirements which are mentioned in PTL U/H Power and Performance requirements document ([Link](#)) . RVP also follows PnP PMR [BKM](#) to select the resistors MPNs.

## 27.2 Voltage margining

For the power and performance validation, margining is supported through Sinai Nevo connector and range of voltages supported are tabulated below. For SoC/PCH a separate +V3P3A \_VAL is provided to support extensive range of margining than +V3P3A VR.

**Table 93: Voltage Margining support on PTL U/H RVP**

VR	VR controller	Nominal Voltage	Voltage range support by VR	Iccmax	Margining Support
+V3P3A	TPS51285A	3.3	2.97V to 3.63V	~25A	Yes
+V1P8A	RT6220A	1.8V	0.6V to 5.0V	7A	Yes
+VNNAON	TPS51219	0.77V	0.5V to 2V	28A	Yes
+VCCIO	TPS51396	1.25V	0.6V to 7V	5A	Yes
+VDD1	RT5795A	1.8V	0.76V to 5.5V	1A	Yes
+VDD2H (DDR5 / LP5x/ CAMM)	RT8231A	1.1V/ 1.05V	0.675 to 3.3V	13A	Yes
+VDD2L	RT5795A	0.92V	0.45V to 3.3V	1.4A	Yes
VDDQ(LP5x)	RT5795A	0.52V	0.45V to 3.3V	2A	Yes
+VCC1P5_RTC	RT9078N-08GJ5	1.5V	0.8V to 3.3V	1A	Yes

## 27.3 Additional Current support (for stress tests)

The IMVP VCC\_CORE, VCCGT, VCCSA and VCC\_LP\_ECORE VRs support additional +20% currents to POR PL2 currents to support stress tests on SoC.

The teams doing stress tests (that draw higher currents than POR) are expected to have external cooling (may be an external cooling fan) for VRs. Thermal solution on board does not support cooling requirements during stress tests for higher currents.

## 27.4

### PnP PMR resistor

2x7 headers are provided on board which brings out voltage and current sense points from the board that can be used for Power and Performance measurement of different power rails for both PCH and CPU and different on-board interfaces. Few of 2x7 connection pairs are left spare, provision to wire for additional measurements on board.

SoC/PCH and CPU current sense lines from Power Measurement Resistor (PMR) are connected to dedicate 2x7 headers. 2x7 HDRs mapping to PMR resistors is available in [LINK](#) (as available). CPU and PCH rails assigned/grouped to 2x7 HDRs to optimize the cable connections to NI DAQ.

Special attention from PnP (CPU, SoC/ PCH & ROP PnP) team is required on type of the PMRs used in PTL U/H RVP. Previous programs use the PMRs only from Vishay, PTL-U/H program follows different approach to enable PMRs from the multiple vendors includes Vishay. Approach in PTL U/H is to select the PMRs from the different vendors with the criteria provided in the BKM below:

[PMR BKM Link](#)

#### 27.4.1

### PnP PMR/Current Sense Resistors Stuffing

As part of cost optimization on PTL RVPs, PMRs/Current Sense Resistors are stuffed and fully supported only on PnP/Chrome SKUs. In Non-PnP SKUs, Current Sense Resistors are partially supported. In Non-PnP SKUs, PnP PMRs are provided for those rails which are connected to Power Accumulator Devices only. The rest of sense resistors will be replaced with shorting resistors/copper shunt resistors. The details of each sense resistor which will be converted to the shorting resistor in non PnP SKUs is captured in xls available at [LINK](#).

## 27.5

### Power Accumulator

Seven power Accumulators (PAC1954T) provided for measure power in following rails. Each power accumulator has 4 channels, Per Channel 48-Bit Power Accumulators Capture 17 Minutes of Data at 1024sps. Also has per Channel 12-Bit Voltage Registers. The data can be read through PCH SM bus.

System meter mapping for PTL U/H RVPs is captured in following section.

### Energy Telemetry Support

Energy telemetry mapping is supported on RVP1 UH-01 and UH-02 Skus. UH-03 and UH-04 follows the PnP mapping/System meter mapping as shown in below table. The details of mapping of different SKUs are also available at power meter wiki [LINK](#).

Table 94: PTL U/H RVP1

Applicable SKUs in RVP1 →					ERB1: PTL-UH LP5x T3 Mem Skt ERB2: PTL-UH LP5x T3 Mem Skt Chrome UH03: PTL-UH LP5x T3 MemSkt PnP UH04: PTL-UH LP5x T3 MemSD Chrome	UH01: PTL-UH LP5x T3 Mem Skt UH02: PTL-UH LP5x T3 MemSD
I2C Host→					SoC(I2C3)	SoC(I2C3)
Power Meter	CH	SMBus Address	7 Bit Address	ADDRSEL_RES(Ω)	PnP Config. Rails PnP Boards	Energy Telemetry Config. Rails Non PnP Boards
1	1	0011 000 (R/W)	0x18	13300	+VCCCORE(Phase1)	+VBATA_VCCCCORE_IN
	2				+VCCCORE(Phase2)	+V12S_PCIE_X8_SLOT
	3				+VCCCORE(Phase3)	+V3P3S_PCIE_X8_SLOT
	4				+VCCCORE(Phase4)	+V5A_TCSS_AIC1
2	1	0011 110 (R/W)	0x1E	226000	+VCCGT(Phase1)	+VBATA_VCCGT_IN
	2				+VCCGT(Phase2)	+V5A_TCSS_AIC2
	3				+VCCSA	+VBATA_VCCSA_IN
	4				+VCC_LP_EORE	+VBATA_VCC_LP_ECORE_IN
3	1	0010 001 (R/W)	0x11	499	+VCCPRIM_VNNAON	+VCCPRIM_VNNAON
	2				+VCCPRIM_IO	+VCCPRIM_IO
	3				+VCCPRIM_3P3	TYPE_C_TCP0_5V
	4				+VCCPRIM_1P8	+VCCPRIM_1P8
4	1	0010 101 (R/W)	0x15	3240	+VCCRTC	+V3P3A_GEN5_SSD
	2				+VCCST	TYPE_C_TCP1_5V
	3				+VDD2_CPU	+VDD2_CPU
	4				+VDDQ_CPU	+VDDQ_CPU
5	1	0011 001 (R/W)	0x19	21500	+VDD2H_MEM	+VBATA_VDD2H_VR_IN
	2				+VDD2L_MEM	+V5A_MEM
	3				+VDDQ_MEM	+V2P5S_UFS
	4				+VDD1_MEM	+V1P2S_UFS
6	1	0010 100 (R/W)	0x14	2050	+VCC_EDP_BKLT	+VCC_EDP_BKLT
	2				+V3P3DX_EDP	+V3P3DX_EDP
	3				+V3P3A_WLAN (Default)	+V3P3A_WLAN
	4				+V3P3A_WWAN (Rework)	+V3P3A_GEN4_SSD
7	1	0010 111 (R/W)	0x17	8450	+V3P3A_GEN4_SSD (Default)	+V3P3A_GEN4_SSD
	2				+V3P3A_GEN5_SSD (Rework)	+V3P3A_IMVP
	3				+V1P8S_MCSI_CAM1(Default)	+VBATA_IMVP
	4				+V1P8S_MCSI_CAM2(Rework)	+VBATA
					+V3P3S_MCSI_CAM1(Default)	+V3P3A_WWAN
					+V3P3S_MCSI_CAM2(Rework)	+V_CHGR_FETIN

Table 95: PTL U/H RVP3

S.No.	Power Meter PAC1954	CH	Rail	Domain	SMBus Address	ADDRSEL_RES(Ω)	I2C Bus Number
1			1 +VCCCCORE (Phase1)	CPU			
2		1	2 +VCCCCORE (Phase2)	CPU			
3			3 +VCCCCORE (Phase3)	CPU			
4			4 +VCCCCORE (Phase4)	CPU			
5			1 +VCC_GT (Phase1)	CPU			
6		2	2 +VCC_GT (Phase2)	CPU			
7			3 +VCC_SA	CPU			
8			4 +VCC_LP_ECORE	CPU			
9			1 +VNNAON	CPU			
10		3	2 +VCCIO	CPU			
11			3 +VCC_3P3	CPU			
12			4 +VCC1P8	CPU			
13			+VCC1P5_RTC	CPU			
14		4	+VCCST	CPU			
15			+VDD2H_CPU	CPU			
16			+VDDQ_CPU	CPU			
17			1 +VDD2H_MEM	DRAM			
18		5	2 +VDD2L_MEM	DRAM			
19			3 +VDDQ_MEM	DRAM			
20			4 +VDD1_MEM	DRAM			
21			1 +VCC_EDP_BKLTX1	Display			
22			2 +V3P3DX_EDPX1	Display			
23		6	+V3P3A_WWWAN (Default) 3 +V3P3A_WLAN (Rework Option)	Connectivity			
24			+V3P3DX_M2_SSD1 (Default) 4 +V3P3DX_M2_SSD2 (Rework Option)	Storage			
25			1 +VBATA_CORE	System VBATA			
26			2 +VBATA	System VBATA			
27		7	+V1P8S_MCSI_CAM1 (Default) 3 +V1P8S_MCSI_CAM2 (Rework Option)	Camera			
28			+V3P3S_MCSI_CAM1 (Default) 4 +V3P3S_MCSI_CAM2 (Rework Option)	Camera			
S.No.	Power Meter PAC1952	CH	CPU SENSE	Domain	SMBus Address	ADDRSEL_RES(Ω)	
1		1	1 SENSE_VCC_CORE	VCCCCORE PKG SENSE			
2			2 SENSE_VCCGT	VCCGT PKG SENSE			
3		2	1 SENSE_VCCSA	VCCSA PKG SENSE			
4			2 SENSE_VCC_LP_ECORE	VCC_LP_ECORE PKG SENSE			

**Table 96: PTL U/H RVP2/RVP4**

S.No.	Power Meter PAC1954	CH	Rail	Rails to be referred by BIOS	Domain	SMBus Address	ADDRSEL_RES(Ω)	I2C Bus Number
1	1	1	1 +VCCCORE (Phase1)	CPU_VCCCORE1	CPU	TBD	TBD	TBD
2			2 +VCCCORE (Phase2)	CPU_VCCCORE2	CPU			
3			3 +VCCCORE (Phase3)	CPU_VCCCORE3	CPU			
4			4 /CCCORE (Phase4)	CPU_VCCCORE4	CPU			
5	2	2	1 +VCC_GT (Phase1)	CPU_VCCGT1	CPU	TBD	TBD	TBD
6			2 +VCC_GT (Phase2)	CPU_VCCGT2	CPU			
7			3 +VCC_SA	CPU_VCCSA	CPU			
8			4 +VCC_LP_ECORE	CPU_VCCSA	CPU			
9	3	3	1 +VNNAON	CPU_VNNAON	CPU	TBD	TBD	TBD
10			2 +VCCIO	CPU_VCCIO	GPU			
11			3 +VCC_3P3	CPU_VCC_3P3	CPU			
12			4 /CC1P8	CPU_VCC1P8	CPU			
13	4	4	+VCC1P5_RTC	CPU_VCC1P5_RT	CPU	TBD	TBD	TBD
14			+VCCST	CPU_VCCST	GPU			
15			+VDD2H_CPU	CPU_VDD2H	GPU			
16			+V5A_DRAM	DRAM_BULK_VIN	DRAM			
17	5	5	1 +V2P5S_UFS	STORAGE_UFS_V2P5	STORAGE	TBD	TBD	TBD
18			2 +V1P2S_UFS	STORAGE_UFS_V1P2	STORAGE			
19			3 +V3P3S_PCIE_X8_SLOT	PCIE_X8_SLOT_V3P3	PCIE_X8_SLOT			
20			4 /125_PCIE_X8_SLOT	PCIE_X8_SLOT_V12	PCIE_X8_SLOT			
21	6	6	1 +VCC_EDP_BKLTX1	DISPLAY_BKLT	Display	TBD	TBD	TBD
22			2 +V3P3DX_EDPX1	DISPLAY_V3P3	Display			
23			+V3P3A_WWAN (Default) +V3P3A_WLAN (Rework 3 Option)	CONNECTIVITY_WWAN	Connectivity			
24			+V3P3DX_M2_SSD1 (Default) +V3P3DX_M2_SSD2 (Rework 4 Option)	STORAGE_PCH_SSD1	Storage			
25	7	7	1 +VBATA_CORE	SYSTEM_VBATA1	System VBATA	TBD	TBD	TBD
26			2 +VBATA	SYSTEM_VBATA2	System VBATA			
27			+V1P8S_MCSI_CAM1 (Default) +V1P8S_MCSI_CAM2 (Rework 3 Option)	CAMERA_V1P8S1	Camera			
28			+V3P3S_MCSI_CAM1 (Default) +V3P3S_MCSI_CAM2 (Rework 4 Option)	CAMERA_V3P3S1	Camera			
S.No.	Power Meter PAC1952	CH	CPU SENSE	Rails to be referred by BIOS	Domain	SMBus Address	ADDRSEL_RES(Ω)	
1	1	1	1 SENSE_VCC_CORE	CPU_VCCCORE1	VCCCORE PKG SENSE	TBD	TBD	TBD
2			2 SENSE_VCCGT	CPU_VCCCORE2	VCCGT PKG SENSE			
3	2	2	1 SENSE_VCCSA	CPU_VCCCORE1	VCCSA PKG SENSE	TBD	TBD	TBD
4			2 SENSE_VCC_LP_ECORE	CPU_VCCCORE2	VCC_LP_ECORE PKG SENSE			

## 28 PPV (Processor/Product Platform Validation)

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PTL-U/H RVP is used in PPV environment for silicon screening.

### 28.1 PPV support on PTL-U/H RVP

PTL-U/H shall support the necessary mechanical and PPV specific socket KOZs required for PPV environment without deviating from POR platform requirements. IO Assignment is covered in the respective IO section. That should be referred to know the exact mapping.

**PPV SKUs key board level interface requirements:**

1. Side band header – for key control signals
  - a. Pins 35/37/39 go to the FRU ROM after the "isolation" jumpers, so we can remove jumpers and FRU connects ONLY to STHI, not to MB SMBUS
  - b. +VRTEC\_BATT is exactly that' the RTC Coin Cell battery.
  - c. There are 4 EDM pins, connect to DUT as appropriate: for U Package for example, 2 to CPU, 1 to EDRAM, with stuffing option for second PCH if applicable, and one to primary PCH.
  - d. Pins 4/6 are the SMBUS connected to the Port80 PLD
2. InTEC header – for thermal connection
3. SINAI2 header – for analog voltage and current sense and a couple DIOs
4. SPI TPM header – For BIOS emulator / programming with stuffing option to allow disconnecting SPI down to have emulator ONLY
5. Debug log capability using either DB9 connector or via uUSB
6. PPV socket specific PDBOM implementation.
7. Header for I2C CLK/DATA connecting to on board FRU EEPROM.
8. PCIe x1 slot – One PCI-E x1 slot on the board to cable PCI-E to host system to connect other PCIe devices down-stream from a bridge.
9. PPV BOM ID should be 101 as per BKM.

**PPV SKUs custom BRD requirements:**

1. CPU pad must have Solder Resist Opening (SRO) 25um radius / 50um diameter larger than the pad, example 250um pad would need 300um SRO. This is to optimize socket alignment.
2. No silk-screen under socket zero height KOZ area, to avoid silk screen lifting socket slightly off board, impacting socket reliability.
3. NiPdAu plating (aka ENEPiG) with Nickel, Palladium, and Gold on surface for the PPV specific builds PCB to make more durable for use in factory.
4. Must review DFx (DFM/DFT) with SIMS team to enable smooth transfer of PPV builds to SIMS to support future builds past PRQ.
5. Mechanical & Socket KOZ / KIZ

## 29 Front Panel Header

PTL-U/H RVP supports the standard front panel 2x8, 16 pin headers. The main purpose of this header is to have some basic control and status indication on the front panel of chassis. The pin out of the front panel header is given below,

Table 97: Front Panel Header Pinout

Signal Name	Pin #	Pin #	Signal
+V5S_VAL	1	2	+V5S_VAL
Hard Disk LED	3	4	GND
GND	5	6	Power Button
Front Panel Rest	7	8	GND
+V5A_VAL	9	10	Key
NC	11	12	GND
GND	13	14	Key
BC_ACOK_DSW	15	16	+V5A_VAL

# 30 Mechanical

## 30.1 Form Factor

The PTL-UH RVP will follow MTL RVP Form Factor → Board size: **11" x 9"**, Board Mounting Holes will follow mostly the micro-ATX requirements (picture below) → A, B, C, F, G, H, J, are included by default, availability of R & S Holes are dependent on Layout. If R & S Holes can't be accommodated, we will provide additional mounting holes wherever necessary based on structural requirement

Each of the holes will follow the standard ATX Mounting Hole spec. (Diameter-156mils) & KoZ.

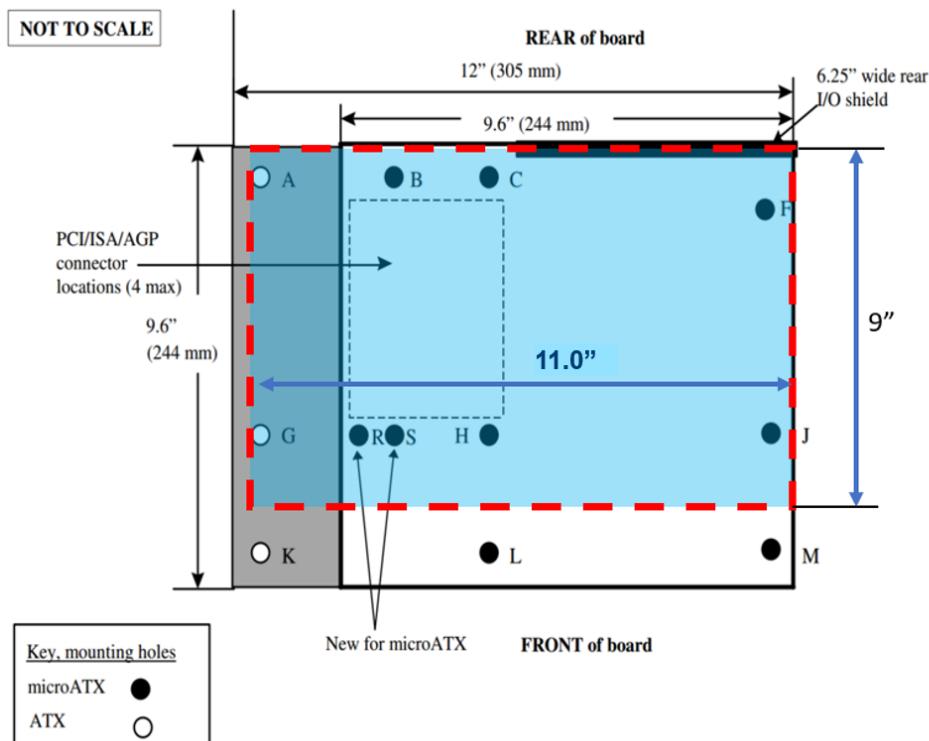


Figure 97: PTL-UH RVP Form factor details

# 31 Chrome Requirements

Chrome architecture varies a little from Windows architecture and Chrome teams need a mechanism to validate delta hardware requirements on the PTL-U/H RVP. Delta subsystems include,

- Chrome EC
- Audio
- Chrome security chip (H1)
- Chrome debug header SERVO
- TCPC AIC

## 31.1 Chrome support on PTL-U/H RVP

PTL RVP supports chrome requirements using Microchip EC on-board. EC to support many other features – WOV, TCPM, Integrated Sensor hub for sensor attach, integrated TCPC ports (in few cases). These features are different from Windows EC.

RVP includes the Chrome EC part MEC1727N-B0-I/SZ-CHRO on-board with some BoM changes for Chrome requirement. No support for Chrome EC AIC on the MECC connector in PTL-U/H RVP.

H1 security IC and Servo debug header will be supported using a new H1-Servo AIC. Dauntless (H1D3) GSC (Google Security chip) AIC to be supported on Chrome SKU using H1 AIC and TTK3 header. H1 AIC supports SMBUS based controller to support chrome keyboard validation.

A dedicated Chrome BOM SKU will be supported in **LP5 (RVP1), DDR5(RVP4)** SKUs of PTL-U/H RVP to enable these features by default. Configuration support model planned for Chrome on PTL RVP as follow:

- Config: onboard EC(Microchip) + H1-Servo AIC + PTL M.2 TCSS module on two TCP ports and MTL TCPC AIC on two TCP ports

**Note:** Chrome requirements have slight changes and are yet to be confirmed. This section might have some modifications once confirmed from Chrome team.

High level block diagram for Chrome from RVP side is shown below.

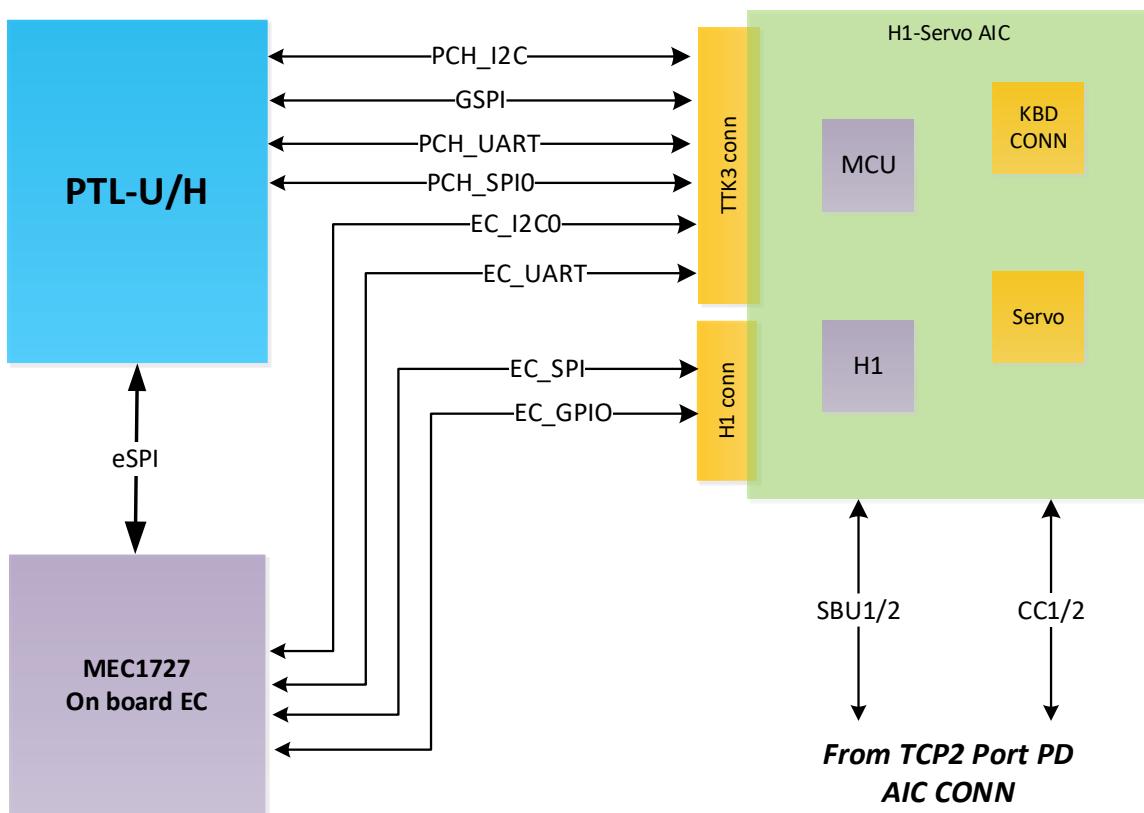


Figure 98 : Chrome support High Level block diagram with on-board Chrome EC

### 31.2

## H1-Servo AIC

H1-Servo AIC is designed based on dauntless GSC security chip. This AIC includes,

- Chrome security chip: It communicates with EC & AP over SPI and does following features.
  - Reset functions.
  - Closed case debugging.
  - Verified boot.
  - Security features
  - Battery cutoff
- Servo header:
  - Access UARTs of EC, CPU, ISH, TPM, PD
  - Flashing firmware like EC, Coreboot, PD, TPM
  - Access device GPIOs like power button, cold reset, warm reset, volume buttons, keyboard pins, lid,etc
- SMBUS companion IC and keyboard connector to support chrome keyboard validation.

TTK3 & H1 connector pinout details are shared over [Link](#)

Table 60: TTKE &amp; H1 Connector

MFG	Mfg. Part Number	IPN Number
Samtec	ASP-203744-03	K18833-001
Samtec	ASP-159358-09	G25403-004

### 31.3 Chrome USB-C support

PTL Chrome planned to support PTL PD AIC 20V SPR with Realtek PD controller. MTL TCPC AIC on two ports is considered as backup option. For other two ports, plan is to have a CFP TypeC M.2 module. TCSS module details are provided in link <https://goto/tcssmodule>

Chrome USB-C modular AIC includes single port PD controller. USB-C connector and the retimer are available on the module. SBU mux shall be added on this AIC for considering SBU signals for DP/debug alternate modes. This AIC follows the latest 2.05 spec PD AIC pinouts. I2C debug over TCP0 is supported. Two different I2C ports from EC are provided for individual TCP port modules.

Since we are trying to re-use the MTL TCPC AIC, we may need to provide few additional options to meet the latest PD AIC spec (2.05) being followed on RVP. SBU signal mapping to be changed as per new spec on RVP. To support CCD debug, SBU and CC signals connected to H1 AIC connector. An external 2:1 SBU mux shall be provided to select between retimer or H1 SBU path. One I2C interface from EC shall be provided for MTL TCPC AIC.

Below block diagram shows the PTL-U/H USB-C TCPC chrome support.

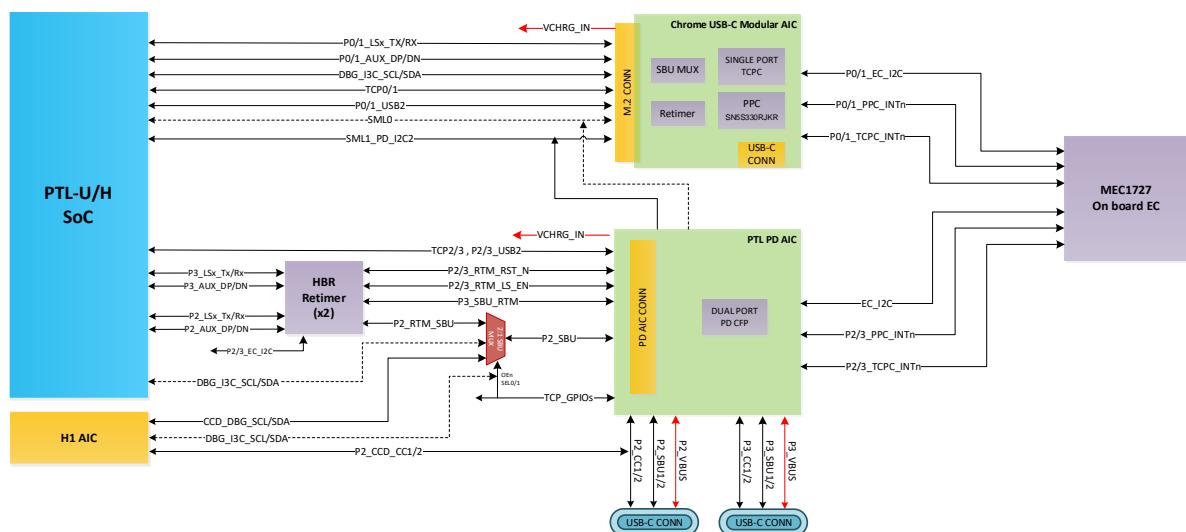


Figure 99 : PTL-U/H Chrome CCD support

## 32 Regulatory & Product Ecology

The following items must be satisfied to meet regulatory and ecology requirements for the PTL-UH RVP.

- An unauthorized device label needs to be attached/tied to the RVP board at the factory. Intel part number K21553-003 (or later) should be used.
- A safety flyer must be shipped with the RVP board. Intel part number J10643-003 should be used and the flyer should be included in the packaging box of RVP board.
- Review batteries (including coin cell) being shipped/used with the RVP for proper shipping and safety compliance. The following certificates should be obtained in cooperation with SSC (MSO): UN38.3/MSDS/1.2m drop, CSTCG (Dangerous good), CB (IEC62133), UL1642, REACH SVHC, and EU battery directive. Please refer to DocLocator document "Battery Selection and Approval Procedure" [DL-0002566](#) (legacy SNAP 227-0029), for details.
- Review power supply being shipped/used with the RVP for safety and energy efficiency compliance in the region it is being shipped. For previous RVPs, power supplies with NRTL certification and US Dept. of Energy Level VI efficiency rating have been used. Please refer to DocLocator document "Mains Connected Power Supply Selection and Approval Procedure" [DL-0002565](#) (legacy SNAP 227-0028), for details.
- Intel Pre-lease Loan Agreement (IPLA) "One Pager" must be shipped with the RVP board. It communicates the important legal information about the DV to customer. Intel part number M21973 should be used and included in the packaging box of RVP board.
- When shipping with a battery, there needs to be a battery warning label on the packaging. Li Metal Battery Warning Label (including coin cell if shipped from China): IPN: J72126-004 and/or Li Ion Battery Warning Label: IPN: J72128-004.
- The RVP BOM needs to be reviewed and undergo a risk assessment by a Product Ecology Engineer and given a ship approval. The results will be documented in the product regulatory plan.
- Ecology labeling needs to be attached to the packaging to show compliance to CA perchlorate requirements. Perchlorate label, (sample IPN: D85237-001), needs to be affixed to the packaging of the board containing coin cell battery shipping to CA. Please refer to DocLocator document [DL-0002372](#) "Environmental Product Content Specification for Suppliers & Outsourced Manufacturers" (legacy SNAP 18-1201), 3.5 for details.
- Review components containing laser emitters for eye safety compliance before usage. shall follow distribution requirements outlined in the Laser Regulatory and Product Safety Requirements [DL-0002555](#) (legacy SNAP 227-0009).
- Review radio (Wi-Fi, WiGig, cellular, BT, NFC, etc.) components for regulatory staging and carrier access compliance in the regions it will be used in.
- Complete radiated emissions (EMI) scans to the limits of the regions it will be shipped to ensure no harmful interference (shall be performed with assistance from the PRE). A schematic and layout review for EMC and RF by PRE is recommended.
- Undergo a Safety Review by a qualified Product Regulations Engineer (PRE) or 3rd party certified safety testing organization and found to be "reasonably safe" as defined in the Intel Corporation "Product Regulations Methodology Specification", [DL-0002650](#) (legacy

SNAP 227-GS0021). The criteria used for the safety review are based on the current version of “Information Technology Equipment - Safety”, IEC 62368 or other relevant product specific safety standard.

DocLocator documents can be found here:

<https://doclocator.intel.com/>

## 33 RVP Health DAC

### 33.1 RVP Health DAC: A novel way to access remote hardware & accelerate debug

The product development life cycle is accelerating at fast pace and platform design complexity continues to increase exponentially. The platforms continue to evolve rapidly, to address aggressive schedules and products time to market goals. A reduced overall silicon development cycle warrants a faster and efficient validation environment. But root-causing platform failures in these circumstances becomes a huge challenge. Accessing and debugging remote deployed systems, becomes a big herculean task. In this challenging ecosystem, it's extremely important to innovate efficient mechanisms for faster debug, to enable high quality validation and bug fixes.

RVP Health DAC (Debug Acceleration card) is a novel approach that facilitates faster remote debug monitoring & root cause of platform issues. It gives a completely new dimension to diagnostics, remote platform access and validation. It's a pluggable kit solution, which reduces main platform design dependency. Thoughtfully designed as a scalable/reusable solution across big & small core products.

### 33.2 RVP DAC (Debug Acceleration Card) Goal is to enable “Remote debug and accessibility” of deployed RVP to validation customers.

RVP Health DAC is based on Intel Altera based MAX10 FPGA (Field programmable gate array) for probing and processing of debug signals. Main goal of DAC (Debug Acceleration card) is to facilitate faster remote debug, monitoring, and root cause of issues. All these features are enabled via user friendly GUI (Graphical user interface).

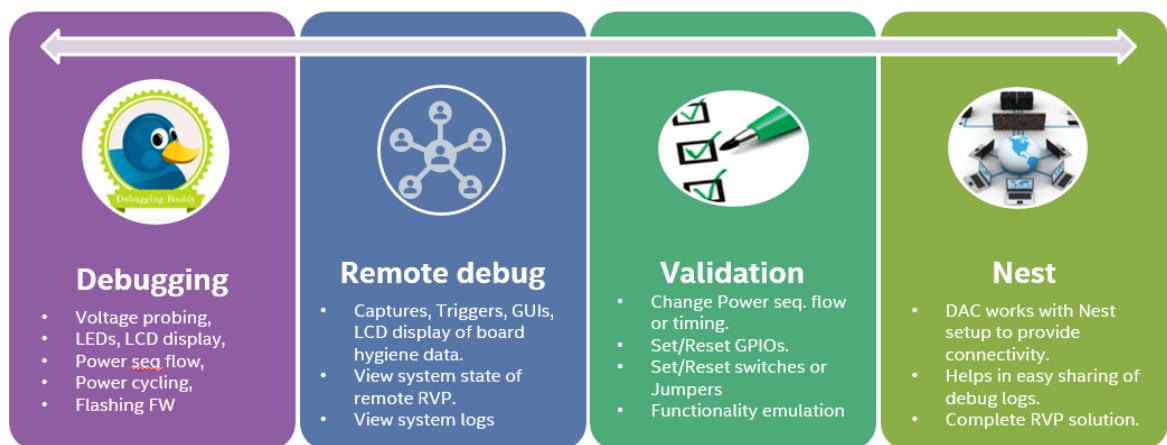


Figure 100 : Strategy for debug acceleration card

### 33.3 The RVP Health DAC solution can be divided into two parts:

#### 33.3.1 Hardware Interface

The DAC (Debug acceleration card) does not need any special header to connect on RVPs.

The overhead is avoided by using existing headers to tap the signals from RVP to provide all the features. This salient unique feature of DAC makes it scalable across all the RVP segments of S, P, M and atom segment N too. There is a single custom designed 100-pin cable on DAC side for ease of connectivity. The HW unit is assembled and shipped in a chassis and a 100-Pin cable, AC-Brick adaptor is included in packaging box. All the soft collaterals and list of key contact are available at <https://goto.intel.com/rvpdac>.

The detailed block diagram of RVP Health DAC is as given below:

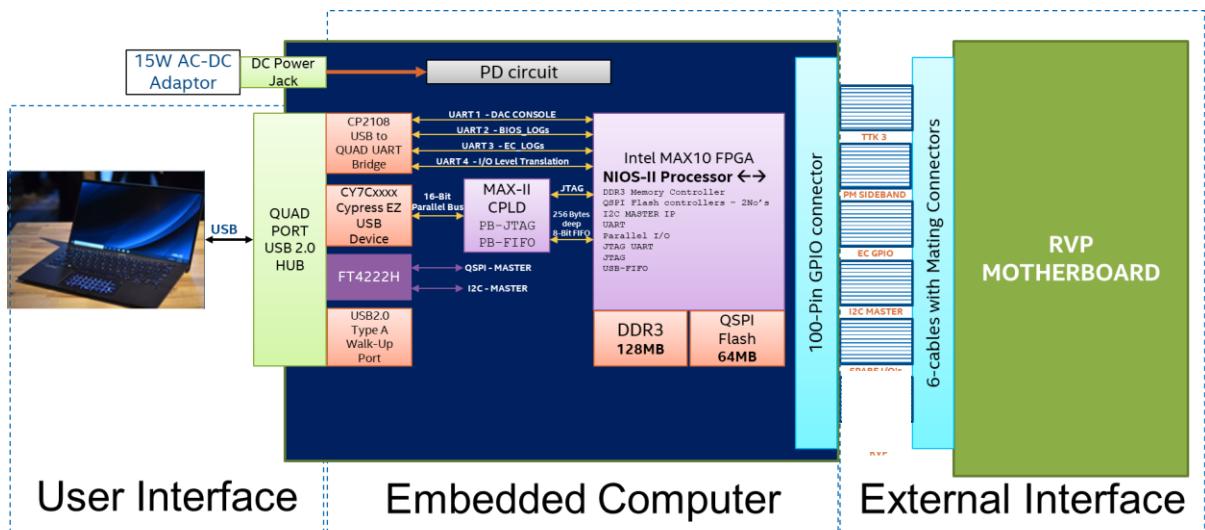


Figure 101 : RVP DAC Block Diagram

The RVP Health DAC snapshot is as given below:

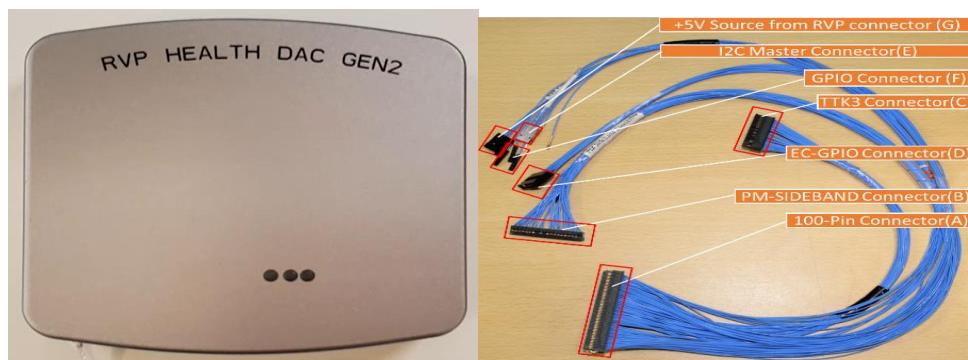
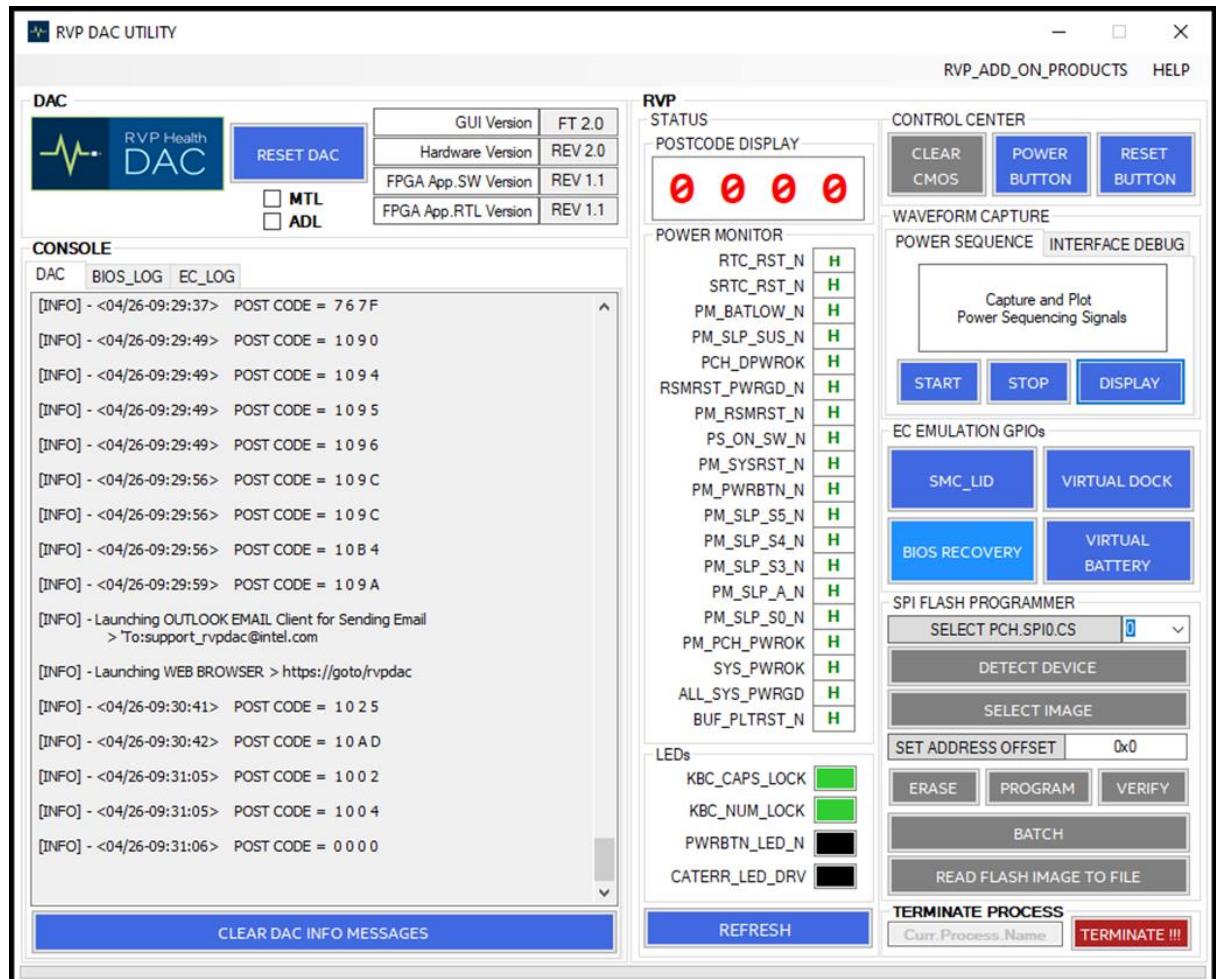


Figure 102 : Snapshot of RVP DAC with Cable

### 33.3.2

### Software interface

For the ease of debug for validation customers, instead of console command-based interface, DAC has been designed with simple, light weight Python based windows GUI application. Below picture of DAC GUI depicts the post code displayed in red, on right side. The console down shows the status of RVP boot and COM port detection. The power monitor shows the status of signals on RVP on successful DAC connection.



**Figure 103 : Debug acceleration graphical user interface and features**

Here are the main features that DAC supports -

- 1) **Communication between HOST and RVP DAC over USB-UART**
- 2) **Reset the RVP DAC from HOST**
- 3) **Configure RVP DAC from HOST**
- 4) **Control RVP power-button & reset-button.**
- 5) **Interface RVP DAC to Target motherboard**
  - 1) **Clear CMOS operation**
  - 2) **Sniff and Display**

- POST Codes over PORT 80
- Num-Lock LED
- Caps-Lock LED
- CAT\_ERR\_LED
- PWR\_BTN\_LED

**3) Control EC Emulating GPIOs**

- Lid Close/Open
- Battery Charger Connect/Disconnect
- Dock Connect/Disconnect
- Set BIOS Recovery Mode ON/OFF

**4) Read and Plot**

- Power Monitoring signals
- Interface debug signals

**5) SPI FLASH Programming****6) Read or Program PSS data <WIP>****7) Capture and save debug Logs over**

- BIOS UART
- EC UART

**For more info on RVP Health DAC, please refer below links:**

Link to Intro video	: <a href="#">DAC_Introduction.mp4</a>
Link to User Guide	: <a href="#">RVP_DAC_UG_Gen2_REV1p0.docx</a>
Link to I/O connector details	: <a href="#">M37690-001.xlsx</a>

## 34.1

### Low cost, Multi-Protocol and Remote programming solution

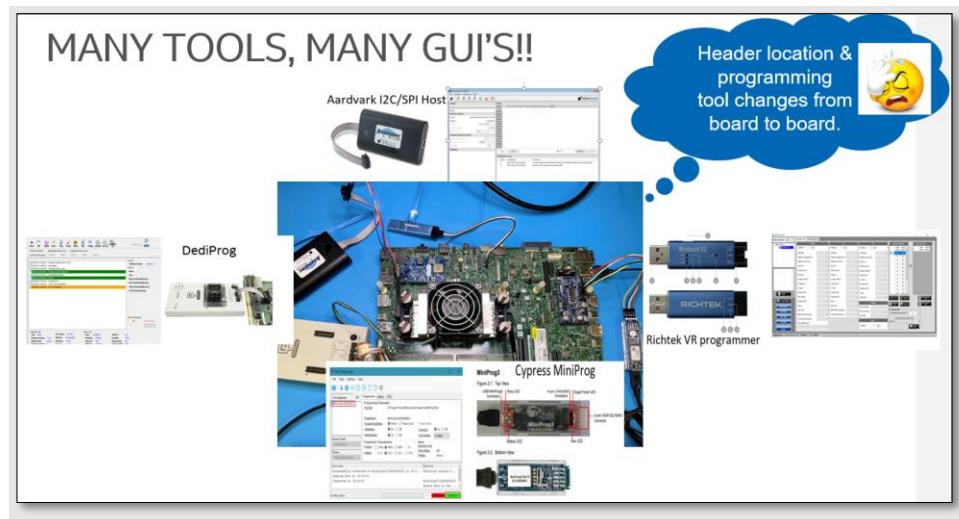
Intel RVP motherboard is the primary validation hardware for Intel CPUs and these motherboards host various ROM devices that store the firmware required. During debug and validation there is frequent need for updating these components and validation engineers need to identify the programming dongle for the ROM device, install the software utilities and drivers, identify where and how to connect the external programming dongle to the motherboard and then proceed for programming.

Traditionally, updating firmware on to each programmable components on Intel RVP motherboard users require different external programming hardware based on the communication protocol supported by the component like SPI NOR Flash for BIOS, I2C EEPROMs for Retimer, PD-Controllers, Firmware Records Unit, Programmable Voltage Regulator Controllers etc., on motherboard and these hardware modules when left attached to motherboard they gate systems from boot.

UCP SQUID is one tool supporting programming over SPI, I2C, SWD and JTAG. It also has GPIOs that connect to Front Panel HDR of RVP and help to get or set the system states. UCP SQUID also has tiny paddle boards and cables designed for needs of Intel RVPs as part of Hardware KIT. The paddle boards host FET devices which enable for systems to boot with UCP SQUID programmer connected to the platform, thus enabling the remote programming hardware tool for Validation teams.

A GUI software package to be installed on HOST PC that can identify the Intel RVP model name, List the reference designators of programming headers, and allows users to program each component individually or all devices in a single click of button. It also allows seamless integration to automation setups through APIs developed in Python, C#, and C++.

With UCP-SQUID **cost savings of about 75%** can be achieved by replacing the multiple programming hardware tools with single hardware module and GUI software significantly reduces time and effort of the users in identifying the ref.des of programming headers on motherboard, identifying the right programming dongle and Installation of each tool's software and drivers.

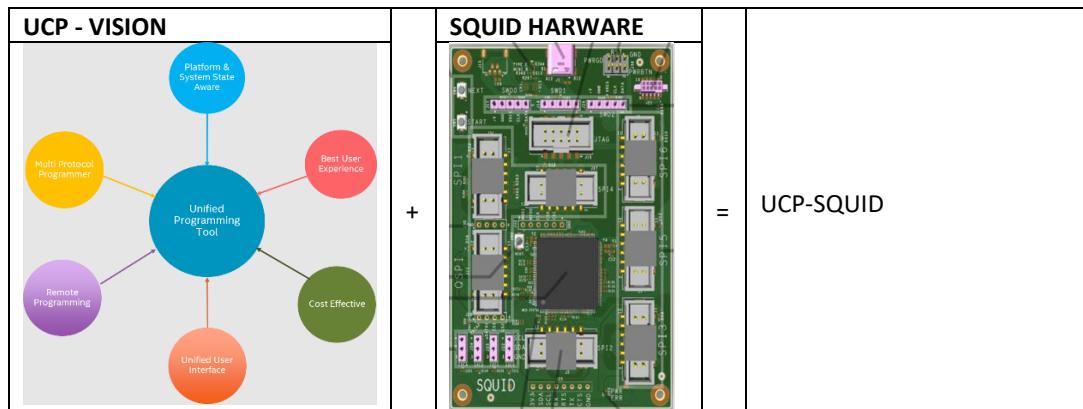


**Figure 104 : Different programmers to RVP & its challenge in locating header**

Current day changes to work models such as Hybrid / Remote increase the need for remote access to hardware and the current day third party programming tools limit this functionality as they are not system state aware and gate the SUT to proceed for boot. This problem is partially address by In-System programming approach by software, but they are dependent on functional status of hardware.

## 34.2 Solution

UCP (Universal Configurable Programmer) is the vision of Platform and Systems Engineering RVP (CCG-CPS-CPE-PSE-RVP) Team to address the problem statement and is realized using the SQUID Hardware developed by Intelligent Validation Tools Engineering Team(iVE-IDC).



**Figure 105 : UCP-Solution**

### 34.2.1

### Hardware

UCP-SQUID is a Micro-Controller based hardware that can support programming of up to 7-SPI Devices, 4 – I2C Devices, 3 – SWD Devices and 1 JTAG Interface port. It is connected to HOST as a USB device and the device and using the cables specifically developed for the requirement are used to connect to programming headers on the DUT. For the solution to system state aware a 2x3 pin header is provided on the hardware which can be cabled to Front Panel of the RVP to control the power button, reset button, and get the system power status. The Paddle boards mentioned in the Kit items host a FET isolation circuit that will allow to disconnect the programming cable connection load on to the RVP traces when not in use. Thus, enabling true remote programming operation for the system under test.

#### 34.2.1.1

#### Block Diagram

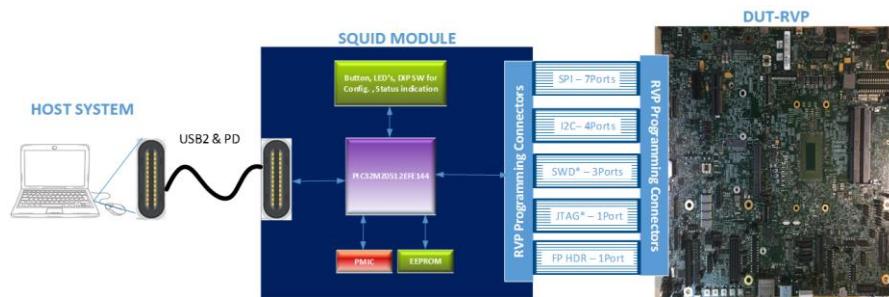


Figure 106 : UCP-Block diagram

#### 34.2.1.2

#### Kit-Items

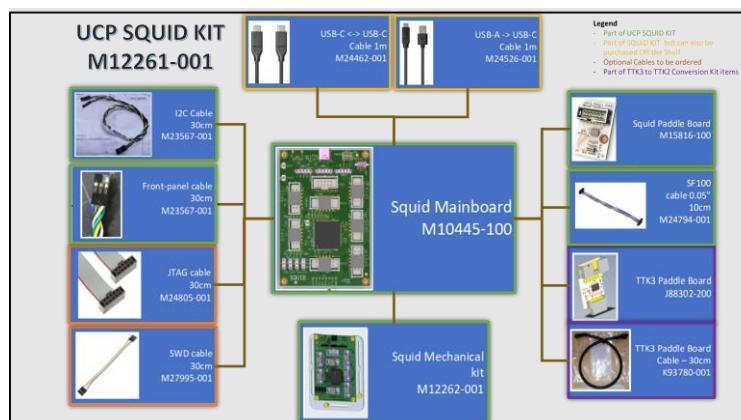


Figure 107 : UCP-Kit item

### 34.2.2

### Software

UCP-SQUID can be accessed through HOST PC either in API mode or GUI utility. The GUI utility automates scan for SQUID USB devices connected at launch and upon successful detection proceeds to identify the RVP Motherboard model by accessing the RFID/I2C Tag EEPROM chip on the motherboard. Once the detection is successful it lists all the programmable ref.des header on the platform from which

user can select choice of device then select the firmware image to programmed or request to readback content of the ROM device to file

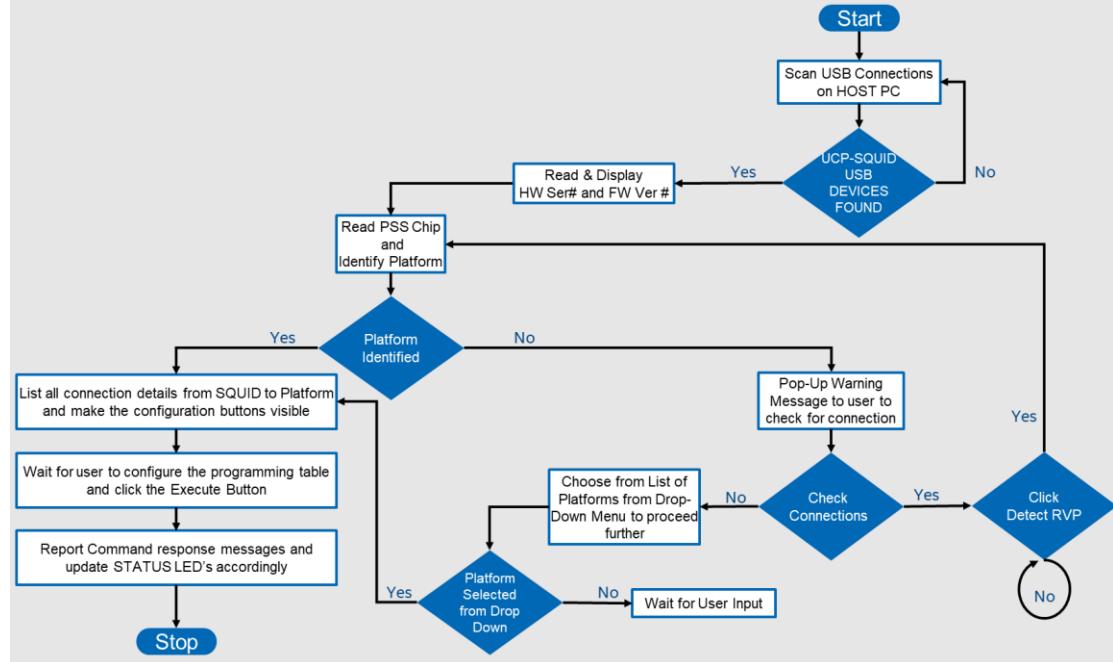


Figure 108 : UCP-SW flow

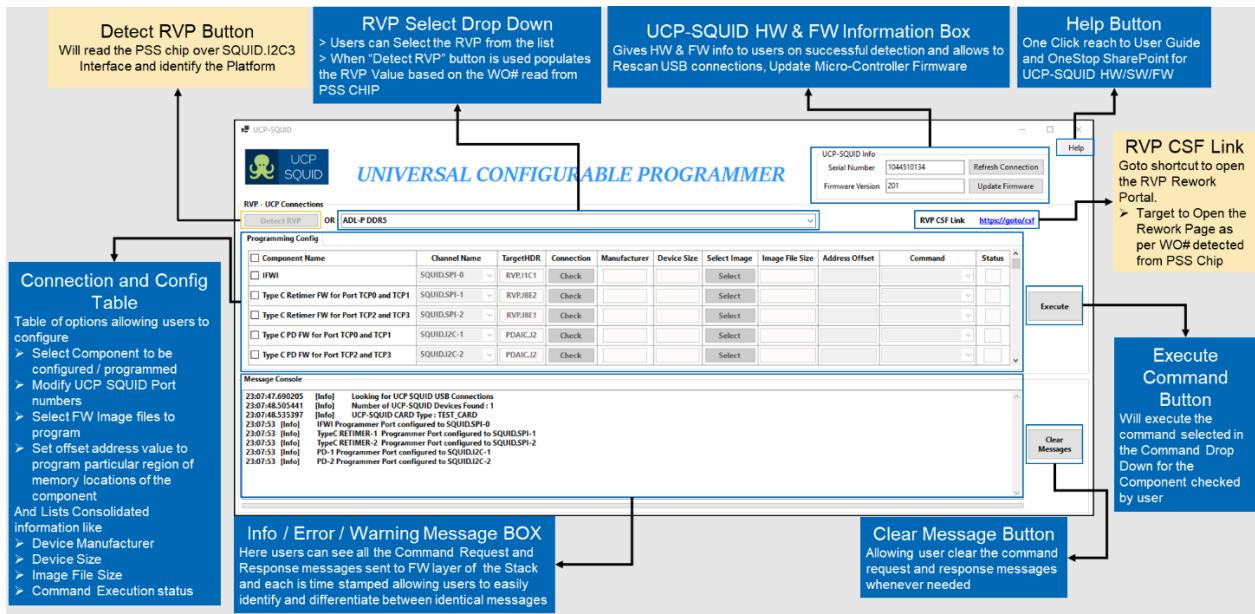


Figure 109 : UCP-GUI

### 34.3

### Cost of Solution

Today the solution is priced at \$ 250 including all required ingredients. However, we are working on a “low-cost” reduced version of SQUID. The final price should be defined soon.

More details about UCP SQUID can be accessed at below link:

\* [UCP SQUID Abstract Demo.pptx](#)

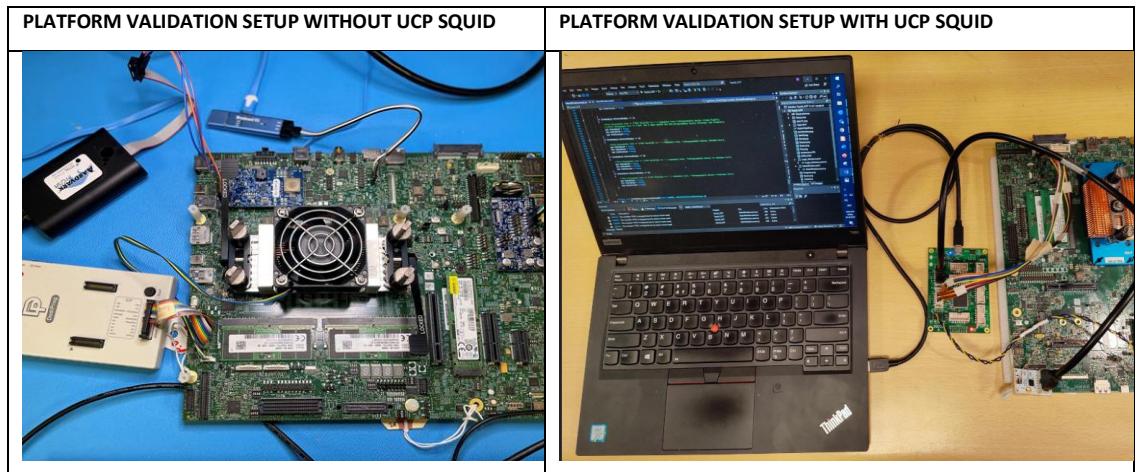


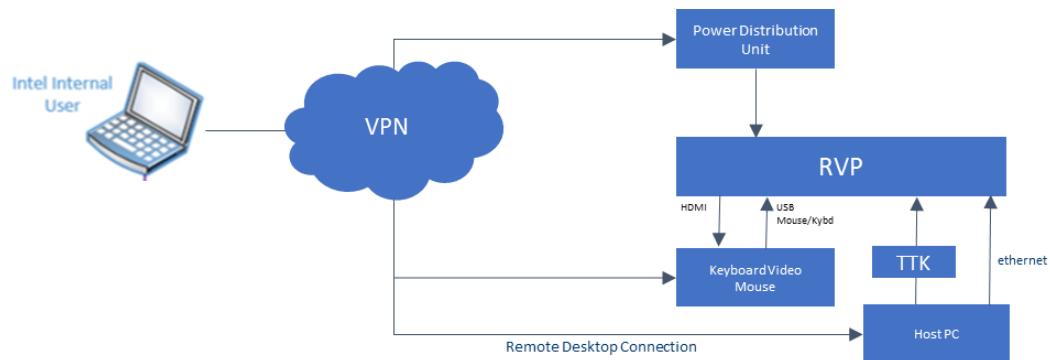
Figure 110 : SNAPSHOT OF UCP SQUID SETUP

# 35 RVP NEST

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## 35.1 Introduction

RVP NEST is a remote access farm hosted and maintained by RVP Team. Goal of RVP NEST is to enable early access to platform for the RVP users. RVP NEST gives the in-lab user experience and allows to remotely control the RVP by logging-in through Host PC.



**Figure 111 : RVP NEST Connection diagram**

By default, each setup has dedicated host in which KVM, IFWI flashing tool (e.g. TTK3 or DAC or UCP), BIOS serial cable, G3 Cycling support through IP PDU connected to RVP. On need basis, we shall support

- Setups can be made fully loaded GC or DC configs
- ITP-XDP debug tools shall be connected
- Flexible to any OS (Ubuntu/Centos/SVOS) on SUT
- Peripherals/3PE shall be connected
- Debug Acceleration Card (DAC) can be connected to platform, UCP, CBS
- Support post PRQ
- Optional/Feature Reworks will be supported

For more details on the RVP Nest User Guide, please visit the below wiki link:

<https://goto.intel.com/rvpnestwiki>