Adarsh Mittal

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Objective

Looking for internship opportunities in system roles involving applications of area such as computer architecture, memory systems, hardware acceleration and VLSI Systems

Education

University of Wisconsin, Madison, WI — Madison, USA
Master of Science in Computer Science; — *Expected May 2021*

Relevant Coursework: Computer Architecture, Operating Systems, Machine Learning, Artificial Intelligence.

Birla Institute of Technology & Science Pilani — Rajasthan, India
Bachelor of Technology in Electrical & Electronics Engineering; GPA: 4.0/4.0 — *Aug 2012 - May 2016*

Relevant Coursework: Data Structure & Algorithms, Object Oriented Programming, Digital Design, Microprocessor, Computer Architecture, Operating Systems, Machine Learning, Artificial Intelligence.

Skills

- **Languages**: Python, C, Java, Perl, Cuda(Basic), Verilog, Linux shell scripting. **Tools & Software**: ICC2, EDI, TensorFlow, ModelSim, gem5

Experience

University of Wisconsin Madison — Madison, USA
Course Project — *Aug 2019 - Present*

- Analysed FFT and SPLASH-2 benchmarks on Gem5 simulator, varying cache sizes and physical register for a 4-core, 64GB System.
- Co-related trends observed in parameters like miss rate, IPC, L2-cache bus traffic, execution cycles and branch mispredicts.

Nvidia Graphics — Bangalore, India
ASIC PD Engineer II — *May 2016 - June 2019*

- Accomplished 4 GPU/Mobile chip tapeouts on cutting edge 16/7 nm technology.
- Implemented (gate level netlist -> GDS) for sub-chiplet of 5+ blocks using EDA tool.
- Automation of Placement and Route flow by developing methodologies for optimizing Performance and Area.
- Leakage and Dynamic Power optimization based on Activity of nets and layer assignment to save 4% power.
- Worked on Floorplanning, Power Routing, Clock Tree Synthesis, logic cloning and Timing Closure.

BITS Pilani — Raj., India
Course Project — *May 2012 - July 2016*

- Design of 32 bit Out of Order Execution (using Tomasulo Algorithm) processor with Speculative Execution.
- Implemented various units: Register File, Dispatch Unit, Reservation Stations, Register Alias Table, Re Order Buffer & Issue Queue.
- Wrote driver functions for ISSUE, EXECUTE and WRITE modules with simulation in C.

Course Project

- Designed and verified data path and control unit of 5 stage in-order linear instruction Pipeline CPU Architecture on MIPS ISA.
- Analyzed various blocks (ALU, Memory, Control Unit) using data flow modelling and behavioral modelling using ModelSim.
- Incorporated hazard detection, stalling, forwarding and flushing mechanism in Verilog.

Study Oriented Project

- Analysis of different Cache Coherence Protocols and issues with Multi Core Cache Synchronization.
- Design and Implementation of MESI protocol to avoid problem of Cache Synchronization.

Technical University of Munich — Munich, Germany
Research Intern — *May 2015 - July 2015*

- Worked on IR Violation prediction of the circuit using Deep Learning Models.

Activities

- Hand written digit recognition using Deep Learning - Neural Networks using Forward and Backward Propagation with 79% accuracy.
- Smart devices for the Gym activities TIC Fit devices - Design and Prototyping the device by interfacing senors & microcontroller.
- Led team of 20 volunteers to methodized 1-week cleanliness drive at campus in collaboration with NGO.

Additional Experience & Achievements

- **University of Wisconsin** - Guaranteed Funding for research in Computer Arch. domain.
- **Merit Scholarship** award for outstanding Academic performance in undergraduate school- **BITS Pilani.**
- **DAAD Wise, Scholarship**, for working in Design Space Exploration project for SOC Architecture.
- Won *Best Technical Innovation* award (out of 800 students) at **Amity University Tech Fest 2016.**

Teaching Assistant

- Digital System and Design, Supervisor: Prof. Sudeep Mohan, BITS Pilani (2015)
- Introduction to Operating System, Supervisor: Prof. Andrea C. Arpaci-Dusseau, UW-Madison (2019)

Work Authorization

- Authorized to work full-time under CPT/OPT