Adarsh Patil

Personal Details

Date of Birth:	17 November 1990
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Portfolio / Blog:	http://adarshpatil.in
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Education

Current **Indian Institute Of Science**, Bangalore, India
M.Sc Engineering | Dept of Computer Science and Automation (In Progress)
Research: *High Performance Computing & Computer Architecture* | Advisor: R. Govindarajan
GPA: 6.33/8.0 | List of Courses

May 2012 **M S Ramaiah Institute of Technology**, Bangalore, India
Bachelor of Engineering | Dept of Computer Science and Engineering
GPA: 9.40/10.0 | List of Courses

June 2008 **Sindhi High School**, Hebbal, Bangalore, India
CBSE 12th
Percentage: 87.56 (PCM: 93) | List of Courses

July 2006 **Presidency School**, R T Nagar, Bangalore, India
ICSE 10th
Percentage: 86.5

Work Experience

June 2012 to July 2014 (2 years 1 month) — Technology Analyst at Goldman Sachs, Bangalore, India
Core Platform Engineering

Member of Operating Systems Engineering team under Core Platform Engineering primarily focused on Virtualization and Linux platforms

Was part of a wide variety of engineering projects ranging from Full blown Virtualization (*VMware ESX, KVM*), Nested Virtualization to Light weight Linux Containers (*LXC, Docker*)

Security Enhanced Linux, low latency Linux to think clients for desktops

Performance Engineering and Architect of Goldman Sachs Private Cloud for the virtualized footprint.

January 2012 to May 2012 (5 months) — Intern at Ignis Technology Solutions, Bangalore, India

Developed an Android application

For a Pharmaceutical ecommerce and Supply Chain Management - *Angooor*

June 2011 to August 2011 (3 months) — Summer Analyst at Goldman Sachs, Bangalore, India

Worked on Process Automation in Technology Division

Received Pre-Placement offer for "*disctinctive*" Performance

June 2010 to September 2010 (4 months) — Intern at Einstasoft, Bangalore, India (renamed GAViSTA Tech)

Worked on LegalCrystal.com - Indian Law Search Engine

Search Optimization and User Interface for systematic results display

Software & Hardware Proficiency

Software

- *Architectural Simulators:*
  gem5-gpu, gem5, DRAMSim, MARSSx86(QEMU based fast-functional simulator),
- *Programming Languages:*
  C / C++, Python, Linux Shell Scripting, Java, SQL, Perl
- *Development Platforms:*
  Eclipse, Vl / VIM, Visual Studio, Code::Blocks, Net Beans, DevCpp, gedit,
  TexMaker, Aptana Studio, Geany
- *Web Technology:*
  HTML, CSS, JQuery, Javascript, PHP, JSP, Curl, XML, REST, WSDL, Perl / Python CGI
- *Operating Systems:* VMware ESX, Linux(RHEL, Fedora, Ubuntu), Windows
- *Mobile Platforms:* Android
- *Libraries:* CUDA, OpenCL, OpenCV, OpenGL
- *Tools:* LaTeX , git, svn, hg, gdb
- *Automation Tool:* HP Operations Orchestrator, iConclude
- *Database:* MySQL, Oracle, DB2
- *Browser Based Applications:* Chrome apps and XULRunner

Hardware

- Hardware Accelerators
  Intel MIC (XeonPhi KNC) and NVIDIA GPGPUs (Fermi, Kepler)
- Micro-Architecture of Modern x86 CPUs
  (Nehalem / Westmere, SandyBridge / IvyBridge, Haswell)
- 8051 based Microcontroller Programming

Positions Held

- Student System Admin at CSA Department, IISc — Aug 2014 - present
- Technology Analyst - 01 at Goldman Sachs — Nov 2013 - Jul 2014
- New Analyst Technology Associate at Goldman Sachs — Jun 2012 - Nov 2013
- Teaching Associate for the CUDA Teaching Centre,
  sponsored by NVIDIA, at the Department of CSE, MSRIT — Jan 2012 - May 2012
- Chairman of VRGLINUG (GNU/Linux users group at MSRIT) — 2011-12
- Secretary and member of executive committee of IEEE-MSRIT — 2011-12
- Been an influential Member of several committees — 2011-12
  RoboMSR, Android AppDev Group, CodeMSRIT,
  Assoc of Computer Engineers (ACE)

Projects

Projects at Indian Institute of Science

Integrated Heterogeneous System (IHS) Architecture with shared Die-Stacked DRAM Cache [Paper submitted, Best Poster EECS'17]

Modern processors chips have heterogeneous processors, intergrating multi-core CPUs & general purpose accelerator GPUs on the same die. These IHS require larger & faster memory to improve overall system performance. Die-stacking technology allows high bandwidth and lower latency DRAM to be integrated close to the processor. Using this memory as shared cache brings novel challenges in resource sharing and request scheduling due to the architectural heterogeneity in these IHS processors which has varied implications on performance of the latency sensitive CPUs vs throughput oriented GPGPUs.

TLB and Pagewalk Performance in Multicore Architectures with Large Die-Stacked DRAM Cache [TO BE PUBLISHED]

The die-stacking technology promises a large capacity DRAMs, in the order of GBs, closer to processors. With such large capacity caches the amount of data that can be accessed without causing a TLB fault i.e. the reach of a TLB, (which is a few MBs on modern X86 processors) becomes severely inadequate. TLBs are on the critical path for data access and incurring an expensive page walk can hinder system performance, especially when data requested is already resident (hit) in the LLC.
http://adar.sh/tlb-pagewalk

Compiler Optimization Transforms 2: Caffe Neural Networks

The work focuses on 2 applications in Caffe - MNIST and CIFAR10.
By using loop parallelization transforms & tiling, performance of these Neural Network applications is improved for multicore machines.
We obtain speedup of between 1.8X-3X over best baseline implementation.
This work also compares thread scaling characteristics and layer wise timing distribution on AMD and Intel multicores vs GPUs.
http://adar.sh/caffe-compiler-optimize

Compiler Optimization Transforms 1: Harris Corner Detection

This work optimizes and tunes the Harris corner detection algorithm for performance using locality, vectorization and multithreading transforms.
We obtain a speedup for 14.6X over OpenCV library implementation and 11.3X over unparallelized reference implementation.
This work also studies performance of GCC 4.9 vs Intel ICC 15.0 for vectorization and code generation optimization performed by them.
http://adar.sh/compiler-optimize

VarMutate:Dynamic Scoping for C Language in clang

Implemented Dynamic Scoping for C in the clang/LLVM compiler via a single pass algorithm that implements shallow binding.
It scans the AST generated and does a source-to-source transform to convert a given program to dynamic scoped program.
http://adar.sh/VarMutate

A Study of Branch Prediction in Android

We focus on Hardware Branch Prediction and aim to understand the interplay for User and Kernel mode branches in Android in light of features like minimize & background app refresh
Simulated ARM CortexA8 chipset with ARMv7-A architecture profile & ran Moby Mobile Benchmark suite on customized gem5 simulator
http://adar.sh/BranchPredAndroid

Plan IKEBANA: ESS Dimensions Reduction for Plan Bouquet

Ranking Error Prone Selectivity Dimensions by impact on Plan Bouquet style query execution i.e. execution of query by discovering selectivity at run time by executing series of cost limited plans.
http://adar.sh/PlanIkebana

PROJECTS AT GOLDMAN SACHS

Architect, design, implement and sustain solutions of various Virtualization & Linux technologies spanning Compute, Storage and Networking.

Hardware and OS Performance Benchmarking & Analysis

- Authored an Automated benchmarking framework to run and report performance by running various test suite on VMs and Baremetals in bash
- Test Suites include – SpecJBB, kmake, blacksholes, Dhrystone, Whetstone, Hackbench, Disk tests, Network uperf, lat proc
- Performance analysis & tuning for specialized internal apps (e.g. Low Latency, high I/O, memory, network intensive)

Linux Containers

- Architecting and implementing Image based and Host based App Containers for Goldman Sachs Cloud within RHEL 7
- Possess a good understanding of underlying technology Namespaces, Cgroups, SELinux, Libvirt API for Management, Network configuration using TUN/TAP Dev

Thin client on desktop for VDI solution

- Engineered a Linux based solution – Minimized and locked down
- Authored several PyGTK and X11 based applications for remote management, diagnostics, troubleshooting and NEA
- Network booted, kickstart and preseed based unsupervised install Next generation to include stateless RAM-based network boot on ARM based hardware including Raspberry Pi.

Nested Virtualization

- Engineered NV as a security solution using Bromium vSentry

Well versed in **PXE / TFTP boot** infrastructure.

Regular **Vendor Interaction and liaising** – Intel, VMware, Redhat

PROJECTS AT M S RAMAIAH INST OF TECH

"Spoken Language Identification using Machine Learning"
under Prof. K.G.Srinivasa as final year project
http://adar.sh/spokenlang

"Intelligent systems for Network Intrusion Detection System"
facilitated and financed by DRDO under Prof. K.G.Srinivasa
Paper Published at ICECIT 2012 titled
"SNIDS: An Intelligent & Multiclass Support Vector Machines Based NIDS"
http://adar.sh/S-NIDS

Mini project on "Line Birds" – a computer graphics project implemented using OpenGL library under Prof D S Jayalakshmi
http://adar.sh/linebird

Mini project on "Implementation of parallel algorithm for Max Flow Algorithm using Ford-Fulkerson method" on Advanced Comp Arch under Asst Prof. Parkavi

Project on "e-Blood Bank" a Database Systems Application Project under Asst. Prof. Arul Kumar

Lead developer of the team that created "ANDROMEDA - MSRIT Linux"

Achievements

- Best Poster at Electrical Science Division Symposium (EECS '17) at IISc, Bangalore

- Represented IISc at 12 hour stadium relay run Bengaluru 2016 (22 km in 2 hours)

- Completed with Certificate of distinction several MooC Data Science Courses from Johns Hopkins University on Coursera

- *"Best outgoing achiever of 2012 batch"* from the Dept. of Computer Science & Engg. at M S Ramaiah Instiute of Technology

- First Place at the National Level Project Competition & Exhibition held at M S Ramaiah Institute of Technology for project "Spoken Language Identification using Machine Learning"

- Second Place at "Random Hacks of Kindness #2" hackathon (2010)

- IBM Certified DB2 9 Database and Application Fundamentals (2011)
- IBM Certified Rational Functional Tester(RFT) for Java (2011)
- Certificate course in "Java Programming" from NIIT-Bangalore by Sun Microsystems (2009)

- Field study titled "Microneedles for medical advancement" as a part of the MEMS course which was recognized by the Staff Council of IEEE MSRIT.
- Credited broad course electives like "Micro-Electro Mechanical Systems (MEMS)", "Digital Signal Processing" and "Supply Chain Management" at MSRIT

Co and extra curricular activities

- Routinely participate in competitive timed runs including TCS World 10k, Bengaluru 10k Challenge, Standard Chartered Mumbai Marathon, Bengaluru Marathon etc.
My personal best times are - *5k(22mins), 10k(48mins) and half marathon (1:55hrs)*

- Periodically author blog articles about my experiences, assessments and outlooks related to my work and hobbies

- Web Design, Development and treasurer for Samanway 2014 - Career fair at IISc

- Member of the Environment committee at Goldman Sachs, regularly conducting awareness drives and camps

- One of few Indians amongst participants from all around the world on a Scholarship Delegation to attend TEDxSummit in Doha, Qatar representing TEDxMSRIT

- TEDx licensee, TED Translator, 1600 TEDCred holder and organizer of TEDxMSRIT
- Involved in various communities and organizing of "Pycon India 2010" and "Random Hacks of Kindness #4" held in MSRIT
- Active Volunteer for Association of Computer Engineers (ACE), IEEE-MSRIT and have been instrumental in organizing several fests and events (2008-2011)
- Delegated at various conferences and Workshops - IEEE International Parallel & Distributed Processing Symposium (IPDPS 2015), Open Hack India 2010/2011, PYCON India 2010, FOSSEE Science and Engineering, Microsoft Dream Spark India, Wikipedia Bangalore Meet-ups, Mobile Camps to name a few

Miscellaneous

Strengths

- Adaptability, Quick learner, Hardworking and Dedication
- Effective communicator and good leadership skills
- Always updated with latest technology and trends of market.
- Analytical and Mathematical Problem Solving, Designing Algorithms and practical Solutions to given problems

Hobbies

- An avid Running, cycling and Swimming enthusiast
- Reading Major Tech News sites, dailies and magazines [LFY, Digit, Chip, etc.]
- Programming, Solving challenging problems either conceptually or programtically

Other Links

github.com/adarshpatil
in.linkedin.com/in/adarshpatil

References

Academic References

Prof. R Govindarajan, Guide
Professor and Chairman SERC, IISc
govind@serc.iisc.ernet.in

Prof. K G Srivinvas, Mentor / Guide
Professor and Head of Dept. CSE, MSRIT
kgsrinivas@msrit.edu

Industry References

On Request

Master of Science in Engineering (IISc, Bangalore)

Grades

Course	Grade	Credit
Database Management Systems	A	4
Computer Architecture	A	4
Design and Analysis of Algorithms	C	4
Compiler Design (NOT IN RTP)	B	-
Final Thesis	In	Progress
	Total	16
	Gpa	**6.33**

Bachelors in Engineering (M S Ramaiah Inst. of Tech, Bangalore)

Principal Courses

- Engineering Mathematics
- Data Structures
- Operating Systems
- Engineering Design
- Web Programming
- Unix System Programming
- Compiler Design
- Discrete Mathematics
- Design & Analysis of Algorithms
- Computer Organization
- Computer Graphics and Visualization
- Advanced Computer Architecture
- Computer Networks
- Software Engineering

Electives

- Artificial Intelligence
- Digital Signal Processing
- Supply Chain Management
- Micro-Electro Mechanical Systems

Higher Secondary (Sindhi High School, CBSE)

Primary Courses

Physics, Chemistry, Mathematics, Computer Science

Languages

Hindi, English
