Parallel Iterative Matching & iSLIP

(Deadline SEP-25, 2059 hrs)

1. Project Description

The objective of this assignment is to thoroughly understand Parallel Iterative Matching(PIM) and iSLIP scheduling algorithms. Implement PIM and iSLIP scheduling algorithms for a NxN switch with inputs described in next section.

2. Inputs

- Switch 8x8 with uniform traffic

In-Port	O/p Port
Port-1	[1 2 3 4 5 6 7 8]
Port-2	[2 3 4 1 5 8 7 6]
Port-3	[1 3 5 7 2 4 6 8]
Port-4	[1 2 5 7 8 3 4 6]
Port-5	[3 5 7 8 1 2 4 6]
Port-6	[1 2 3 4 5 6 7 8]
Port-7	[2 4 6 8 1 3 5 7]
Port-8	[8 6 7 1 2 3 5 4]

- Switch 4x4 with FullSkew traffic

In-Port	O/p Port
Port-1	[1 2 3 4]
Port-2	[2]
Port-3	[3]
Port-4	[4]

- Switch 8x8 with FullCycle traffic

In-Port	O/p Port
Port-1	[1 2 3 4 5 6 7 8]
Port-2	[3]
Port-3	[3]
Port-4	[5]
Port-5	[5]
Port-6	[7]
Port-7	[7]
Port-8	[-]

3. Output

Compare the number of iterations in each round for each algorithm. The output from both the programs should be compared with each other.

4. What to submit?

A single zip file containing

--> Source files
--> Makefile
--> README file that explains how to compile and run the program; whether your program works correctly or whether there are any known bugs/errors in your program

6. Grading

--> Correct implementation
--> Viva voce

7. Policies

--> Penalties will be there for any form of academic dishonesty, plagiarism, etc. There should be no downloaded code.
--> Software for checking plagiarism of the code will be used.
--> The program can be written in C/C++/Java/python/MATLAB.