Capacitive Controller ICs

Capacitive Switch Controller IC (Switch)

BU21077MUV

General Description

BU21077MUV is a capacitive switch controller for switch operation. Low power consumption can be realized by an intermittent detection mode. This IC supports regular simple switches and matrix switches that sensors are arranged in a matrix form. It performs automatically calibration when detect noise and temperature variation.

Features

- 8 Capacitive Sensor Ports
- Low Current Consumption by Intermittent Detection Mode
- Matrix Switch (Maximum 16 switches)
- Long press detection
- Automatic Calibration
- Interrupt controller
- 2-wire Serial Bus Interface
- Single Power Supply
- IC Containing Power-on-Reset and Oscillator

Applications

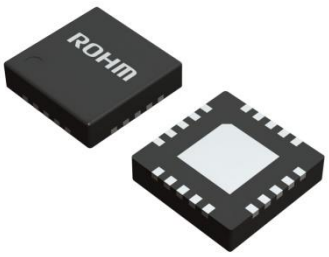
- Portable Device such as Smart Phone, PDA.
- Electronic Device with Multi Switches.
- Information Appliance such as Projector.
- AV Appliance such as Digital TV, HDD recorder.
- PC / PC Peripheral Equipment such as Laptop PC.

Key Specifications

- Input voltage Range 2.7 to 5.5V
- Operating Temperature Range -20 to +85°C
- Operating Current 75μA (Typ in Intermittent mode)
- Detecting cycle 8ms (Typ)

Package

VQFN020V4040 4.00 ㎜×4.00 ㎜×1.00 ㎜



Typical Application Circuit

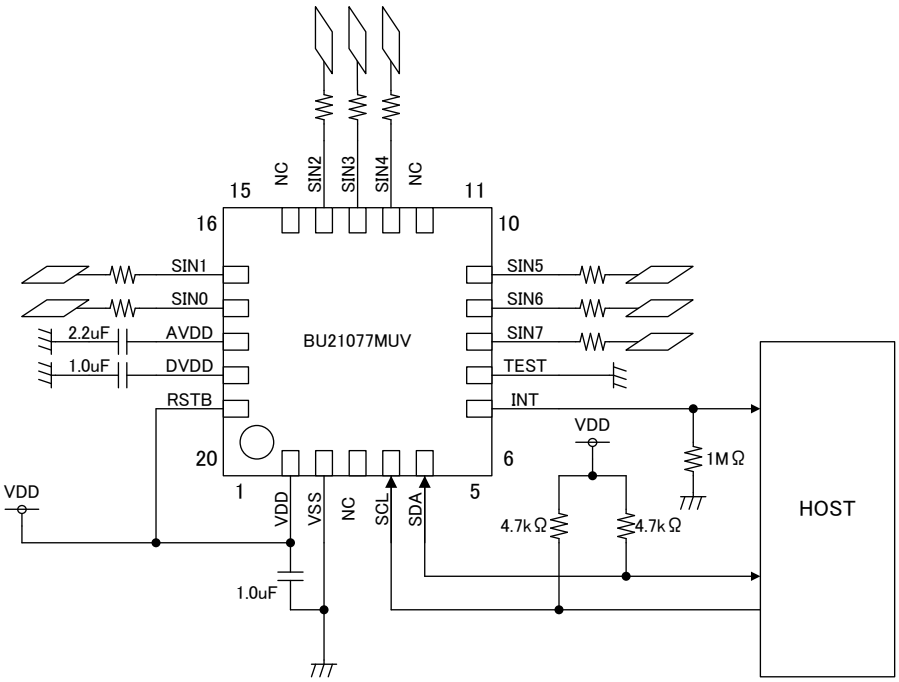


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configurations

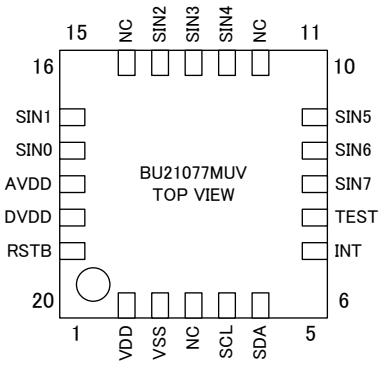


Figure 2. Pin Configrations

Pin Descriptions

Pin No.	Pin Name	I/O	Functions	Note	Power	Initial Condition (During Reset)	I/O Equivalent Circuit
1	VDD	Power	Power		-	-	-
2	VSS	Ground	Ground		-	-	-
3	NC	-	-		-	-	-
4	SCL	In	Host I/F SCL		VDD	Hi-Z	b
5	SDA	InOut	Host I/F SDA		VDD	Hi-Z	b
6	INT	Out	Interrupt output	Active ‘H’	VDD	Hi-Z	b
7	TEST	In	Test input	Fix ‘L’ at the normal operation	VDD	Hi-Z	c
8	SIN7	InOut	Sensor 7		AVDD	Hi-Z	a
9	SIN6	InOut	Sensor 6		AVDD	Hi-Z	a
10	SIN5	InOut	Sensor 5		AVDD	Hi-Z	a
11	NC	-	-		-	-	-
12	SIN4	InOut	Sensor 4		AVDD	Hi-Z	a
13	SIN3	InOut	Sensor 3		AVDD	Hi-Z	a
14	SIN2	InOut	Sensor 2		AVDD	Hi-Z	a
15	NC	-	-		-	-	-
16	SIN1	InOut	Sensor 1		AVDD	Hi-Z	a
17	SIN0	InOut	Sensor 0		AVDD	Hi-Z	a
18	AVDD	Power	LDO output for analog blocks		-	-	-
19	DVDD	Power	LDO output for digital blocks		-	-	-
20	RSTB	In	Reset bar input	Active ‘L’	VDD	Hi-Z	c

I/O Equivalent Circuits

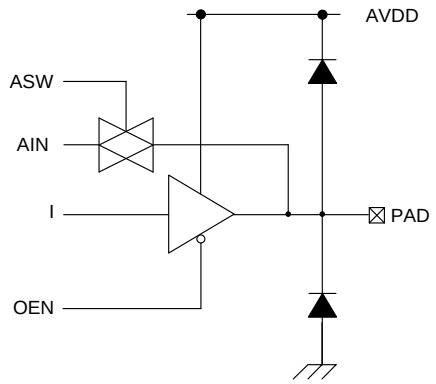


Figure 3. I/O Equivalent Circuit (a)

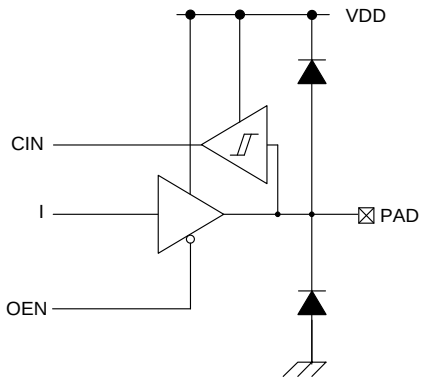


Figure 4. I/O Equivalent Circuit (b)

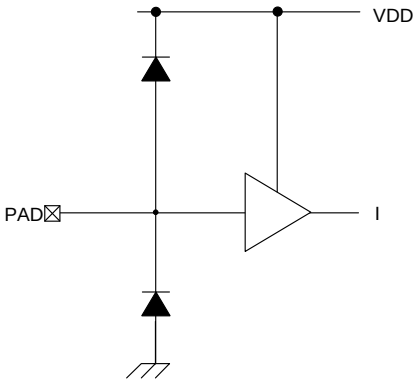


Figure 5. I/O Equivalent Circuit (c)

Block Diagram

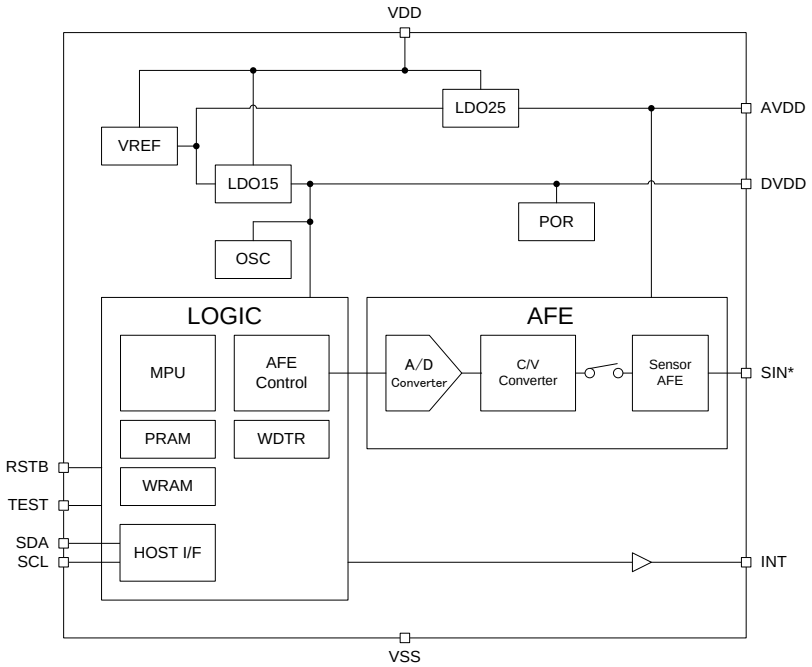


Figure 6. Block Diagram

Description of Blocks

●Sensor AFE, C/V Converter
This block converts from capacitance to voltage for each sensor
●A/D Converter
This block converts from analog value to digital value
●LDO25
This block is 2.5V output LDO regulator for Sensor AFE, C/V Converter, and A/D converter.
●LDO15
This block is 1.5V output LDO regulator for OSC and Logic blocks.
●OSC
This block is oscillator for MPU and Logic.
●POR
This block is Power-On-Reset for system reset.
●MPU
This block performs ON/OFF detection of switches and an automatic calibration based on the detection results.
●PRAM
This block is 8kbyte Program RAM for MPU. This block needs to download program from host.
●WRAM
This block is Working RAM for MPU.
●HOST I/F
2-wire serial bus interface compatible with I2C protocol.
●AFE Control
This block is control sequencer for Sensor AFE, C/V Converter, and A/D Converter.
●WDTR
This block is watchdog timer reset. System reset is performed when the MUP is hang-upped.

Host Interface

Communication with BU21077MUV is accomplished via 2-wire serial bus interface. It is compatible with I2C protocol and BU21077MUV is a slave device. Slave address of BU21077MUV is 5Ch (7-bit notation). And it supports Standard-mode (100 KHz) and Fast-mode (400 kHz). It has sequential read for reduce access time.

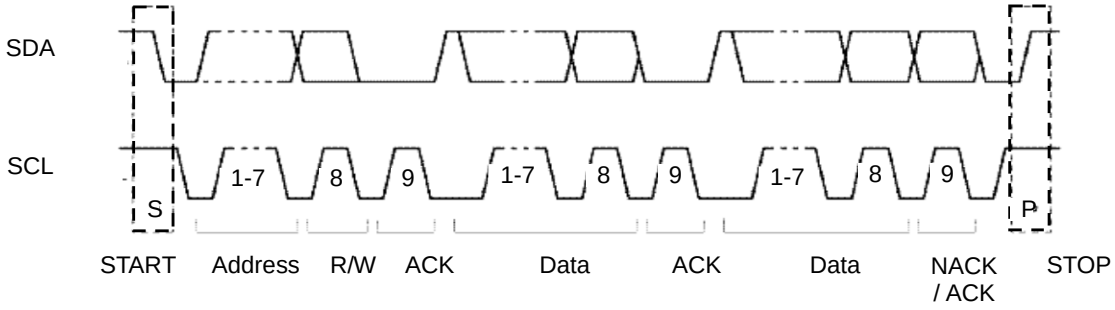


Figure 7. 2-wire Serial Bus Interface Data Format

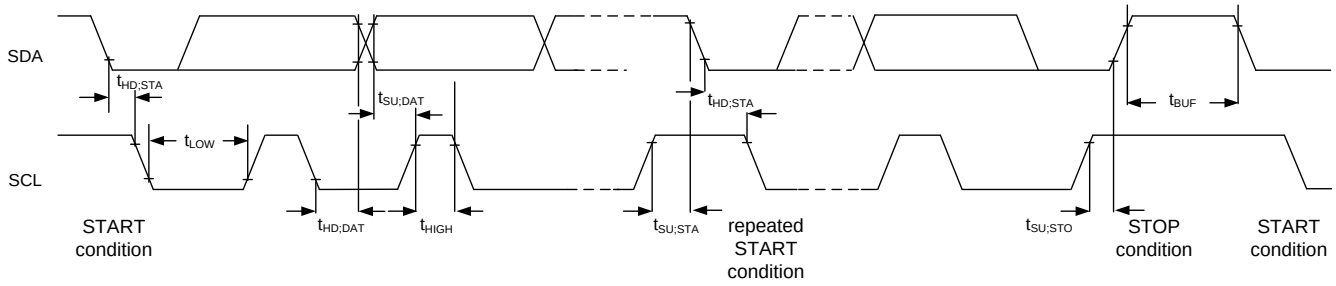


Figure 8. 2-wire Serial Bus Interface Timing Chart

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time for (Repeated) START Condition	$t_{HD;STA}$	4.0	-	0.6	-	µs
Low Period of SCL	t_{LOW}	4.7	-	1.3	-	µs
High Period of SCL	t_{HIGH}	4.0	-	0.6	-	µs
Data Hold Time	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	µs
Data Setup Time	$t_{SU;DAT}$	0.25	-	0.1	-	µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Setup Time for STOP Condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus Free Time Between STOP and START Condition	t_{BUF}	4.7	-	1.3	-	µs

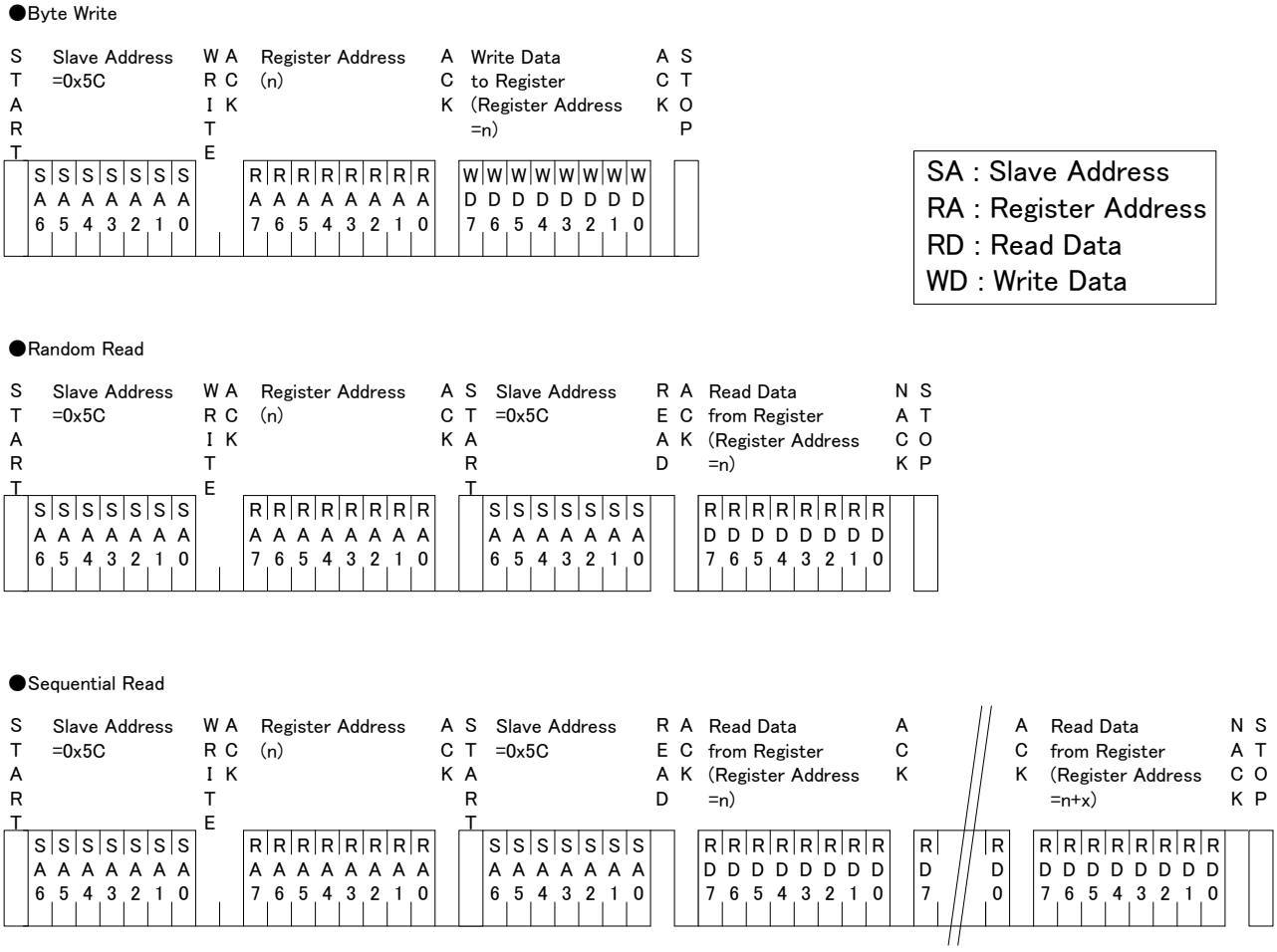


Figure 9. 2-wire Serial Bus Protocol

Overview

BU21077MUV is a capacitive sensor controller for switch operation. It contains analog front end (AFE) for detecting capacitance, analog to digital (A/D) converter, micro processing unit (MPU), 2-wire serial bus interface compatible with I2C protocol, power-on-reset circuit, oscillators, and low dropout regulator. And it works with a supply 2.7 to 5.5V voltage.
The results of detected switches state are kept to each register. If external noise and temperature variation are detected, automatic self-calibration is performed.

- Intermittent operation
  For low power operation, BU21077MUV shifts from normal operation to intermittent operation when the sensing results are stable with the state of switch OFF. It shifts from intermittent operation to normal operation when the sensing results are unstable.

- Simple switch
  One sensor is assigned to one switch. This IC has registers for showing the detected results (ON/OFF/LONG PRESS). It supports multi-simultaneous detection.

- Matrix switch
  The cross points of the sensors which are arranged in a matrix form are assigned to switches. This IC has registers for showing the detected results (ON/OFF/LONG PRESS). It does not support multi-simultaneous detection for matrix switches. Please set mask register about unused matrix switches. It supports 16 matrix switches arranged by a 4x4 matrix.

- Automatic self-calibration
  BU21077MUV monitors the neighboring situation by a detection result. If it detects external noise and a temperature drift, it executes the automatic self-calibration to get a stable detection result.

- Host Interface
  Communication with BU21077MUV is accomplished via 2-wire serial bus interface. It is compatible with I2C protocol and BU21077MUV is a slave device. Slave address of BU21077MUV is 5Ch (7-bit notation).

Register Map

Accessing the reserved area is prohibited.

0x00-0xBF

Address	Name	R/W	Ini	7	6	5	4	3	2	1	0
0x00	SIN_DATA0	R	0x00	SD_SIN0							
0x01	SIN_DATA1	R	0x00	SD_SIN1							
0x02	SIN_DATA2	R	0x00	SD_SIN2							
0x03	SIN_DATA3	R	0x00	SD_SIN3							
0x04	SIN_DATA4	R	0x00	SD_SIN4							
0x05	SIN_DATA5	R	0x00	SD_SIN5							
0x06	SIN_DATA6	R	0x00	SD_SIN6							
0x07	SIN_DATA7	R	0x00	SD_SIN7							
0x08	SIN_DATA8	R	0x00	SD_SIN8							
0x09	Reserved	R	0x00	-							
0x0A	Reserved	R	0x00	-							
0x0B	Reserved	R	0x00	-							
0x0C	Reserved	R	0x00	-							
0x0D	Reserved	R	0x00	-							
0x0E	Reserved	R	0x00	-							
0x0F	Reserved	R	0x00	-							
0x10	INT_STATE	R	0x00	CONTDET	OFFDET	ONDET	PERCAL	WDT	RECAL	CAL	INI
0x11	SW_STATE	R	0x00	SW7_STAT	SW6_STAT	SW5_STAT	SW4_STAT	SW3_STAT	SW2_STAT	SW1_STAT	SW0_STAT
0x12	Reserved	R	0x00	-							
0x13	DETECT_SW_ON	R	0x00	SW7_ON	SW6_ON	SW5_ON	SW4_ON	SW3_ON	SW2_ON	SW1_ON	SW0_ON
0x14	Reserved	R	0x00	-							
0x15	DETECT_SLIDERON	R	0x00	SLID_ON	SLID_KEEP	SLID_CNT					
0x16	DETECT_MAT_ON	R	0x00	MAT_ON	-			KEY_ON			
0x17	DETECT_SW_OFF	R	0x00	SW7_OFF	SW6_OFF	SW5_OFF	SW4_OFF	SW3_OFF	SW2_OFF	SW1_OFF	SW0_OFF
0x18	Reserved	R	0x00	-							
0x19	DETECT_SLIDER_OFF	R	0x00	SLID_OFF	-	SLIDLAST					
0x1A	DETECT_MAT_OFF	R	0x00	MAT_OFF	-			KEY_OFF			
0x1B	DETECT_SW_CONT	R	0x00	SW7_CONT	SW6_CONT	SW5_CONT	SW4_CONT	SW3_CONT	SW2_CONT	SW1_CONT	SW0_CONT
0x1C	DETECT_MAT_CONT	R	0x00	MAT_CONT	-			KEY_CONT			
0x1D	CONTROL_STATE	R	0x00	E_CALIB	-	-	-	-	-	INTM	D_CALIB
0x1E	RACT	R	0x00	RACT							
0x1F	Reserved	R	0x00	-							
0x20-84	Reserved	-	-	-							
0x85	SOFTRESET0	R/W	0x00	SRST[7:0]							
0x86-89	Reserved	-	-	-							
0x8A	SOFTRESET1	R/W	0x00	SRST[15:8]							
0x8B-AF	Reserved	-	-	-							
0xB0	DLSETTING	R/W	0x00	-						MPUEN	OSCEN
0xB1	Reserved	-	-	-							
0xB2	DLCLR	R/W	0x00	-							DLCLR
0xB3	DLDAT0	R/W	0x00	DLDAT[7:0]							
0xB4	DLDAT1	R/W	0x00	DLDAT[15:8]							
0xB5	DLDAT2	R/W	0x00	DLDAT[23:16]							
0xB6	DLDAT3	R/W	0x00	DLDAT[31:24]							
0xB7	DLRES	R	0x00	-				DL_FAIL	DL_PASS	-	-
0xB8	CKSUM0	R	0x00	CKSUM[7:0]							
0xB9	CKSUM1	R	0x00	CKSUM[15:8]							
0xBA	CKSUM2	R	0x00	-		CKSUM[21:16]					
0xBB-BF	Reserved	-	-	-							

Register Map-continued

Accessing the reserved area is prohibited.

0xC0-0xFF

Address	Name	R/W	Ini	7	6	5	4	3	2	1	0
0xC0	SEL_SIN_1_0	R/W	0x00	GA_SIN1		ON_SIN1		GA_SIN0		ON_SIN0	
0xC1	SEL_SIN_3_2	R/W	0x00	GA_SIN3		ON_SIN3		GA_SIN2		ON_SIN2	
0xC2	SEL_SIN_5_4	R/W	0x00	GA_SIN5		ON_SIN5		GA_SIN4		ON_SIN4	
0xC3	SEL_SIN_7_6	R/W	0x00	GA_SIN7		ON_SIN7		GA_SIN6		ON_SIN6	
0xC4	SEL_SIN_x_8	R/W	0x00	-		-		GA_SIN8		ON_SIN8	
0xC5	Reserved	R/W	0x00	-							
0xC6	Reserved	R/W	0x00	-							
0xC7	Reserved	R/W	0x00	-							
0xC8	GAIN_1_0	R/W	0x00	GA1				GA0			
0xC9	GAIN_x_2	R/W	0x00	-				GA2			
0xCA	ON_TH0	R/W	0x00	ON0							
0xCB	ON_TH1	R/W	0x00	ON1							
0xCC	ON_TH2	R/W	0x00	ON2							
0xCD	OFF_TH	R/W	0x00	-	OFF						
0xCE	CHATTERING	R/W	0x00	-				CHATTER			
0xCF	CONT_TIME	R/W	0x00	CONTSEL	-	CONT					
0xD0	MSK_INT_STATE	R/W	0x00	-	-	-	MSK_PERCAL	MSK_WDT	MSK_RECAL	MSK_CAL	-
0xD1	MSK_SW	R/W	0x00	MSK_SW7	MSK_SW6	MSK_SW5	MSK_SW4	MSK_SW3	MSK_SW2	MSK_SW1	MSK_SW0
0xD2	MSK_MAT0	R/W	0x00	MSK_KEY07	MSK_KEY06	MSK_KEY05	MSK_KEY04	MSK_KEY03	MSK_KEY02	MSK_KEY01	MSK_KEY00
0xD3	MSK_MAT1	R/W	0x00	MSK_KEY15	MSK_KEY14	MSK_KEY13	MSK_KEYM12	MSK_KEY11	MSK_KEY10	MSK_KEY09	MSK_KEY08
0xD4	SENS_SETTING	R/W	0x00	KEEP_SENS_NUM				UNIT_SENS_NUM			
0xD5	TH_INTERMITTENT_H	R/W	0x00	TH_INTM[15:8]							
0xD6	TH_INTERMITTENT_L	R/W	0x00	TH_INTM[7:0]							
0xD7	OUTPUT_OFFSET	R/W	0x00	OUTPUT_OFFSET							
0xD8	Reserved	R/W	0x00	-							
0xD9	Reserved	R/W	0x00	-							
0xDA	Reserved	R/W	0x00	-							
0xDB	Reserved	R/W	0x00	-							
0xDC	Reserved	R/W	0x00	-							
0xDD	Reserved	R/W	0x00	-							
0xDE	Reserved	R/W	0x00	-							
0xDF	EN_SLIDER	R/W	0x00	EN_SLID_SIN7	EN_SLID_SIN6	EN_SLID_SIN5	EN_SLID_SIN4	EN_SLID_SIN3	EN_SLID_SIN2	EN_SLID_SIN1	EN_SLID_SIN0
0xE0	MODE_SETTING0	R/W	0x00	-	-	FIX_BASE_CYC	FIX_SENS_CYC	-	SLID_LOOP	EN_DSLP	DET_MOD
0xE1	MODE_SETTING1	R/W	0x00	DIS_SIN8	-	MEDIAN_DIS	PERCAL_DIS	RETURN_DIS	HOPPING_DIS	ERROR_DIS	DRIFT_DIS
0xE2	EN_SIN	R/W	0x00	EN_SIN7	EN_SIN6	EN_SIN5	EN_SIN4	EN_SIN3	EN_SIN2	EN_SIN1	EN_SIN0
0xE3	SENS_NUM	R/W	0x00	SENS_NUM							
0xE4	SENS_RD_TIME	R/W	0x00	SENS_RD_TIME							
0xE5	SENS_RST_TIME	R/W	0x00	SENS_RST_TIME							
0xE6	SENS_IRST_TIME	R/W	0x00	SENS_IRST_TIME							
0xE7	CHK_NUM	R/W	0x00	CHK_NUM							
0xE8	CHK_RD_TIME	R/W	0x00	CHK_RD_TIME							
0xE9	CHK_RST_TIME	R/W	0x00	CHK_RST_TIME							
0xEA	CHK_IRST_TIME	R/W	0x00	CHK_IRST_TIME							
0xEB	DIG_GAIN	R/W	0x00	CHK_DIG_GAIN				SENS_DIG_GAIN			
0xEC	CHK_WAIT_TIME	R/W	0x00	CHK_WAIT_TIME							
0xED	SENS_WAIT_TIME	R/W	0x00	SENS_WAIT_TIME							
0xEE	CALIB_SETTING0	R/W	0x00	RET_NUM							
0xEF	CALIB_SETTING1	R/W	0x00	PRECAL_PERIOD				DRIFT_SIN_NUM			
0xF0	CLR_INT_STATE	R/W	0x00	-	-	-	C_PERCAL	C_WDT	C_RECAL	C_CAL	C_INI
0xF1	Reserved	R/W	0x00	-							
0xF2	Reserved	R/W	0x00	-							
0xF3	CLR_SW_ON	R/W	0x00	C_SW7_ON	C_SW6_ON	C_SW5_ON	C_SW4_ON	C_SW3_ON	C_SW2_ON	C_SW1_ON	C_SW0_ON
0xF4	Reserved	R/W	0x00	-							
0xF5	CLR_SLIDER_ON	R/W	0x00	C_SLID_ON	-	-	-	-	-	-	-
0xF6	CLR_MAT_ON	R/W	0x00	C_MAT_ON	-	-	-	-	-	-	-
0xF7	CLR _SW_OFF	R/W	0x00	C_SW7_OFF	C_SW6_OFF	C_SW5_OFF	C_SW4_OFF	C_SW3_OFF	C_SW2_OFF	C_SW1_OFF	C_SW0_OFF
0xF8	Reserved	R/W	0x00	-							
0xF9	CLR_SILDER_OFF	R/W	0x00	C_SLID_OFF	-	-	-	-	-	-	-
0xFA	CLR_MAT_OFF	R/W	0x00	C_MAT_OFF	-	-	-	-	-	-	-
0xFB	CLR_SW_CONT	R/W	0x00	C_SW7_CONT	C_SW6_CONT	C_SW5_CONT	C_SW4_CONT	C_SW3_CONT	C_SW2_CONT	C_SW1_CONT	C_SW0_CONT
0xFC	CLR_MAT_CONT	R/W	0x00	C_MAT_CONT	-	-	-	-	-	-	-
0xFD	Reserved	R/W	0x00	-							
0xFE	WACT	R/W	0x00	WACT							
0xFF	CONTROL	R/W	0x00	-	-	-	CALMOD	-	CFG	CALIB	ACT

Register Description

(OSC = 50MHz, unless otherwise noted).

【0x00-0x08 : Sensor Data】

Name: SIN_DATA
Address: 0x00-0x08
Description: These registers are 8-bit sensor data.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	SD_SIN0[7]	SD_SIN0[6]	SD_SIN0[5]	SD_SIN0[4]	SD_SIN0[3]	SD_SIN0[2]	SD_SIN0[1]	SD_SIN0[0]
0x01	SD_SIN1[7]	SD_SIN1[6]	SD_SIN1[5]	SD_SIN1[4]	SD_SIN1[3]	SD_SIN1[2]	SD_SIN1[1]	SD_SIN1[0]
0x02	SD_SIN2[7]	SD_SIN2[6]	SD_SIN2[5]	SD_SIN2[4]	SD_SIN2[3]	SD_SIN2[2]	SD_SIN2[1]	SD_SIN2[0]
0x03	SD_SIN3[7]	SD_SIN3[6]	SD_SIN3[5]	SD_SIN3[4]	SD_SIN3[3]	SD_SIN3[2]	SD_SIN3[1]	SD_SIN3[0]
0x04	SD_SIN4[7]	SD_SIN4[6]	SD_SIN4[5]	SD_SIN4[4]	SD_SIN4[3]	SD_SIN4[2]	SD_SIN4[1]	SD_SIN4[0]
0x05	SD_SIN5[7]	SD_SIN5[6]	SD_SIN5[5]	SD_SIN5[4]	SD_SIN5[3]	SD_SIN5[2]	SD_SIN5[1]	SD_SIN5[0]
0x06	SD_SIN6[7]	SD_SIN6[6]	SD_SIN6[5]	SD_SIN6[4]	SD_SIN6[3]	SD_SIN6[2]	SD_SIN6[1]	SD_SIN6[0]
0x07	SD_SIN7[7]	SD_SIN7[6]	SD_SIN7[5]	SD_SIN7[4]	SD_SIN7[3]	SD_SIN7[2]	SD_SIN7[1]	SD_SIN7[0]
0x08	SD_SIN8[7]	SD_SIN8[6]	SD_SIN8[5]	SD_SIN8[4]	SD_SIN8[3]	SD_SIN8[2]	SD_SIN8[1]	SD_SIN8[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x10 : Interrupt State】

Name: INT_STATE
Address: 0x10
Description: This register shows the interrupt state. A result of this register's OR operation is outputted to the INT pin.

INI: Initialization completion
The data 1 is set to this register when the MPU initialization processing is completed. The register address for clearing this register is 0xF0 [0].

CAL: Software calibration completion
The data 1 is set to this register when the calibration executed by a host command is completed. The register address for masking this register is 0xD0 [1], and the address for clearing this register is 0xF0 [1].

RECAL: Re-calibration completion
The data 1 is set to this register when the calibration executed by the error is completed. The register address for masking this register is 0xD0 [2], and the address for clearing this register is 0xF0 [2].

WDT: Watch dog timer (WDT) timeout
The data 1 is set to this register when WDT timeout is detected. IC executes hardware reset and initialization, if WDT interrupt is generated again without clearing WDT. The register address for masking this register is 0xD0 [3], and the address for clearing this register is 0xF0 [3]. Please refer to WDT function on page 31.7

PERCAL: Periodic calibration completion
The data 1 is set to this register when the periodic calibration is completed. The register address for masking this register is 0xD0 [4], and the address for clearing this register is 0xF0 [4].

ONDET: ON detection
The data 1 is set to this register when the OR operation of DETECT_SW_ON (0x13), DETECT_SLIDER_ON (0x15[7]) and DETECT_MAT_ON (0x16[7]) becomes '1'. In order to clear this register, it is necessary to clear each ON detection.

OFFDET: OFF detection
The data 1 is set to this register when the OR operation of DETECT_SW_OFF (0x17), DETECT_SLIDER_OFF (0x19[7]) and DETECT_MAT_OFF (0x1A [7]) becomes '1'. In order to clear this register, it is necessary to clear each OFF detection.

CONTDET: Long press detection
The data 1 is set to this register when the OR operation of DETECT_SW_CONT (0x1B) and DETECT_MAT_CONT (0x1C [7]) becomes '1'. In order to clear this register, it is necessary to clear each long press detection.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	CONTDET	OFFDET	ONDET	PERCAL	WDT	RECAL	CAL	INI
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x11 : Switch ON/OFF State】

Name: SW_STATE
Address: 0x11
Description: This register shows ON or OFF state of simple switch.

1: ON state 0: OFF state

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	SW7_STAT	SW6_STAT	SW5_STAT	SW4_STAT	SW3_STAT	SW2_STAT	SW1_STAT	SW0_STAT
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x13 : Switch ON Detection】

Name: DETECT_SW_ON
Address: 0x13
Description: This register shows that the state of each simple switches changed from OFF to ON. This IC supports multi-simultaneous detection for simple switches and it has a detection result bit for each switch. The data 1 is set to the register ONDET (0x10[5]) when this register becomes to 1. The address for clearing this register is 0xF3.

1: ON-detected 0: ON-undetected

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	SW7_ON	SW6_ON	SW5_ON	SW4_ON	SW3_ON	SW2_ON	SW1_ON	SW0_ON
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x15 : Slider ON Detection】

Name: DETECT_SLIDER_ON
Address: 0x15
Description: This register shows the data when slider ON operation is detected.

SLID_CNT: The quantity of slider movement
This register shows the quantity of slider movement shown in two's complement. This register is updated every detecting slider operation. IC calculates the gravity center position of sensors which detects ON. The quantity of the movement becomes 1 when center gravity position moves to between 2 sensors, and the quantity of the movement becomes 2 when center gravity position moves to the next sensor. The amount of movement detected in order of SIN0→SIN1→SIN2→⋯→ SIN7 is expressed by a positive value, and the amount of the movement detected in a reverse order is expressed by a negative value. The quantity of movement loops when it exceeded this register range. For example, the next of 31(011111b) becomes -32(100000b).

SLID_KEEP: Slider ON-keeping
The data 1 is set to this register while slider operation is detected. This register becomes 0 automatically when slider operation is finished.

SLID_ON: Slider ON-detected
The data 1 is set to this register while slider ON operation is detected. The data 1 is set to the register ONDET (0x10[5]) when this register becomes to 1. The address for clearing this register is 0xF5 [7].

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	SLID _ON	SLID _KEEP	SLID _CNT[5]	SLID _CNT[4]	SLID _CNT[3]	SLID _CNT[2]	SLID _CNT[1]	SLID _CNT[0]]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x16 : Matrix ON Detection】

Name: DETECT_MAT_ON
Address: 0x16
Description: This register shows that the state of each matrix switches changed from OFF to ON. This IC does not support multi-simultaneous detection for the matrix switches.

KEY_ON: Matrix key number that detected ON
This register is a matrix switches number that detected ON. It is impossible to clear this register. This is updated when IC detects matrix switch ON again.

MAT_ON: Matrix Switch ON-detected
The data 1 is set to this register when the state of each matrix switch changed from OFF to ON. The data 1 is set to the register ONDET (0x10[5]) when this register becomes to 1. The address for clearing this register is 0xF6 [7].

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	MAT_ON	-	-	-	KEY_ON[3]	KEY_ON[2]	KEY_ON[1]	KEY_ON[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x17 : Switch OFF Detection】

Name: DETECT_SW_OFF
Address: 0x17
Description: This register shows that the state of each simple switch changed from ON to OFF. This IC supports multi-simultaneous detection for simple switches and it has a detection result bit for each switch. The data 1 is set to the register OFFDET (0x10[6]) when this register becomes to 1. The address for clearing this register is 0xF7.

1: OFF-detected 0: OFF-undetected

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x17	SW7_OFF	SW6_OFF	SW5_OFF	SW4_OFF	SW3_OFF	SW2_OFF	SW1_OFF	SW0_OFF
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x19 : Slider OFF Detection】

Name: DETECT_SLIDER_OFF
Address: 0x19
Description: This register shows the data when slider OFF operation is detected.

SLID_LAST: The final quantity of slider movement
This register shows the amount of final slider movement shown in two's complement. This value corresponds to final SLID_CNT in DETECT_SLIDER_ON (0x19).

SLID_OFF: Slider OFF-detected
The data 1 is set to this register while slider OFF operation is detected. The data 1 is set to the register OFFDET (0x10[5]) when this register becomes to 1. It is necessary to clear this register in order to detect slider OFF operation again. The address for clearing this register is 0xF9 [7].

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19	SLID _OFF	-	SLID _LAST[5]	SLID _LAST[4]	SLID _LAST[3]	SLID _LAST[2]	SLID _LAST[1]	SLID _LAST[0]]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1A : Matrix OFF Detection】

Name: DETECT_MAT_OFF
Address: 0x1A
Description: This register shows that the state of matrix switch changed from ON to OFF. This IC supports multi-simultaneous detection for simple switches.

KEY_OFF: Matrix key number that detected OFF
This register is a matrix switches number that detected OFF. It is impossible to clear this register. This is updated when IC detects matrix switch OFF again.

MAT_OFF: Matrix Switch OFF-detected
The data 1 is set to this register when the state of each matrix switch changed from ON to OFF. The data 1 is set to the register OFFDET (0x10[6]) when this register becomes to 1. The address for clearing this register is 0xFA [7].

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A	MAT_OFF	-	-	-	KEY_OFF[3]	KEY_OFF[2]	KEY_OFF[1]	KEY_OFF[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1B : Switch Long Press Detection】

Name: DETECT_SW_CONT
Address: 0x1B
Description: This register shows that long press of simple switch was detected. This IC supports multi-simultaneous detection for simple switches and it has a detection result bit for each switch. The data 1 is set to this register CONTDET (0x10 [7]) when this register becomes to 1. The address for clearing this register is 0xFB.

1: Long Press detected 0: Long Press undetected

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	SW7_CONT	SW6_CONT	SW5_CONT	SW4_CONT	SW3_CONT	SW2_CONT	SW1_CONT	SW0_CONT
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1C : Matrix Switch Long Press Detection】

Name: DETECT_MAT_CONT
Address: 0x1C
Description: This register shows that long press of matrix switch was detected. This IC supports multi-simultaneous detection for matrix switches.

KEY_CONT: Matrix key number that detected long press
This register is a matrix switches number that detected long press. It is impossible to clear this register. This is updated when IC detects matrix switch long press again.

MAT_CONT: Matrix Switch long press detected
The data 1 is set to this register when IC detected long press. The data 1 is set to the register CONTDET (0x10[7]) when this register becomes to 1. The address for clearing this register is 0xFC [7].

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	MAT _CONT	-	-	-	KEY _CONT[3]	KEY _CONT[2]	KEY _CONT[1]	KEY _CONT[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1D : Control State】

Name: CONTROL_STATE
Address: 0x1D
Description: This register shows IC operating state.

D_CALIB: This register shows whether IC is performing calibration. D_CALIB=1 shows that IC is performing calibration.

INTM: This register shows whether IC works in intermittent operation. INTM=1 shows that IC is in intermittent operation.

E_CALIB: The data 1 is set to this register when the calibration failed in succession three times. It is impossible to clear this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	E_CALIB	-	-	-	-	-	INTM	D_CALIB
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1E : Checking Activity Read Register】

Name: RACT
Address: 0x1E
Description: This register is used to check operation of IC. The data written in WACT (0xFE) is copied to this register. Normal operation of I/F and MPU can be checked by comparing the data written value with the data read.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	RACT[7]	RACT[6]	RACT[5]	RACT[4]	RACT[3]	RACT[2]	RACT[1]	RACT[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x85, 0x8A : Software Reset】

Name: SOFTRESET
Address: 0x85, 0x8A
Description: These registers are for software reset. When the data of register 0x85 become 55h and the data of register 0x8A become AAh, software reset is generated and IC is initialized.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x85	SRST[7]	SRST[6]	SRST[5]	SRST[4]	SRST[3]	SRST[2]	SRST[1]	SRST[0]
0x8A	SRST[15]	SRST[14]	SRST[13]	SRST[12]	SRST[11]	SRST[10]	SRST[9]	SRST[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xB0 : Download Setting】

Name: DLSETTING
Address: 0xB0
Description: This register is used to download MPU program.

OSCEN: Oscillator function

1: enabled 0: disabled

MPUEN: MPU function

MPU is reset when the data of this register is 0. Please set the data 0 to this register at downloading MPU program. MPU boots and start initialization if the data 1 is set to this register after MPU download is completed with a success. MPU do not boot and start initialization even if the data 1 is set to this register after MPU download is completed with a fail.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB0	-	-	-	-	-	-	MPUEN	OSCEN
R/W	R	R	R	R	R	R	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xB2 : Download Circuit Clear】

Name: DLCLR
Address: 0xB2
Description: This register is used to initialize the circuit for program download. Please initialize before starting program download. Initialization starts if the data 1 is set to this register. And the value of this register returns to 0 automatically after initialization.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB2	-	-	-	-	-	-	-	DLCLR
R/W	R	R	R	R	R	R	R	W
Initial val.	0	0	0	0	0	0	0	0

【0xB3 - 0xB6 : Download Data】

Name: DLDAT
Address: 0xB3 - 0xB6
Description: This register is used for MPU program download. The 32-bit data of DLDAT are written in RAM when the data is sent to 0xB6 with OSCEN=1. Please set 1 to OSCEN at download.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB3	DLDAT[7]	DLDAT[6]	DLDAT[5]	DLDAT[4]	DLDAT[3]	DLDAT[2]	DLDAT[1]	DLDAT[0]
0xB4	DLDAT[15]	DLDAT[14]	DLDAT[13]	DLDAT[12]	DLDAT[11]	DLDAT[10]	DLDAT[9]	DLDAT[8]
0xB5	DLDAT[23]	DLDAT[22]	DLDAT[21]	DLDAT[20]	DLDAT[19]	DLDAT[18]	DLDAT[17]	DLDAT[16]
0xB6	DLDAT[31]	DLDAT[30]	DLDAT[29]	DLDAT[28]	DLDAT[27]	DLDAT[26]	DLDAT[25]	DLDAT[24]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xB7 : Download Result】

Name: DLRES
Address: 0xB7
Description: This register shows a download result. When MPU download is completed, IC compares the checksum value calculated from download data with the checksum value attached to 4 bytes of end of download data, and sets the result. The result is cleared by writing 1 to DLCLR (0xB2 [0]).

DL_PASS: Success in program downloading
The data 1 is set to this register when download is successful. If the data 1 is set to this register, MPUEN (0xB0 [1]) is enabled.

DL_FAIL: Failure in program downloading
The data 1 is set to this register when download is failed.

*Program data format
program data: DLDAT[0:8187]
check sum : DLDAT[8188:8191]
check sum : DLDAT[0] + DLDAT[1] + ・・・ + DLDAT[8186] + DLDAT[8187]

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB7	-	-	-	-	DL_FAIL	DL_PASS	-	-
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0xB8 - 0xBA : Download Checksum Data】

Name: CKSUM
Address: 0xB8 - 0xBA
Description: These registers show the checksum value of downloading data. This is updated at the timing when the data of all 8kByte downloaded.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB8	CKSUM[7]	CKSUM[6]	CKSUM[5]	CKSUM[4]	CKSUM[3]	CKSUM[2]	CKSUM[1]	CKSUM[0]
0xB9	CKSUM[15]	CKSUM[14]	CKSUM[13]	CKSUM[12]	CKSUM[11]	CKSUM[10]	CKSUM[9]	CKSUM[8]
0xBA	-	-	CKSUM[21]	CKSUM[20]	CKSUM[19]	CKSUM[18]	CKSUM[17]	CKSUM[16]
R/W	R	R	R	R	R	R	R	R
Initial val	0	0	0	0	0	0	0	0

【0xC0 - 0xC4 : ON Threshold Value and Gain Selection Setting】

Name: SEL_SIN
Address: 0xC0 - 0xC4
Description: These registers are used to set ON threshold value and the gain value.

ON_SIN* : Sensor threshold value selection
These registers show ON threshold value used about each sensor.
0x0 : ON0(0xCA) is used
0x1 : ON1(0xCB) is used
0x2 : ON2(0xCC) is used
0x3 : ON0(0xCA) is used

GA_SIN* : Sensor gain value selection
These registers show gain value used about each sensor.
0x0 : GA0(0xC8) is used
0x1 : GA1(0xC8) is used
0x2 : GA2(0xC9) is used
0x3 : GA0(0xC8) is used

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC0	GA_SIN1[1]	GA_SIN1[0]	ON_SIN1[1]	ON_SIN1[0]	GA_SIN0[1]	GA_SIN0[0]	ON_SIN0[1]	ON_SIN0[0]
0xC1	GA_SIN3[1]	GA_SIN3[0]	ON_SIN3[1]	ON_SIN3[0]	GA_SIN2[1]	GA_SIN2[0]	ON_SIN2[1]	ON_SIN2[0]
0xC2	GA_SIN5[1]	GA_SIN5[0]	ON_SIN5[1]	ON_SIN5[0]	GA_SIN4[1]	GA_SIN4[0]	ON_SIN4[1]	ON_SIN4[0]
0xC3	GA_SIN7[1]	GA_SIN7[0]	ON_SIN7[1]	ON_SIN7[0]	GA_SIN6[1]	GA_SIN6[0]	ON_SIN6[1]	ON_SIN6[0]
0xC4	-	-	-	-	GA_SIN8[1]	GA_SIN8[0]	ON_SIN8[1]	ON_SIN8[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xC8, 0xC9 : Sensor Gain Setting】

Name: GAIN
Address: 0xC8, 0xC9
Description: These registers are used to set sensor gain value. IC has 15 step settings. The smaller the setting is, the larger the sensor gain is. If setting value becomes small, the sensor gain will become large. This IC has three gain settings and it is possible to select gain setting value for each sensor.

The setting range : 0x1 ≤ GA ≤ 0xF

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC8	GA1[3]	GA1[2]	GA1[1]	GA1[0]	GA0[3]	GA0[2]	GA0[1]	GA0[0]
0xC9	-	-	-	-	GA2[3]	GA2[2]	GA2[1]	GA2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xCA - 0xCC : Sensor ON Threshold Setting】

Name: ON_TH
Address: 0xCA - 0xCC
Description: These registers are used to set sensor ON threshold value. IC has 3 ON threshold settings and it is possible to select ON threshold setting value for each sensor.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCA	ON0[7]	ON0[6]	ON0[5]	ON0[4]	ON0[3]	ON0[2]	ON0[1]	ON0[0]
0xCB	ON1[7]	ON1[6]	ON1[5]	ON1[4]	ON1[3]	ON1[2]	ON1[1]	ON1[0]
0xCC	ON2[7]	ON2[6]	ON2[5]	ON2[4]	ON2[3]	ON2[2]	ON2[1]	ON2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xCD : Sensor OFF Threshold Setting】

Name: OFF_TH
Address: 0xCD
Description: These registers are used to set sensor OFF threshold value. When the 8bit ADC value of each sensor (SENS_DATA) is smaller than this setting value, IC judges the sensor changed from OFF to ON.

The setting range : 0x00 ＜ OFF ＜ ON ＜ 0xFF

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCD	-	OFF [6]	OFF [5]	OFF [4]	OFF [3]	OFF [2]	OFF [1]	OFF [0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	-	0	0	0	0	0	0	0

【0xCE :Chattering cancel setting】

Name: OVERSAMPLES
Address: 0xCE
Description: This register is used to set the number of times of oversampling to cancel chattering when the state of sensor changes. If the continuance of the ON or OFF operations is lower than this register value, the operations are ignored. The canceling chattering is disabled when the data 0 is set.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCE	-	-	-	-	CHATTER[3]	CHATTER[2]	CHATTER[1]	CHATTER[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xCF :Long Press setting】

Name: CONTTIMES
Address: 0xCF
Description: This register is used to set long press setting.

CONT: This register is used to select the frequency of the interrupt generated by long press.
Long press is detected when the state of switch ON lasts for the period 6times as large as the register value. Long press is disabled when the data 0 is set to this register.

CONTSEL: This register is used to set settings of the interrupt generated at detecting long press operation.

1: output at every detection 0: output at first detection only.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCF	CONTSEL	-	CONT[5]	CONT[4]	CONT[3]	CONT[2]	CONT[1]	CONT[0]
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	-	0	0	0	0	0	0

【0xD0 : Interrupt State Mask Setting】

Name: MSK_INT_STATE
Address: 0xD0
Description: This register is used to mask the interrupt. Masked interrupt is not reflected in INT_STATE.

1: Interrupt is masked 0: Interrupt is not masked

MSK_CAL: The setting to mask software calibration completion
This register is used to mask CAL (0x10[1]) that the data 1 is set when software calibration is completed.

MSK_RECAL: The setting to mask re-calibration completion
This register is used to mask RECAL (0x10[2]) that the data 1 is set when re-calibration is completed.

MSK_WDT: The setting to mask watch dog timer timeout
This register is used to mask WDT (0x10[3]) that the data 1 is set when WDT timeout occurred.

MSK_PERCAL: The setting to mask periodic calibration completion
This register is used to mask PERCAL (0x10[4]) that the data 1 is set when periodic calibration is completed.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD0	-	-	-	MSK_ PERCAL	MSK_WDT	MSK_RECAL	MSK_CAL	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD1 : Simple Switch Mask Setting】

Name: MSK_SW
Address: 0xD1
Description: This register is used to mask the interrupt generated by simple switches operation. Masked interrupt is not reflected in INT_STATE. Please mask about unused simple switch. Even if it is masked, ON/OFF state of simple switch is detected. Please set EN_SIN (0xE2) in case you would like to stop the ON/OFF detection.

1 :DETECT_SW_ON is masked 0 :DETECT_SW_ON is not masked

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD1	MSK_SW7	MSK_SW6	MSK_SW5	MSK_SW4	MSK_SW3	MSK_SW2	MSK_SW1	MSK_SW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD2, 0xD3 : Matrix Switch Mask Setting】

Name: MSK_MAT
Address: 0xD2, 0xD3
Description: This register is used to mask the interrupt generated by matrix switches operation. Masked interrupt is not reflected in INT_STATE. This IC does not support multi-simultaneous detection for matrix switches. Please mask about unused matrix switches. The unanticipated matrix switch operation may be detected if the unused matrix switches are not masked.

1 :DETECT_MAT_ON is masked 0 :DETECT_MAt_ON is not masked

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD2	MSK_KEY07	MSK_KEY06	MSK_KEY05	MSK_KEY04	MSK_KEY03	MSK_KEY02	MSK_KEY01	MSK_KEY00
0xD3	MSK_KEY15	MSK_KEY14	MSK_KEY13	MSK_KEY12	MSK_KEY11	MSK_KEY10	MSK_KEY09	MSK_KEY08
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD4 : Sensing Setting】

Name: SENS_SETTING
Address: 0xD4
Description: This register is used to set setting about the sensing operation in the intermittent state. It is effective in the intermittent detection mode only.

UNIT_SENS_NUM : The setting about the number of normal sensing between check sensing.
This register is used to set setting for the number of normal sensing performed after check sensing. The normal sensing is performed (setting value + 1) times.For example, IC operates as follows when the setting value is 3.
Check -> Normal -> Normal -> Normal -> Normal -> Check -> Normal -> Normal -> ・・・

KEEP_SENS_NUM : The setting about the number of normal sensing
This register is used to set the period for which normal sensing performs when the change is not detected in check sensing. When the number of times of check sensing from which change was not detected continuously is less than a setting value, the normal sensing is performed regardless of a result of check sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD4	KEEP_SENS_NUM[0]	KEEP_SENS_NUM[0]	KEEP_SENS_NUM[0]	KEEP_SENS_NUM[0]	UNIT_SENS_NUM[3]	UNIT_SENS_NUM[2]	UNIT_SENS_NUM[1]	UNIT_SENS_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD5, 0xD6 : Intermittent Operation Return Threshold Value Setting】

Name: TH_INTERMITTENT
Address: 0xD5, 0xD6
Description: This register is used to set a threshold value to shift from intermittent operation to normal operation. It is effective in the intermittent detection mode only. When the difference value of the result of check sensing and the expected value calculated from the result of normal sensing becomes more than a threshold value, IC returns from intermittent operation.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD5	TH_INTM[15]	TH_INTM[14]	TH_INTM[13]	TH_INTM[12]	TH_INTM[11]	TH_INTM[10]	TH_INTM[9]	TH_INTM[8]
0xD6	TH_INTM[7]	TH_INTM[6]	TH_INTM[5]	TH_INTM[4]	TH_INTM[3]	TH_INTM[2]	TH_INTM[1]	TH_INTM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD7 : Output Offset Setting 】

Name: OUTPUT_OFFSET
Address: 0xD7
Description: This register is set an offset of the sensor value outputted to SD_SIN (0x00 to 0x08). When a calibration is completed, these sensor values turn into a value of the zero neighborhoods. Therefore, when a sensor value downs, 0 always be displayed, and it is impossible to show an exact value. If offset is added, it is possible to read the downed value, and to check an exact value. The Offset does not affect ON and OFF detection of switches.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD7	OUTPUT_OFFSET[7]	OUTPUT_OFFSET[6]	OUTPUT_OFFSET[5]	OUTPUT_OFFSET[4]	OUTPUT_OFFSET[3]	OUTPUT_OFFSET[2]	OUTPUT_OFFSET[1]	OUTPUT_OFFSET[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDF : Slider Setting】

Name: EN_SLIDER
Address: 0xDF
Description: This register is used to enable sensors of slider function. The function is enabled when the data 1 is set to this register. The order is SIN0, 1, 2, 3, 4, 5, 6, and 7, and the disabled sensor is skipped. For example, when only SIN1, 2, 5, and 6 are enabled, the order is SIN1, 2, 5, 6. Moreover, when SLIDER_LOOP (0xE0 [2]) is enabled, SIN7 and SIN0 are set as a consecutive sensor. When touch is detected in any of the enabled sensors in intermittent mode, all enabled sensors start sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDF	EN_SLID_SIN7	EN_SLID_SIN6	EN_SLID_SIN5	EN_SLID_SIN4	EN_SLID_SIN3	EN_SLID_SIN2	EN_SLID_SIN1	EN_SLID_SIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE0 : MODE SETTING 0】

Name: MODE_SETTING 0
Address: 0xE0
Description: This register is used to set the mode of operation.

DET_MOD: Detection mode setting
It is possible to select the mode in which the IC operates.

1: Intermittent sensing 0: Nomarl sensing

EN_DSLP: Deep Sleep function setting
This register is used to set deep sleep function. When this function is enabled and main clock is unnecessary, IC suspends a main clock and reduces actuating current.

1: Deep sleep is enabled 0: Deep sleep is disableb

SLID_LOOP: Slider loop function setting
2 Sensors of the edge are recognized as a consecutive sensor like SIN6->SIN7->SIN0 and SIN1 ->SIN0 ->SIN7.

1: Slider loop is enabled 0: Slider loop is disabled

FIX_SENS_CYC: Sensing frequency fixed setting
This register is used to set the function changing sensing frequency every sensing for noise protection. When this function is enabled, the sensing frequency changes every sensing.

1: fixed frequency 0: modulated frequency

FIX_BASE_CYC: Base Frequency fixed setting
This register is used to set the function changing sensing frequency at the failure of calibration and the execution of return calibration. When this function is enabled, the sensing frequency changes at the failure of calibration and the execution of return calibration.

1: fixed frequency 0: modulated frequency

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	-	-	FIX_BASE_CYC	FIX_SENS_CYC	-	SLID_LOOP	EN_DSLP	DET_MOD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE1 : Operation mode setting1】

Name: MODE_SETTING1
Address: 0xE1
Description: This register is used to set the mode of operation.

DIRFT_DIS: Drift calibration setting
This register is used to enable drift calibration.

1: Drift calibration is disabled 0: Drift calibration is enabled

ERROR_DIS: Calib-error calibration setting
This register is used to enable Calib-error calibration.

1: Calib-error calibration is disabled 0: Calib-error calibration is enabled

HOPPING_DIS: Hopping calibration setting
This register is used to enable hopping calibration.

1: Hopping calibration is disabled 0: Hopping calibration is enabled

RETURN_DIS: Return calibration setting
This register is used to enable return calibration.

1: Return calibration is disabled 0: Return calibration is enabled

RERCAL_DIS: Periodic calibration setting
This register is used to enable periodic calibration.

1: Periodic calibration is disabled 0: Periodic calibration is enabled

MEDIAN_DIS: Median filter setting
This register is used to enable median filter. Please refer to page34 about median filter.

1: Median filter is disabled 0: Median filter is enabled

DIS_EN8: SIN8 setting for noise detection
This register is used to enable SIN8 for detecting noise.

1: SIN8 is disabled 0 : SIN8 is enabled

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE1	DIS_SIN8	-	MEDIAN_DIS	RERCAL_DIS	RETURN_DIS	HOPPING_DIS	ERROR_DIS	DRIFT_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE2 : Enable Sensor Setting】

Name: EN_SIN
Address: 0xE2
Description: This register is used to enable sensors. Sensing and judging is performed when the data 1 is set this register. It is possible to reduce current consumption by disabling unused sensors.

1: Sensor is enabled 0: Sensor is disabled

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE2	EN_SIN7	EN_SIN6	EN_SIN5	EN_SIN4	EN_SIN3	EN_SIN2	EN_SIN1	EN_SIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE3 : Normal Sensing Data Comparison Number Setting】

Name: SENS_NUM
Address: 0xE3
Description: This register is used to set the number of data compared for each sensor at normal sensing. If the setting value is increased, the accuracy rises but sensing time and current consumption increase. Please set 50 (32h) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE3	SENS_NUM[7]	SENS_NUM[6]	SENS_NUM[5]	SENS_NUM[4]	SENS_NUM[3]	SENS_NUM[2]	SENS_NUM[1]	SENS_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE4 : Normal Sensing Read Time Setting】

Name: SENS_RD_TIME
Address: 0xE4
Description: This register is used to set the read time at normal sensing. If a setting value is increased, sensing time becomes long. Please set 5 (05h) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE4	SENS_RD_ TIME[7]	SENS_RD_ TIME[6]	SENS_RD_ TIME[5]	SENS_RD_ TIME[4]	SENS_RD_ TIME[3]	SENS_RD_ TIME[2]	SENS_RD_ TIME[1]	SENS_RD_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE5 : Normal Sensing Reset Time Setting】

Name: SENS_RST_TIME
Address: 0xE5
Description: This register is used to the reset time at normal sensing. If a setting value is increased, sensing time becomes long. Please set 12 (0Ch) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE5	SENS_RST_ TIME[7]	SENS_RST_ TIME[6]	SENS_RST_ TIME[5]	SENS_RST_ TIME[4]	SENS_RST_ TIME[3]	SENS_RST_ TIME[2]	SENS_RST_ TIME[1]	SENS_RST_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE6 : Normal Sensing Initial Reset Time Setting】

Name: SENS_IRST_TIME
Address: 0xE6
Description: This register is used to the initial reset time at normal sensing. If a setting value is increased, sensing time becomes long. Please set 12 (0Ch) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE6	SENS_IRST_ TIME[7]	SENS_IRST_ TIME[6]	SENS_IRST_ TIME[5]	SENS_IRST_ TIME[4]	SENS_IRST_ TIME[3]	SENS_IRST_ TIME[2]	SENS_IRST_ TIME[1]	SENS_IRST_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE7 : Check Sensing Data Comparison Number Setting】

Name: CHK_NUM
Address: 0xE7
Description: This register is used to set the number of data compared for each sensor at check sensing. If the setting value is increased, the accuracy rises but sensing time and current consumption increase. Please set 5 (05h) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE7	CHK_NUM[7]	CHK_NUM[6]	CHK_NUM[5]	CHK_NUM[4]	CHK_NUM[3]	CHK_NUM[2]	CHK_NUM[1]	CHK_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE8 : Check Sensing Read Time Setting】

Name: CHK_RD_TIME
Address: 0xE8
Description: This register is used to set the read time at check sensing. If a setting value is increased, sensing time becomes long. Please set 5 (05h) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE8	CHK_RD_ TIME[7]	CHK_RD_ TIME[6]	CHK_RD_ TIME[5]	CHK_RD_ TIME[4]	CHK_RD_ TIME[3]	CHK_RD_ TIME[2]	CHK_RD_ TIME[1]	CHK_RD_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE9 : Check Sensing Reset Time Setting】

Name: CHK_RST_TIME
Address: 0xE9
Description: This register is used to the reset time at check sensing. If a setting value is increased, sensing time becomes long. Please set 12 (0Ch) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE9	CHK_RST_ TIME[7]	CHK_RST_ TIME[6]	CHK_RST_ TIME[5]	CHK_RST_ TIME[4]	CHK_RST_ TIME[3]	CHK_RST_ TIME[2]	CHK_RST_ TIME[1]	CHK_RST_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEA : Check Sensing Initial Reset Time Setting】

Name: CHK_IRST_TIME
Address: 0xEA
Description: This register is used to the initial reset time at check sensing. If a setting value is increased, sensing time becomes long. Please set 12 (0Ch) to this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEA	CHK_IRST_ TIME[7]	CHK_IRST_ TIME[6]	CHK_IRST_ TIME[5]	CHK_IRST_ TIME[4]	CHK_IRST_ TIME[3]	CHK_IRST_ TIME[2]	CHK_IRST_ TIME[1]	CHK_IRST_ TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEB : Digital Gain Setting】

Name: DIG_GAIN
Address: 0xEB
Description: This register is used to set the number of bits which shifts 16-bit A/D converted result to the right. It is possible to adjust the amount of change of a sensor value by changing the number of bits shifted to the right.

SENS_DIG_GAIN: Normal sensing digital gain setting
This register is used to set the number of bits which shifts A/D converted result of normal sensing to the right.

CHK_DIG_GAIN: Check sensing digital gain setting
This register is used to set the number of bits which shifts A/D converted result of check sensing and calibration sensing to the right.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEB	CHK_DIG _GAIN[3]	CHK_DIG _GAIN[2]	CHK_DIG _GAIN[1]	CHK_DIG _GAIN[0]	SENS_DIG_ GAIN[3]	SENS_DIG_ GAIN[2]	SENS_DIG_ GAIN[1]	SENS_DIG _GAIN[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEC : Check Sensing Waiting Time Setting】

Name: CHK_WAIT_TIME
Address: 0xEC
Description: This register is used to set the waiting time to the next check sensing in intermittent operation. It is effective in the intermittent detection mode only. In normal operation, the interval of check sensing is determined by setting of UNIT_SENS_NUM (0xD4) and SENS_WAIT_TIME (0xED). Please refer to Operational control function on page 7 and 33 for detail of it.

Check sensing waiting time = (setting value + 1) x 4 [ms]

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEC	CHK_WAIT TIME[7]	CHK_WAIT TIME[6]	CHK_WAIT TIME[5]	CHK_WAIT TIME[4]	CHK_WAIT TIME[3]	CHK_WAIT TIME[2]	CHK_WAIT TIME[1]	CHK_WAIT TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xED : Normal Sensing Waiting Time Setting】

Name: SENS_WAIT_TIME
Address: 0xED
Description: This register is used to set the waiting time to the next normal sensing in normal operation.
If the setting value is 0, the next sensing is started without waiting time after MPU operation is finished.

Normal sensing waiting time = (setting value + 1) x 4 [ms]

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xED	SENS_WAIT _TIME[7]	SENS_WAIT _TIME[6]	SENS_WAIT _TIME[5]	SENS_WAIT _TIME[4]	SENS_WAIT _TIME[3]	SENS_WAIT _TIME[2]	SENS_WAIT _TIME[1]	SENS_WAIT _TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEE : Calibration Setting 0】

Name: CALIB_SETTING_0
Address: 0xEE
Description: This register is used to set the conditions of performing return calibration. Please refer to on page 38.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEE	RET_NUM[7]	RET_NUM[6]	RET_NUM[5]	RET_NUM[4]	RET_NUM[3]	RET_NUM[2]	RET_NUM[1]	RET_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEF : Calibration Setting 1】

Name: CALIB_SETTING1
Address: 0xEF
Description: This register is used to set the calibration setting.

DRIFT_SIN_NUM : The number of sensors for detecting drift
The drift calibration is executed when the drift is detected more than this register value.

PERCAL_PERIOD : The interval of periodic calibration
The periodic calibration is performed when either of the next conditions is filled.

Normal sensing mode is enabled and (setting value +1) x 500 >= the number of sensing
Intermittent sensing mode and (setting value +1) x 50 >= the number of check sensing

The number of sensing is reset to '0' at calibration.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEF	PRECAL_ PERIOD [3]	PRECAL_ PERIOD [2]	PRECAL_ PERIOD [1]	PRECAL_ PERIOD [0]	DRIFT_SIN **_NUM[3]**	DRIFT_SIN **_NUM[2]-**	DRIFT_SIN **_NUM[1]-**	DRIFT_SIN **_NUM[0]-**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF0 : Interrupt State Clear】

Name: CLR_INT_STATE
Address: 0xF0
Description: When the data 0 is set this register, the interrupt corresponding to this register is cleared. When it is set to 1, the interrupt corresponding to this register isn't cleared.

C_INI: Clearing initialization completion
When the data 0 is set this register, INI (0x10[0]) is cleared.

C_CAL: Clearing software calibration completion
When the data 0 is set this register, CAL (0x10[1]) is cleared.

C_RECAL: Clearing re-calibration completion
When the data 0 is set this register, RECAL (0x10[2]) is cleared.

C_WDT: Clearing watch dog timer timeout
When the data 0 is set this register, WDT (0x10[3]) is cleared.

C_PERCAL: Clearing periodic calibration completion
When the data 0 is set this register, RECAL (0x10[4]) is cleared.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF0	-	-	-	C_PERCAL	C_WDT	C_RECAL	C_CAL	C_INI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF3 : Switch ON Detection Clear】

Name: CLR_SW_ON
Address: 0xF3
Description: When the data 0 is set this register, the register DETECT_SW_ON (0x13) is cleared. This IC supports multi-simultaneous detection for simple switches and it has bit to clear for each switch.

1: SW_ON is not cleared 0: SW_ON is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF3	C_SW7_ON	C_SW6_ON	C_SW5_ON	C_SW4_ON	C_SW3_ON	C_SW2_ON	C_SW1_ON	C_SW0_ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF5 : Slider ON Detection Clear】

Name: CLR_SLIDER_ON
Address: 0xF5
Description: When the data 0 is set this register, the register SLID_ON (0x15 [7]) is cleared.

1: SLID_ON is not cleared 0: SLID_ON is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF5	C_SLID_ON	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF6 : Matrix ON Detection Clear】

Name: CLR_MAT_ON
Address: 0xF6
Description: When the data 0 is set this register, the register C_MAT_ON (0x16 [7]) is cleared.

1: MAT_ON is not cleared 0: MAT_ON is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF6	C_MAT_ON	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF7 : Switch OFF Detection Clear】

Name: CLR_SW_OFF
Address: 0xF7
Description: When the data 0 is set this register, the register DETECT_SW_OFF (0x17) is cleared. This IC supports multi-simultaneous detection for simple switches and it has the bit to clear for each switch.

1: SW_ON is not cleared 0: SW_ON is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF7	C_SW7_OFF	C_SW6_OFF	C_SW5_OFF	C_SW4_OFF	C_SW3_OFF	C_SW2_OFF	C_SW1_OFF	C_SW0_OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF9 : Slider OFF Detection Clear】

Name: CLR_SLIDER_OFF
Address: 0xF9
Description: When the data 0 is set this register, the register SLID_OFF (0x19 [7]) is cleared.

1: SLID_OFF is not cleared 0: SLID_OFF is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF9	C_SLID_OFF	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFA : Matrix OFF Detection Clear】

Name: CLR_MAT_OFF
Address: 0xFA
Description: When the data 0 is set this register, the register MAT_OFF (0x1A [7]) is cleared.

1: MAT_OFF is not cleared 0: MAT_OFF is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFA	C_MAT_OFF	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFB : Long Press Detection Clear】

Name: CLR_SW_CONT
Address: 0xFB
Description: When the data 0 is set this register, the register DETECT_SW_CONT (0x1B) is cleared. This IC supports multi-simultaneous detection for simple switches and it has the bit to clear for each switch.

1: SW_CONT is not cleared 0: SW_CONT is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFB	C_SW7_CONT	C_SW6_CONT	C_SW5_CONT	C_SW4_CONT	C_SW3_CONT	C_SW2_CONT	C_SW1_CONT	C_SW0_CONT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFC : Matrix Long Press Detection Clear】

Name: CLR_MAT_CONT
Address: 0xFC
Description: When the data 0 is set this register, the register MAT_CONT (0x1C [7]) is cleared.

1: MAT_CONT is not cleared 0: MAT_CONT is cleared

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFC	C_MAT_CONT	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFE : Checking Activity Write Register】

Name: WACT
Address: 0xFE
Description: This register is used to check operation of IC. The data written in this register is copied to the register RACT (0x1E). Normal operation of I/F and MPU can be checked by comparing the data written value with the data read.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFE	WACT[7]	WACT[6]	WACT[5]	WACT[4]	WACT[3]	WACT[2]	WACT[1]	WACT[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFF : Sensing Control】

Name: CONTROL
Address: 0xFF
Description: This is used to control sensor operations.

ACT: Operation mode setting
This register is used to set operation mode.

1: Detection mode 0: Stop mode

CALIB: Software Calibration
Software calibration is performed by setting 1 in both this bit and ACT (0xFF [0]). And it is possible to choose calibration mode by CALMOD (0xFF [4]). When this command is received during calibration execution, the calibration is continued and the command is cancel.

CFG: Setting Update
The setting values from the register 0xC0 to 0xEF are reflected by setting 1 in this register. Please set 1 to this register for setting reflection after changing register settings.

CALMOD: Calibration mode setting

0: Calibration is performed with all of enabled sensors.
1: Calibration is performed with sensors that are judged as OFF.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFF	-	-	-	CALMOD	-	CFG	CALIB	ACT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

Timing Chart

Detection cycle

In the detection mode, sensing of each sensor is performed to order. After all the sensor detection finishes, the sensing results is processed in MPU. A detection cycle becomes about 8 ms when all sensors are enabled and the data 0 is set to the register SENS_WAIT_TIME (0xED).

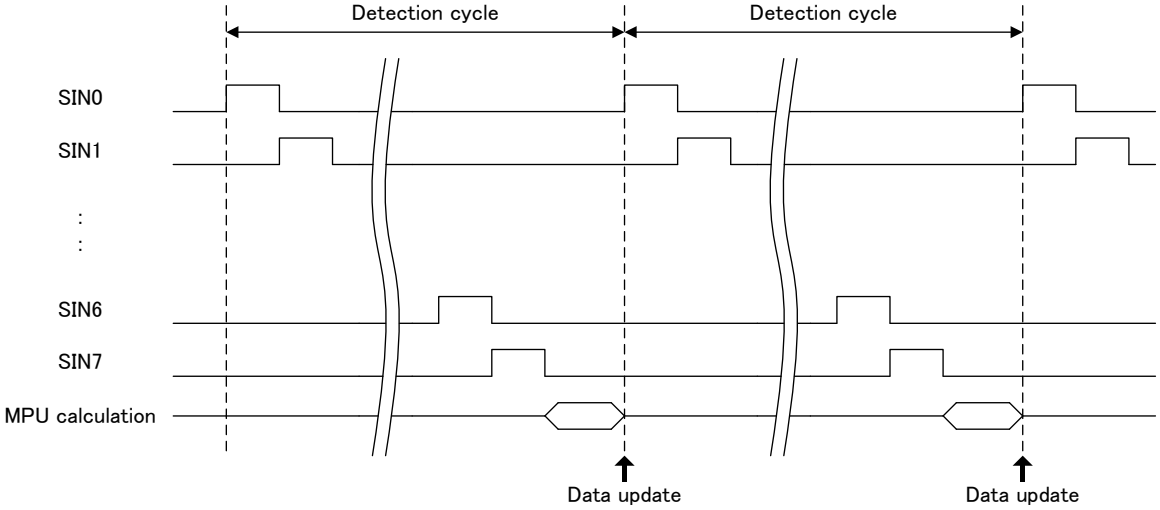


Figure 10. Detection Cycle Timing Chart

Power on Sequence

The power supply pin is only VDD. AVDD and DVDD are generated by built-in LDO regulator, it is not necessary to supply from external. LDO regulator boots and DVDD voltage is raised hen the voltage level of RSTB changes form low to high after power was supplied. And built-in power on reset (POR) circuit is turned off and it is possible to access by host interface after DVDD voltage reached the normal voltage range. It is possible to use with connecting RSTB and VDD because this IC has POR circuit. In this case, POR circuit is turned off automatically after VDD is supplied.

Recommended Value of External Capacitors

C_1	1.0uF	Decoupling capacitor for VDD
C_2	1.0uF	Decoupling capacitor for DVDD
C_3	2.2uF	Decoupling capacitor for AVDD

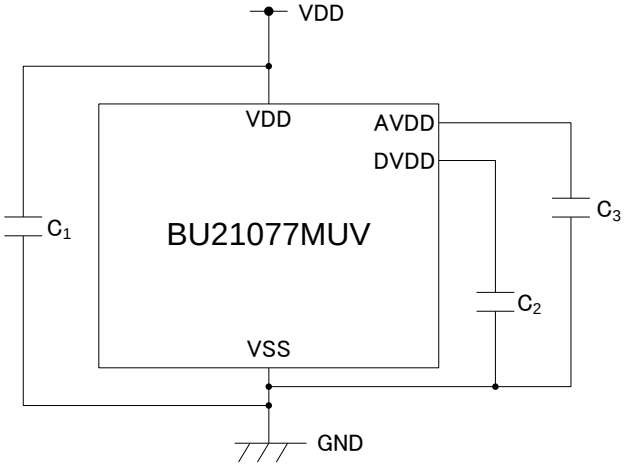


Figure 11. Placement of External Capacitors

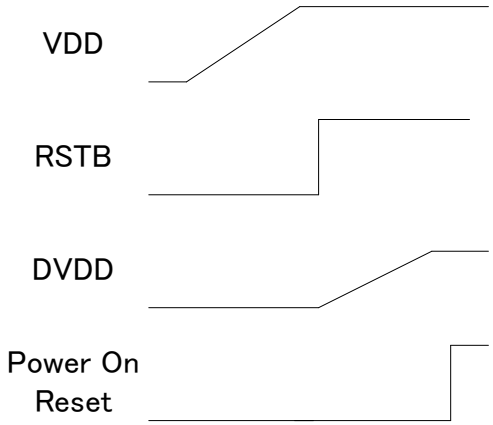


Figure 12. Power on Sequence (Controlled RSTB)

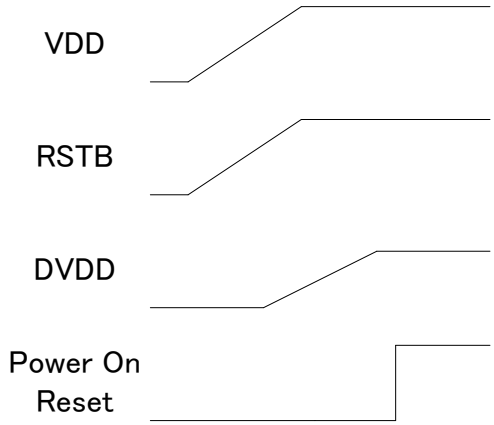


Figure 13. Power on Sequence (VDD-Shorted RSTB)

Function explanation

Software reset function

Software reset is the function which resets IC by host access. If both the value of register 0x85 become 55h and the value of register 0x8A become AAh, software reset is generated and IC is initialized. Reset timing is a rise edge of SCL on ACK timing. ACK response is performed at different timing from usual because a host interface control circuit is also reset. Please note that wrong communication may be recognized depending on a host interface. Figure 14 shows a waveform at the time of reset by writing AAh to the register 0x8A.

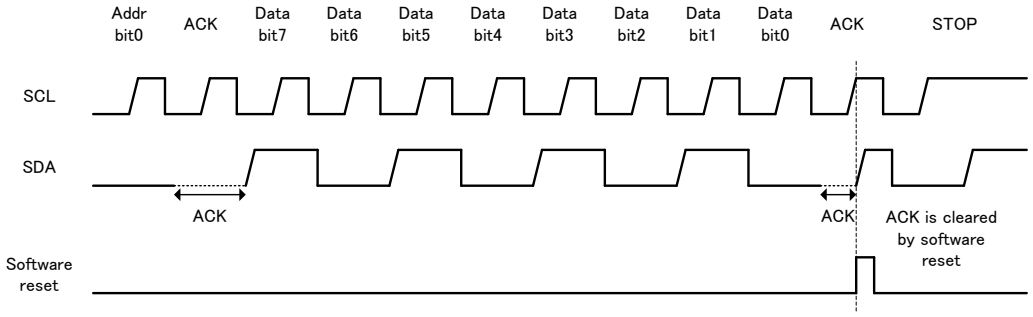


Figure 14. Software Reset Timing

WDT function

A Watchdog timer (WDT) is the function for checking normal operation of MPU. WDT is a simple counter. If WDT becomes enabled, a count starts. If a counter overflows, a WDT interrupt (0x10[3]) is generated. When the WDT interrupt has already occurred at this time, IC is reset and is initialized. When operation of MPU is normal, MPU resets a counter periodically so that a counter may not overflow. When operation of MPU is abnormal, since MPU does not reset a counter, a counter overflows. The WDT interrupt is generated at this time, so it is possible to detect abnormal operation. However, it is only in the detection mode that this IC resets a counter periodically. Therefore, when IC is operated with deep sleep mode (0xE0 [1] = 1) and detection stop mode (0xFF [0] =0), a WDT interrupt is generated.

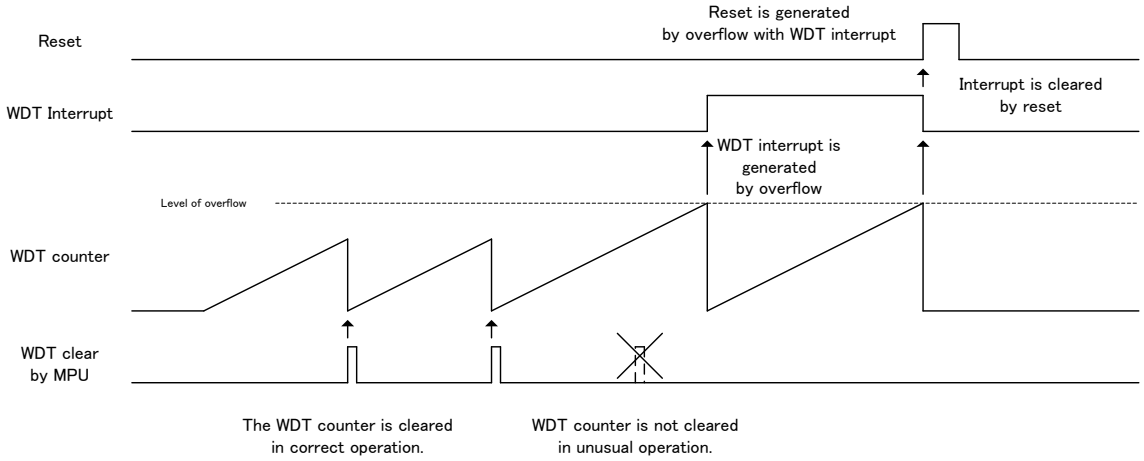


Figure 15. WDT Operation

Operational control function

This IC has two operational modes, a stop and detection. These two operational modes are controlled by the register ACT (0xFF [0]). When the data 0 is set to this register, it operates with stop mode. When the data 1 is set to this register, it operates with detection mode. Furthermore, the detection mode has the two modes, continuous detection mode and intermittent detection mode, and it is set by register DET_MOD (0xE0 [0]). In continuous detection mode, IC always performs sensing and normal sensing. In intermittent detection mode, IC performs normal operation and intermittent operation appropriately depending on the results of sensing.

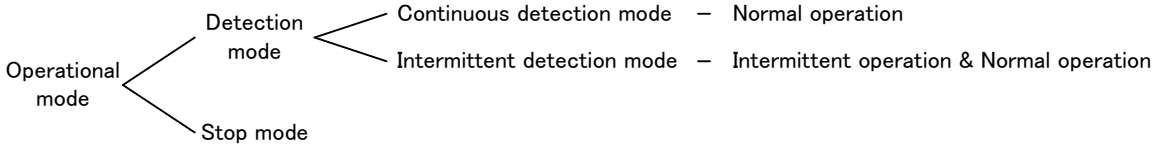


Figure 16. Image of Operation Mode

Continuous detection mode sequence

Step 1. IC performs normal sensing with enabled sensors.
Step 2. IC calculates using sensing results and updates the sensor data.
Step 3. IC waits for normal sensing waiting time (0xED).
Step 4. IC repeats Step1 – Step3.

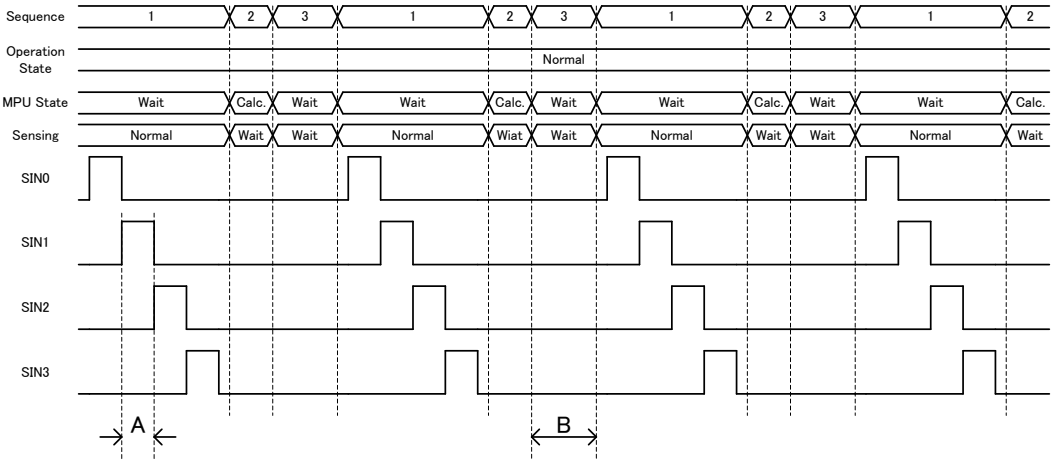


Figure 17. Image of Continuous detection mode sequence

Intermittent detection mode sequence

Step 1. IC performs check sensing with enabled sensors.
Step 2. If the change of sensor data in the results of check sensing is found, IC moves to Step 3, otherwise, IC waits for check sensing waiting time (0xEC) and returns to Step 1.
Step 3. IC performs normal sensing about the sensor that the change was detected.
Step 4. IC calculates using sensing results and updates the sensor data.
Step 5. IC waits for a fixed period on the number of sensors that change was not detected.
Step 6. IC waits for normal sensing waiting time (0xED).
Step 7. IC performs normal sensing depending on UNIT_SENS_NUM (0xD4). If the number of times of normal sensing is performed for setting times, IC returns to step1.

The operation of the Step 1 and Step 2 is defined as intermittent operation. And the operation after step 3 is defined as normal operation.

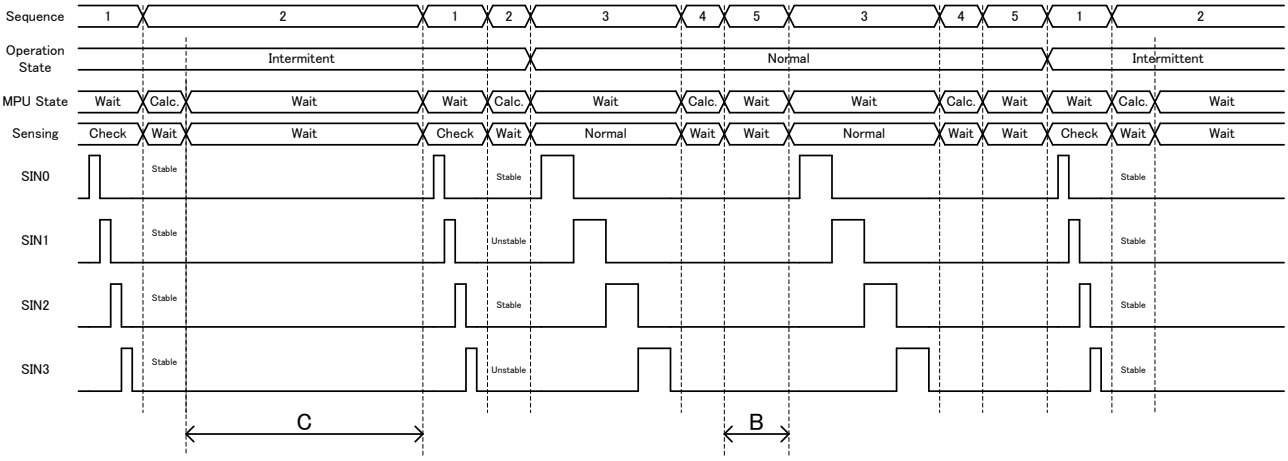


Figure 18. Image of Intermittent Detection Mode Sequence

A: Sensing period of each sensor.
B: Normal sensing waiting period. It is set in register SENS_WAIT_TIME (0xED). (About 0 to 1020 ms)
C: Check sensing waiting period. It is set in register CHK_WAIT_TIME (0xEC). (About 4 to 1024 ms)
D: Normal sensing waiting period for the sensor that change is not detected.

Noise protection function

In order to reduce the influence of a noise which synchronizes with a sampling frequency, IC uses combining a frequency hopping function and a median filter function.

Frequency hopping function

It is the function to prevent a sampling frequency period and a noise frequency from synchronizing by changing a sampling frequency. Five kinds of sampling frequency (A, B, C, D, and E in the following figure) are prepared for frequency hopping, and IC changes a sampling frequency every sensing. It is possible to disable the function by setting 1 to the register FIX_SENS_CYC (0xE0 [4]).

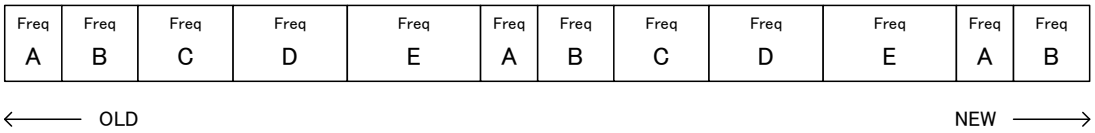


Figure 19. Image of Frequency Hopping Function

Median filter function

It is the function to stabilize data. Median filter is the filter which selects the center value from multiple data. IC processes five data (the newest and the past 4 times of A/D conversion results). Unlike a simple moving average, there is an advantage such as not being affected by abnormal data and such as not missing the edge data. However, this function delays the response to use the median of five data. It is possible to disable the function by setting 1 to the register MEDIAN_DIS (0xE1 [5]).

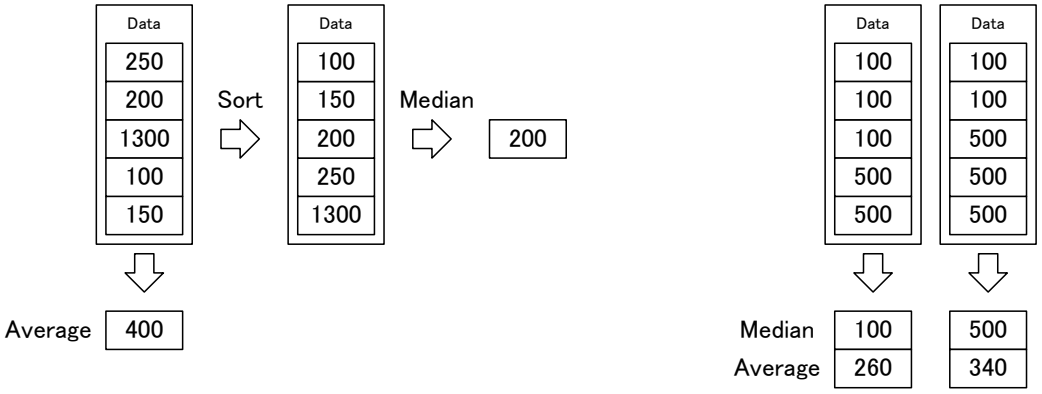


Figure 20. Image of Median Filter Function

IC operates with making the number of sampling for the hopping function and the number of the data used for median filter same. Therefore, the difference in the sampling result by hopping frequency is canceled completely.

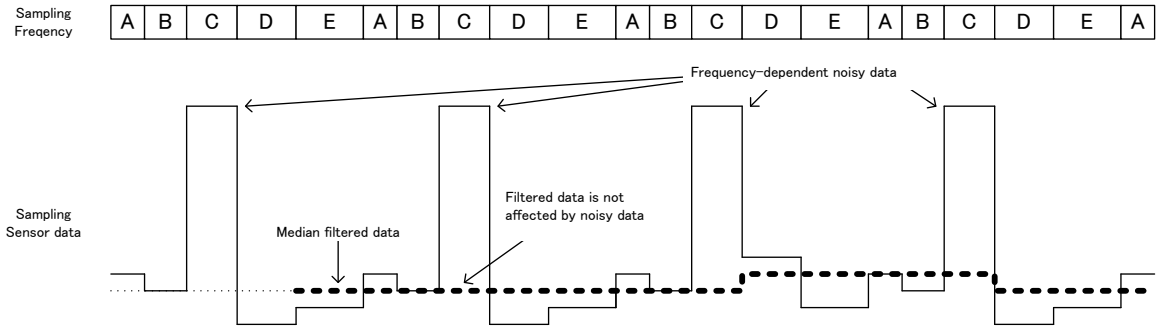


Figure 21. Image of Noise Protection Function

Simple switch function

When a sensor is touched, sensor value increases. When the sensor is left, sensor value decreases. ON/OFF recognition of simple switch is executed by using this change. The simple switch supports multi-simultaneous detection and it is possible to use as 8 simple switches.

Simple switch function

The following judgments are performed by every each sensor, and a value is set to in a corresponding bit of the register. IC performs calibration and set a reference value to perform ON, OFF judgment. It is judged as ON when a sensor level is larger than the value that increased the ON threshold to reference value. Then the state turns ON from OFF and the data 1 is set to the corresponding bit in the register SW_STATE (0x11) and the data 1 is set to the correspondence bit in the register DETECT_SW_ON (0x13). It is judged as OFF when a sensor level is less than the value that increased the OFF threshold to reference value. Then the state turns OFF from ON and the data 0 is set to the corresponding bit in the register SW_STATE (0x11) and the data 1 is set to the corresponding bit in the register DETECT_SW_OFF (0x17).

It is difficult to judge ON and OFF if the interrupt is generated before the register DETECT_SW_ON and DETECT_SW_OFF are cleared. Please clear an interrupt factor and judge the state of the switch. It is possible to set ON threshold and OFF threshold independently.

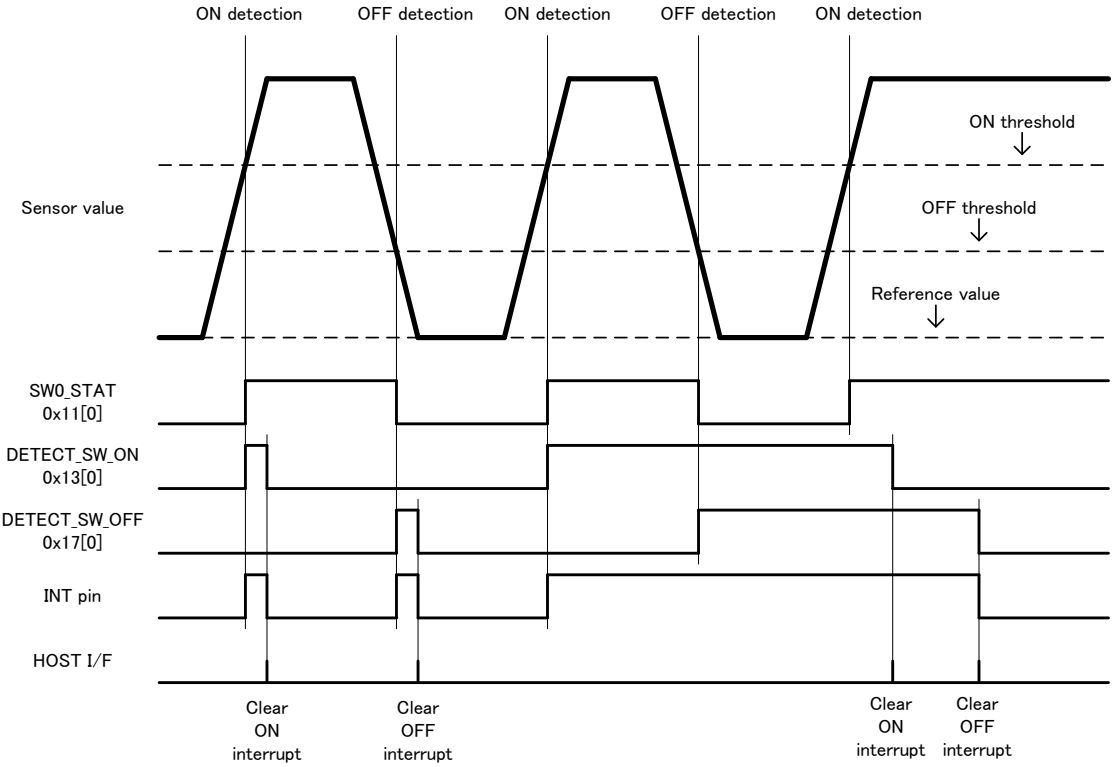


Figure 22. Simple switch function

Chattering cancel function

IC considers it to be a chattering state until constant number of times continues with ON and OFF state. IC doesn't reflect the judgment result on register while chattering state. IC reflects the judgment result when constant number of times continues with same ON and OFF state. It is possible to set constant number of times in CHATTERING (0xDE [3:0]).

If the function is enabled, short ON and OFF less than set value are not detected. But the response becomes slower.

We show the schematic chart in Figure23 in case of setting CHATTERING '2'. IC reflects the judgment result on register when three times of same judgment continues in case of setting CHATTERING '2'.

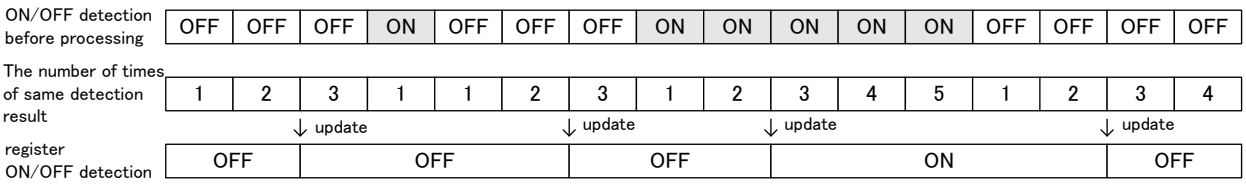


Figure 23.Chattering cancel function (CHATTERING=2)

Slider function

This is the function to convert the change of the center of gravity position of the sensor with ON state into quantity of movement and output when sensor pin SIN0-7 is arranged to be next to each other. It is possible to select the sensor to be used for slider and to get the large amount of movement by placing as figure 24. The result of simple switch with chattering cancel function is used for slider judgment.

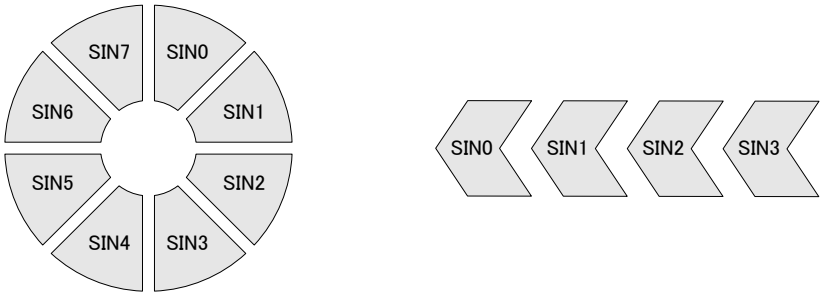


Figure 24. Arrangement for sliders

Slider

The order of the sensor becomes SIN7 from SIN0. It is possible to recognize SIN0 and SIN7 as sensors to be next to each other by enabling register SLID_LOOP (0xE0 [2]). It is possible to disable the sensors to be used for slider function by setting register EN_SLIDER (0xDF). IC recognizes as slider off when the state of sensors more than 4 sensors or the state of separated sensors are ON. IC calculates the center of gravity position of the sensor and if IC detects the quantity of movement over than 1, IC judges as slider and sets 1 to the register SLID_ON (0x15[7]) and SLID_KEEP (0x15[6]). IC recognizes the movement like SIN0→SIN1→SIN2→…→SIN7 as a plus slider and the movement like SIN7→SIN6→SIN5→…→SIN0 as a minus slider. SLIDER_CNT is incremented by 1 when the gravity center position moves by plus 0.5. SLIDER_CNT is decremented by 1 when the gravity center position moves by minus 0.5. The slider recognition is finished when all sensors are OFF or the amount of movement for one sampling is over than 2. When the slider is finished, the data 1 is set to the register SLID_OFF (0x19 [7]) and the final quantity of movement is set to SLID_LAST (0x19 [5:0]) and the register SLID_KEEP (0x15 [6]) ON become to 0. IC does not detect sliders while SLID_OFF (0x19 [7]) is 1. Please clear the register SLIDER_OFF to detect next sliders. It is cleared by setting 0 to the register C_SLID_OFF (0xF9 [7]).

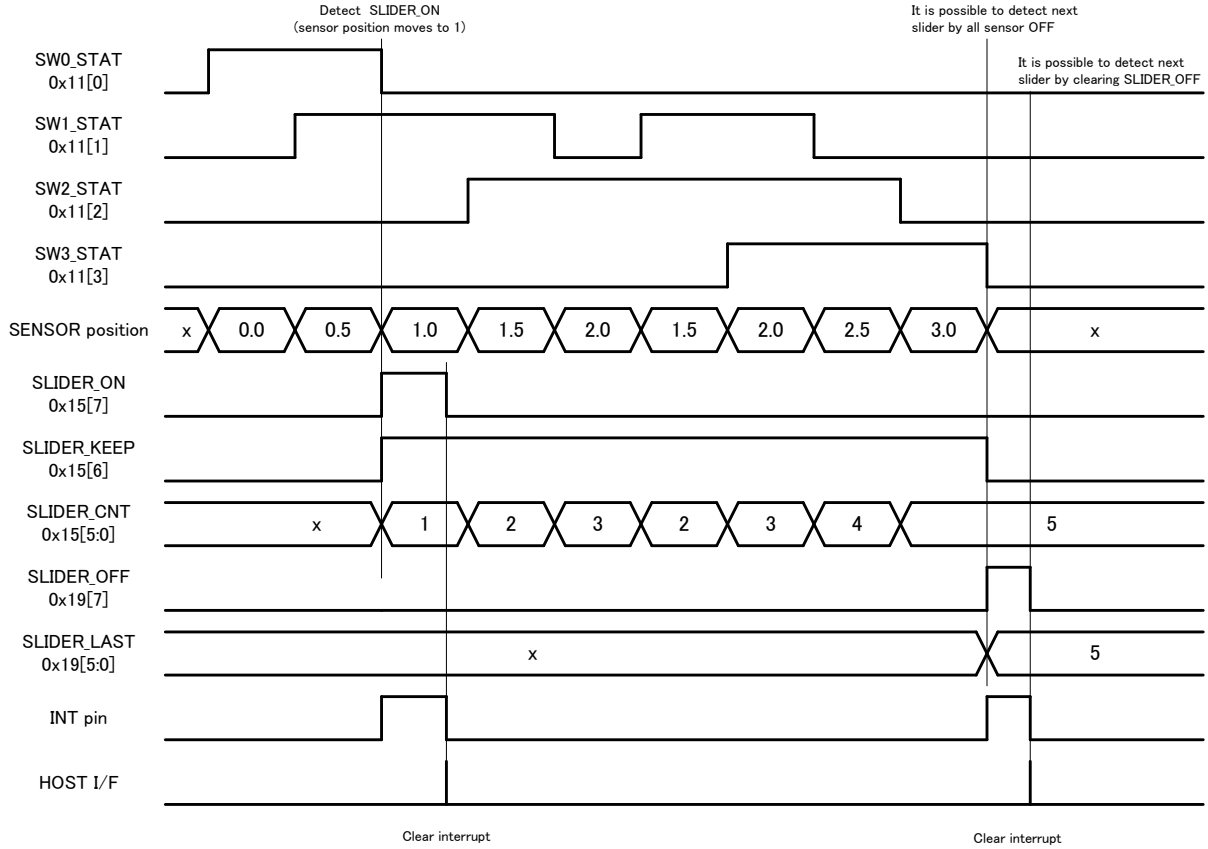


Figure 25. Slider function

Matrix Switch

It is possible to use cross point as key switch by arranging sensor pins as matrix. It is possible to use 16 key switches. 16 keys from KEY00 to KEY15 are assigned to each cross point as Figure 26. IC doesn't support simultaneous push of matrix switch. Please set mask in order to avoid false detection in case there are unused sensors. It is possible to set mask by the register MSK_MAT (0xD2, 0xD3). The result of simple switch with chattering cancel function is used for matrix switch judgment.

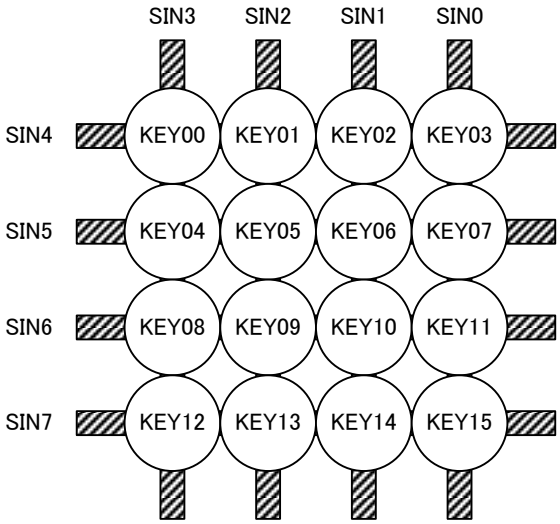


Figure 26. Arrangement for matrix switch

Matrix Switch

The data 1 is set to the register MAT_ON (0x16 [7]) and KEY_ON (0x16 [3:0]) when IC detects ON of key switch. IC detects only OFF or long press of key switch after having detected ON of key switch. The date 1 is set to the register DETECT_MAT_OFF (0x1A) when IC detects OFF of key switch. The date 1 is set to the register DETECT_MAT_CONT (0x1C) when IC detects long press of key switch. Please clear the register DETECT_MAT_ON and DETECT_MAT_OFF to detect the next state of key switch. They are cleared by setting "0" to the register CLR_MAT_ON (0xF6) and CLR_MAT_OFF (0xFA).

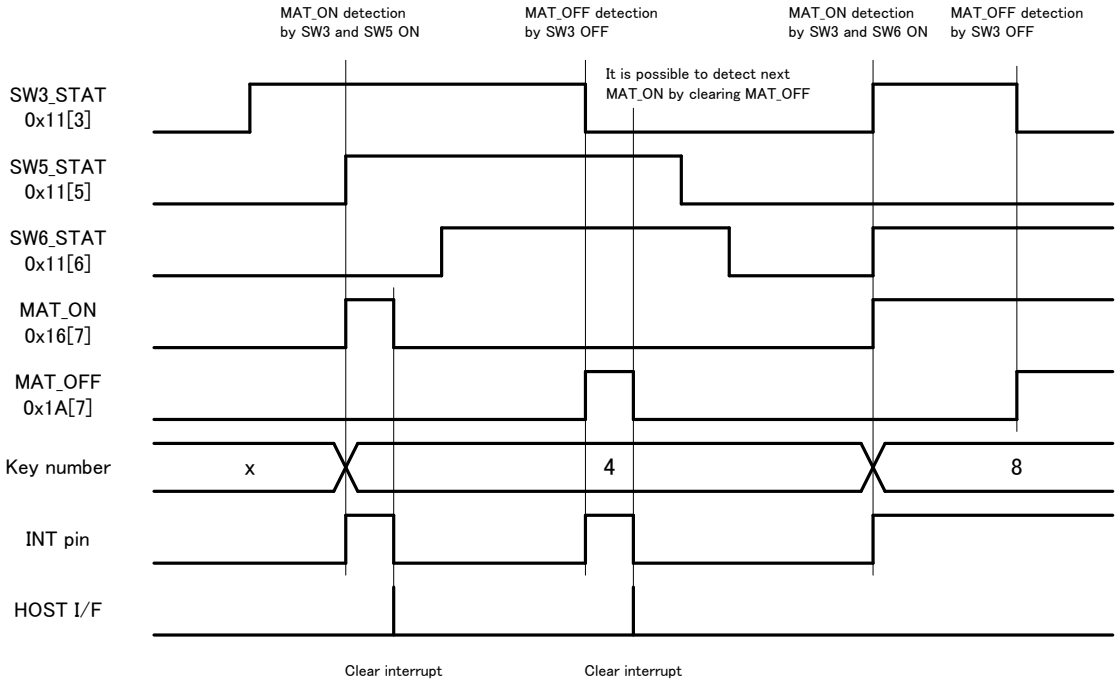


Figure 27. Matrix Switch

Calibration function

An internal circuit setting and reference data setting are performed by the calibration. Because the control is different from the normal sensing during performing calibration, IC does not detect the ON / OFF judgment and update the value of sensor.

There are three kinds of calibration, software calibration, periodic calibration, and the re-calibration due to an error.

Software calibration (CAL)

This is a calibration executed by writing '1' to both register CALIB (0xFF [1]) and register ACT (0xFF [0]). When a setting is changed, please perform a software calibration. When the software calibration is completed, the data '1' is set to register CAL (0x10[1]) and an interrupt is generated. It is possible to select whether IC execute this calibration for ON sensor by setting the register CALMOD (0xFF [4]).

Periodic calibration (PERCAL)

This is a calibration executed periodically. It is possible to select whether IC execute this calibration by setting PERCAL_DIS (0xE1 [4]). When the periodic calibration is completed, the data '1' is set to the register PERCAL (0x10[4]). The periodic calibration interval is set by register PERCAL_PERIOD (0xEF [7:4]).

Re-calibration due to an error (RECAL)

This calibration is performed when the following situations occur. The data 1 is set to the register RECAL (0x10 [2]) after the calibration is completed.

Drift calibration

This IC performs the calibration when IC detected drift by temperature. It performs calibration when the number of sensor recognized drift is larger than DRIFT_SIN_NUM (0xFE [3:0]) setting value. IC does not recognize when there is a sensor with ON state. It is possible to disable drift calibration by setting DIRFT_DIS (0xE1 [0]) to 1.

Calib-error calibration

This IC performs a calibration when sensor value is less than reference value. It is assumed that the reference value after calibration is a least value. However if the calibration is performed with a finger on sensor, the reference value is larger than the value assumed. The calibration is performed to prevent the situation. The calibration is performed about only sensor channels are detected the error. It is possible to disable calib-error calibration by setting 1 to the register ERROR_DIS (0xE1 [1]).

Hopping calibration

This IC performs a calibration when IC detected noise. It performs a calibration with changing sampling frequency not to synchronize noise frequency. It is possible to disable changing frequency by setting 1 to the register FIX_BASE_CYC (0xE0 [5]). And it is possible to disable hopping calibration by setting 1 to the register HOP_DIS (0xE1 [2]).

Return calibration

This IC performs a calibration when the operation returns to intermittent operation again without finding a change of state after returning to normal operation from intermittent operation. It is possible to set the number of times of performing the calibration by the register RET_NUM (0xEE). It is possible to disable the function by setting 1 the register RET_DIS (0xE1 [4]).

Flow Chart Description Explanation

Operation is explained using the flow chart in the next chapter. Since the flow charts are created according to the following explanation, refer to it if needed. Note that there is also a different point although the base of description is the C language.

Explanation of a flow box.

... Details of this function are shown in other flow. Refer to the specified flow

Explanation of strings

Constant: The first character of a constant is the alphabetic character of a capital letter. And all alphabets are also capital letters henceforth. A value is set in constant declaration and the value is not changed after it.
example: SAMPLE

Variable: The first character of a variable is the alphabetic character of a small letter. And all alphabets are also small letters henceforth. An initial value is set if needed in variable declaration and a value is changed within a flow.
example: sample

Array: A constant and a variable may be used in an array. When using an array, a number enclosed in square brackets [] is shown in the last of a character string. The number in constant declaration and variable declaration expresses the number of elements of array. And the number in other flow expresses an element number of array. When initial values are assigned into array, the initial values array enclosed in braces { } is shown in declaration.
example: sample[4] = {2, 3, 5, 7} (in variable declaration)
Variable called sample consists of four elements and initial values are 2, 3, 5, and 7.
sample[2] (in normal flow)
It means second element of variable called sample. If it is in the above-mentioned initialization state, value of it is '3'.

Value: It is shown in any of a decimal number, a binary number, or a hexadecimal number. The first character of the value is digit or a capital latter of A to F, and the last of a character string shows number base. If the last character is a digit, it is a decimal number. If the last character is 'b', it is a binary number. If the last character is 'h', it is a hexadecimal number. When shown by the hexadecimal number, all alphabetic characters are shown by the capital letter. Since 'h' which shows the hexadecimal notation is shown by the small letter, it is distinguishable from a constant.
example : 46, 2Eh, 101110b

Register: It begins "0x" and an address is shown by the hexadecimal number. When specifying a bit, the bit range is shown by enclosing in square brackets [].

example:	0x30	1 byte of the register 0x30
	0x30[7:4]	bits 7-4 of the register 0x30
	0x30[0]	bits 0 of the register 0x30

Explanation of processing

The calculation result of the right-hand side is assigned to the left-hand side. When a register is in left-hand side, it means register writing. And when a register is in right-hand side, it means a result of register reading. However, in the case of a condition process, even if the register is described in the left-hand side, it means a result of register reading. When "to" is inserted into two registers, it means doing sequential access of the data between the two addresses.
example: 0x20 to 0x2B a sequential access from the register 0x20 to register 0x2B

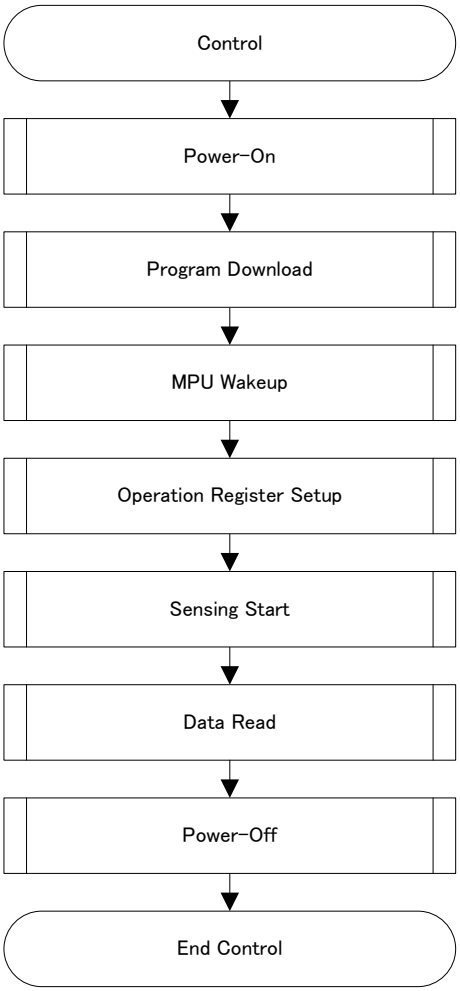
Control

BU21077MUV is controlled by the following flows

1 Power-On
2 Program Download
3 MPU Wakeup
4 Operation Register Setup
5 Sensing Start
6 Data Read
7 Power-Off

Control Flow Chart

Details of each flow are shown from the next page. Please refer to Flow Chart Description Explanation on page 7 for description of a flow chart.



Please refer to page 41 for detail
Please refer to page 42 for detail
Please refer to page 44 for detail
Please refer to page 45 for detail
Please refer to page 46 for detail
Please refer to page 47 for detail
Please refer to page 49 for detail

Power-On

The reset is canceled by changing RSTB from low to high after power is supplied. DVDD rises by reset cancel and power on reset is canceled. And built-in power on reset (POR) circuit is turned off and it is possible to access by host interface. When short-circuiting RSTB to VDD, DVDD rises automatically after power is supplied, and power on reset is canceled. In case of connecting RSTB and VDD, DVDD boots and POR circuit is turned off automatically.

Power-On Flow Chart

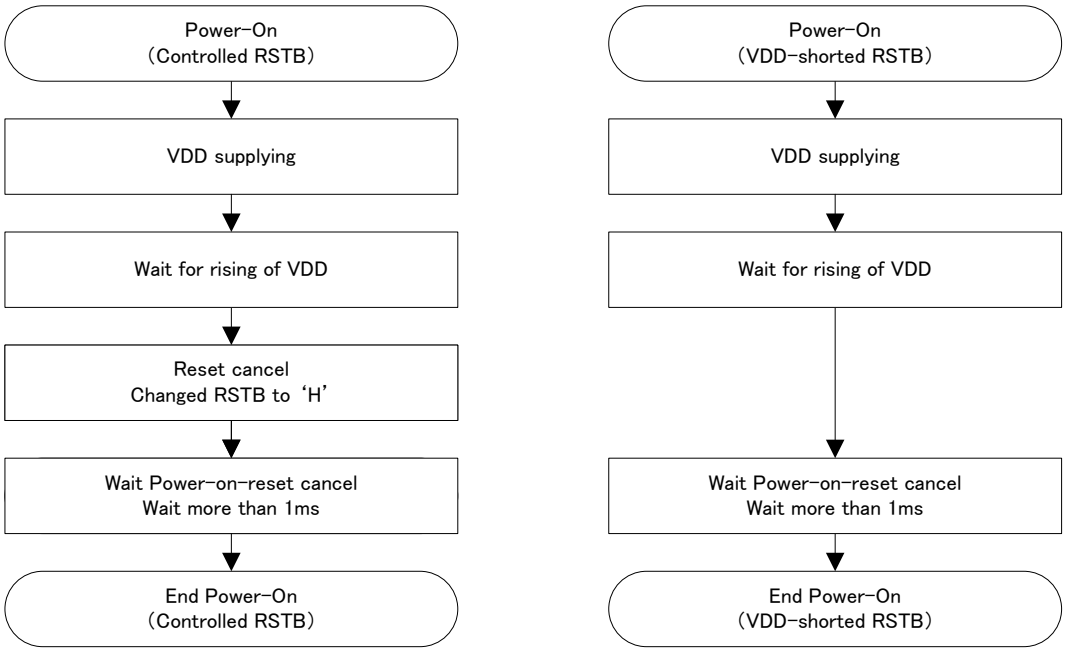


Figure 288. Power-On Flow Chart

Power-On Waveform

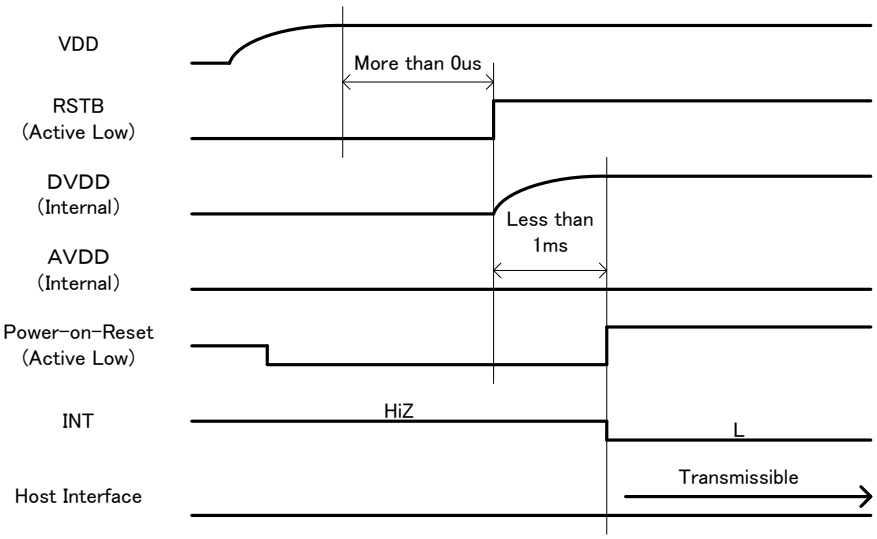


Figure 29. Power-On Waveform

Program Download

When IC is reset by RSTB, WDTR reset, and software reset, IC is initialized and clear all register values. It is necessary to download a program to program RAM after reset cancel in order to operate MPU. Program download is performed by writing data in the register for download after enabling an oscillator and resetting a download circuit. When the data transfer for 8K bytes is completed, IC judges whether program download is successful by comparing a checksum. If download is successful, the data 1 is set to DL_PASS (0xB7 [2]). If download is failed, the data 1 is set to DL_FAIL (0xB7 [3]). Please note that the MPU does not operate when program download is failed.

Program Download Flow Chart

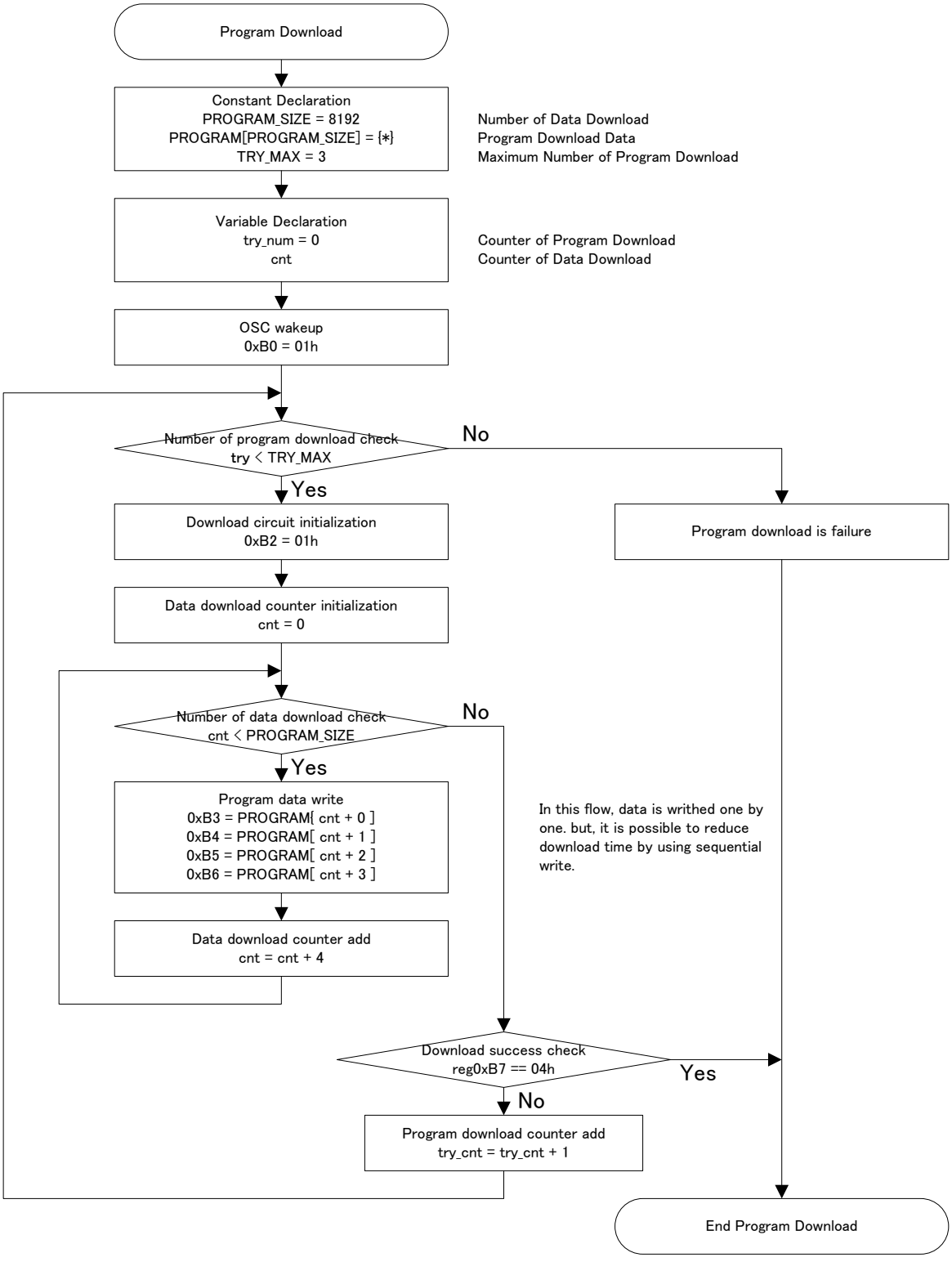


Figure30. Program Download Flow Chart

Program Download Waveform

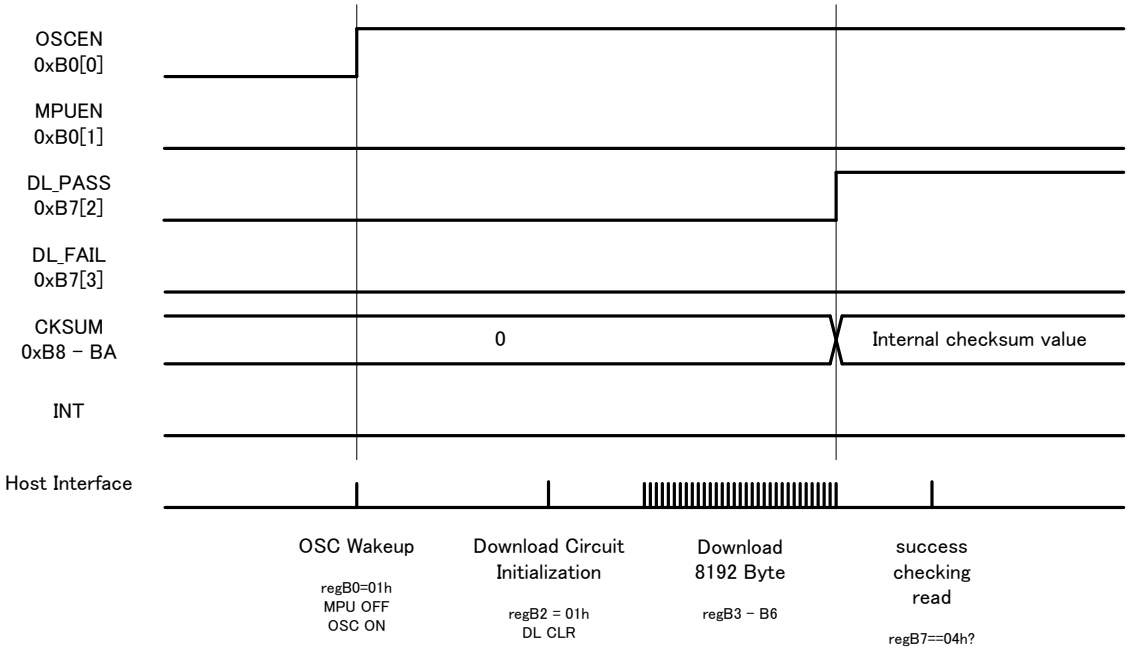


Figure 3129. Program Download Waveform

MPU Wakeup

MPU boots and starts initialization when the data 1 is set to the register MPUEN (0xB0 [0]) with DL_PASS (0xB7 [2]) =1. The data 1 is set to the register INI (0x10[0]) when the MPU initialization is completed.

MPU Wakeup Flow Chart

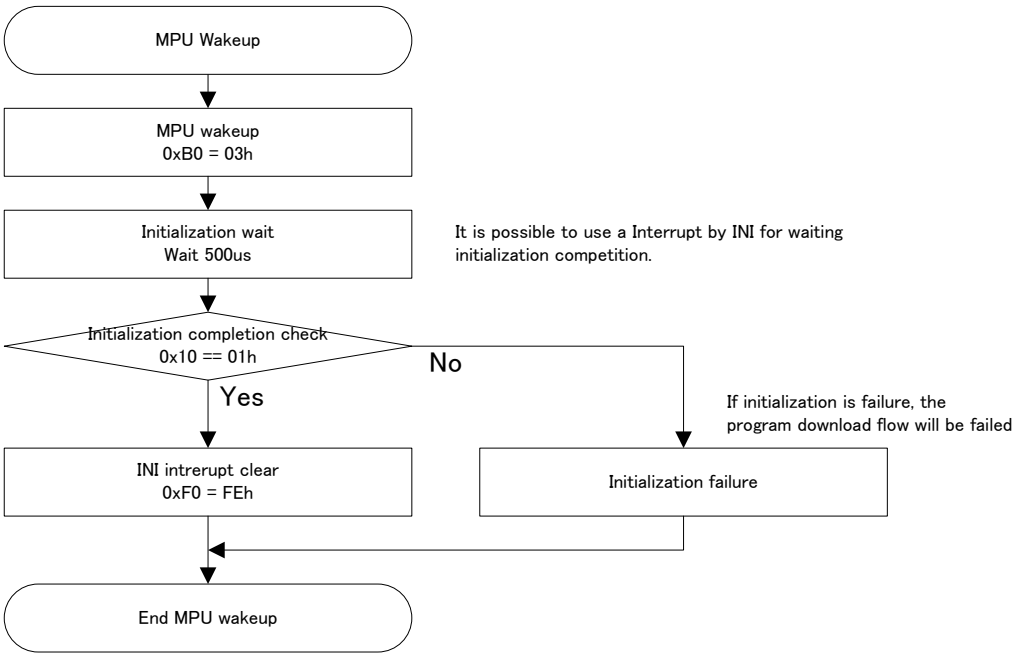


Figure 3230. MPU Wakeup Flow Chart

MPU Wakeup Waveform

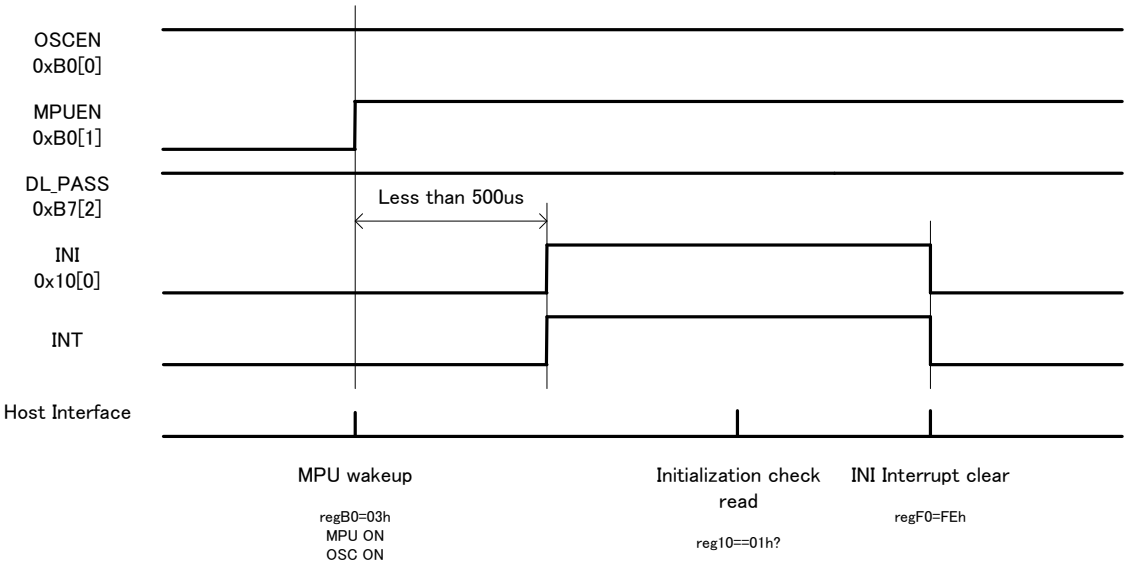
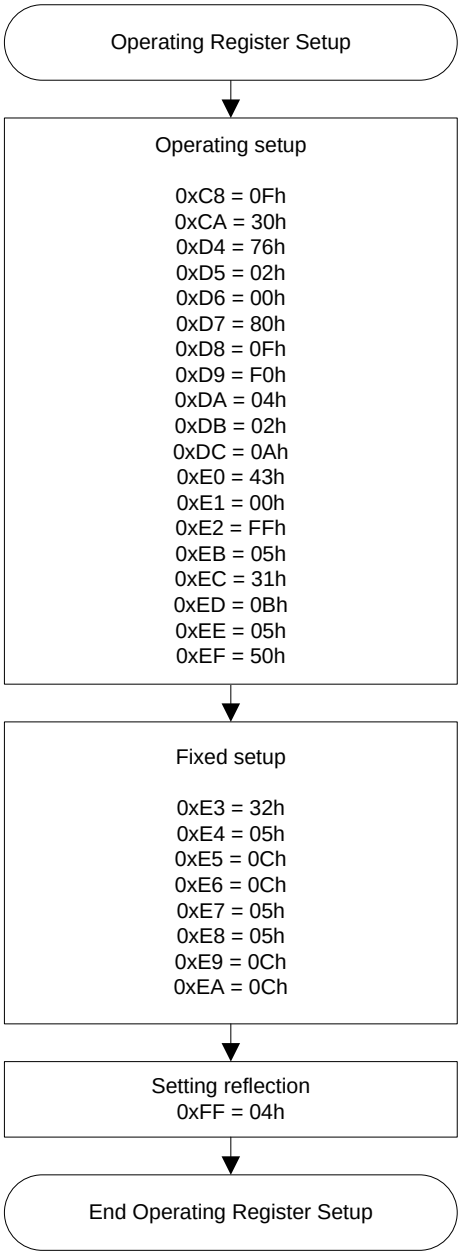


Figure 313. MPU Wakeup Waveform

Operating Register Setup

The setting values that set in register address from 0xC0 to 0xEF are reflected by setting 1 to the register CFG (0xFF [2]). Please set the data 1 to CFG (0xFF [2]) when the setting value is changed.

Operating Register Setup Flow Chart



These setting values are examples.
Change these values if needed.

These are fixed values usually.
Sense these does not match the initial values, setup these values.

Figure 34. Operating Register Setup Flow Chart

Sensing Start

Sensing starts by setting 1 to the register ACT (0xFF [0]). Please send the soft calibration command at a sensing start. The data 1 is set to the register CAL (0x10[1]) when the software calibration is completed. The processing of the register CFG is preferred to the processing of the register ACT. It is possible to reflect setting values, calibration and starting sensing by setting 07h to the register CONTROL (0xFF).

Sensing Start Flow Chart

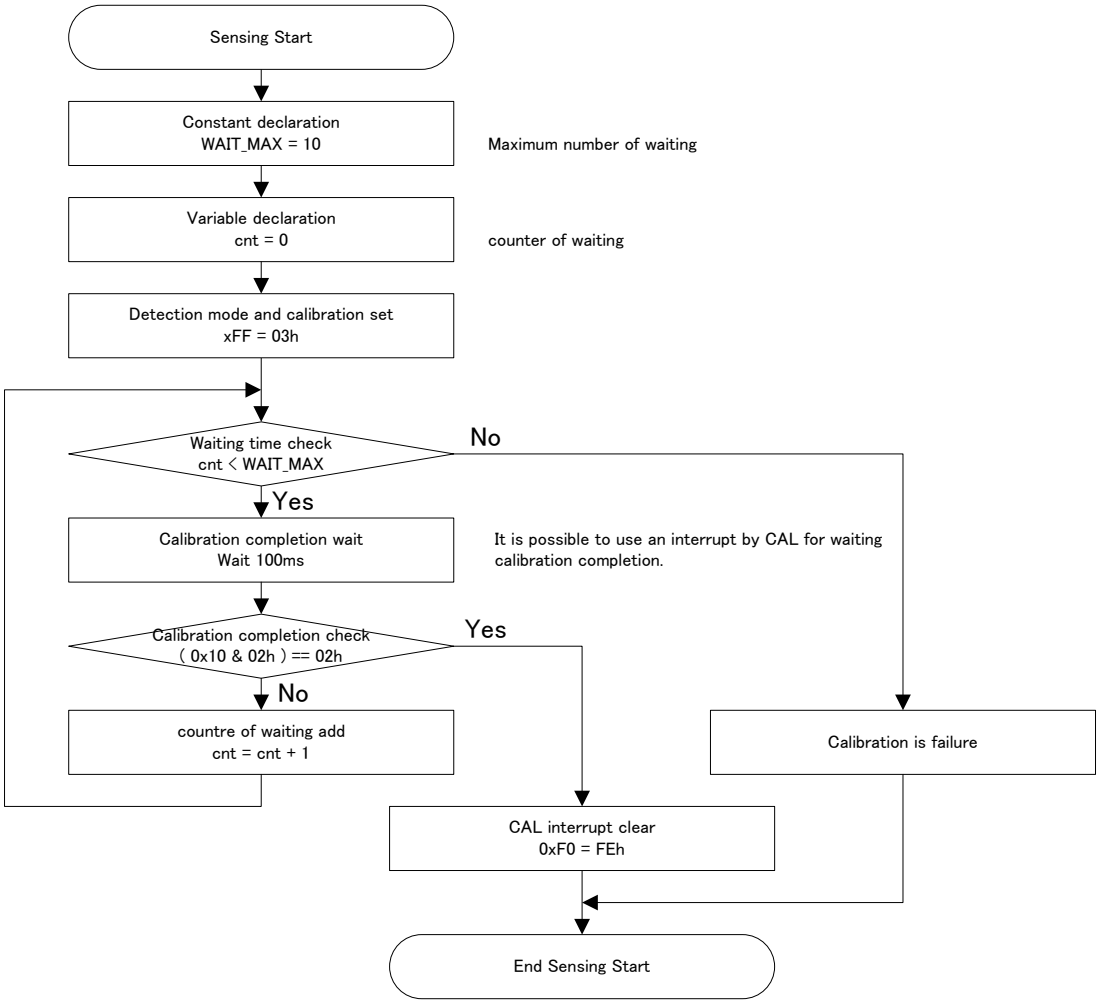


Figure 35. Sensing Start Flow Chart

Sensing Start Waveform

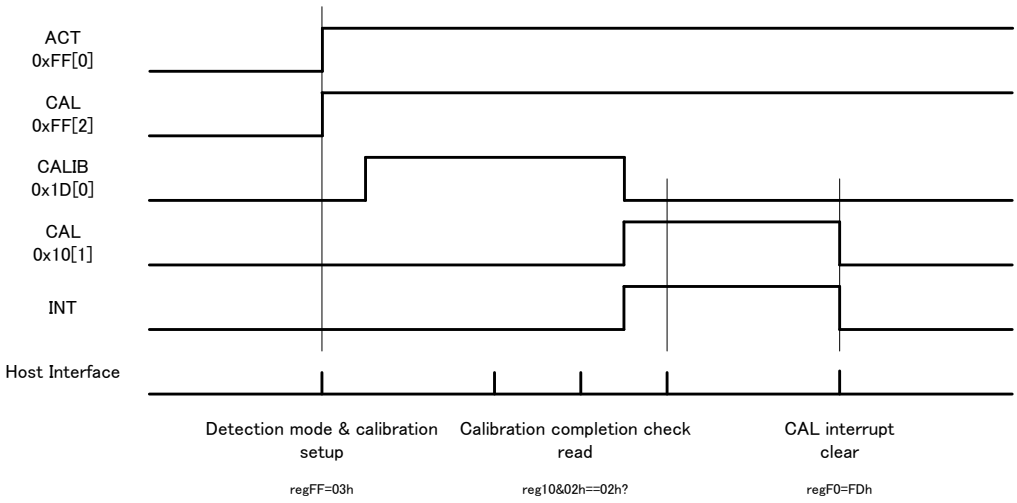


Figure 326. Sensing Start Waveform

Data Read

IC performs ON and OFF detection of switches by using the sensor data when sensing starts. The result is stored in registers. It is possible to recognize the state of sensors by reading the registers. There are 2 methods to read the data. First is the polling system which reads at a fixed interval. Second is the interrupt system which uses the INT pin.

Polling System

This system is simple. But current consumption is larger because the data is always accessed.

Polling System Flow Chart

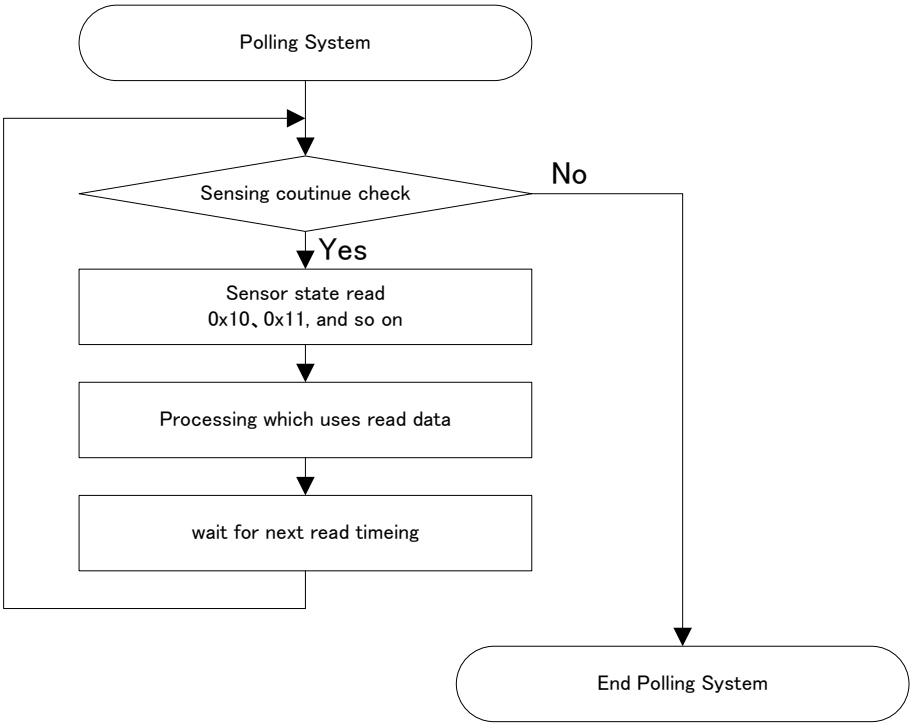


Figure 337. Polling System Flow Chart

Polling System Waveform

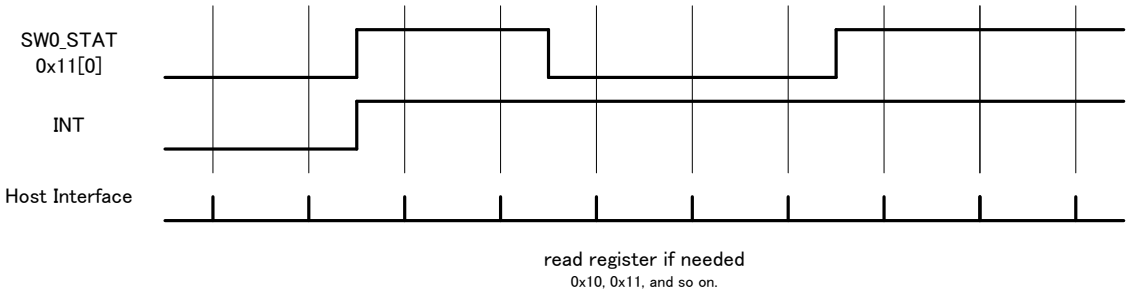


Figure 348. Polling System Waveform

Interrupt system

This system is to read the data at INT pin high with checking the state of the INT pin. The result of calibration completion and ON/OFF result is assigned to the register INT_STATE (0x10) and the result of OR operation of the registers is outputted from INT pin. The interrupt signal is kept until clearing the register. Please clear the interrupt data if necessary. It is to mask the particular interrupt by using mask function.

Interrupt System Flow Chart

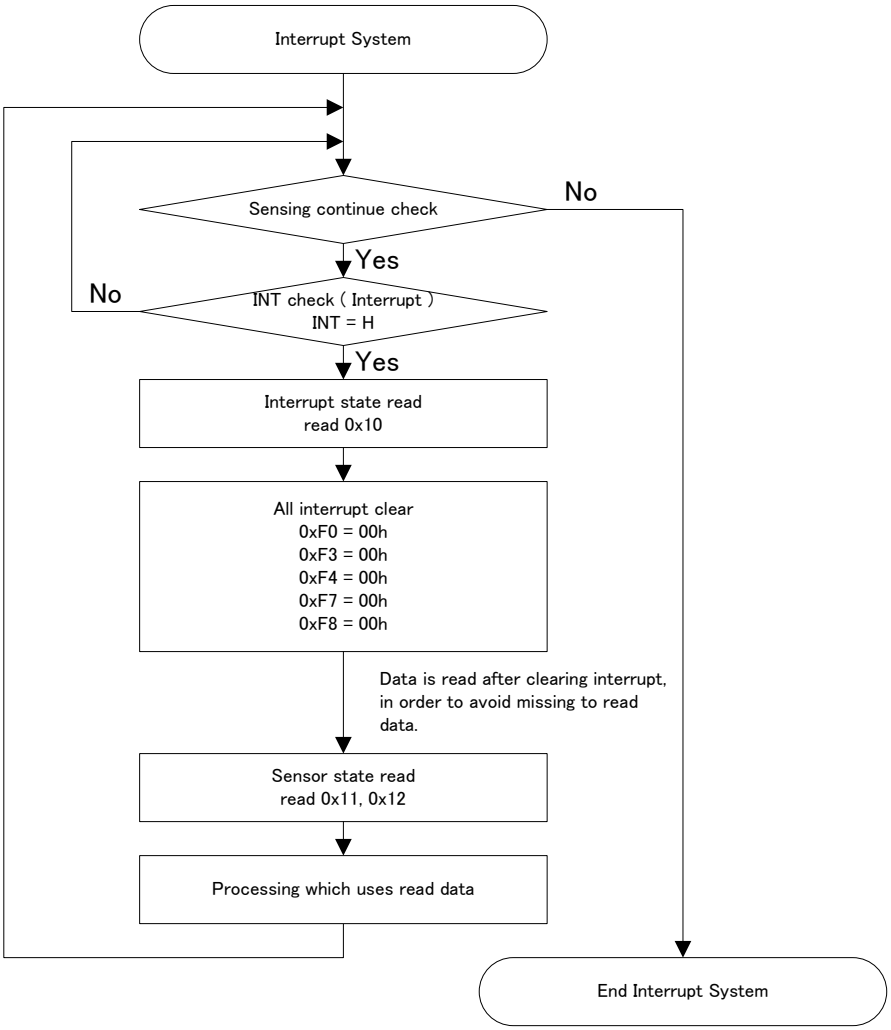


Figure 359. Interrupt System Flow Chart

Interrupt System Waveform

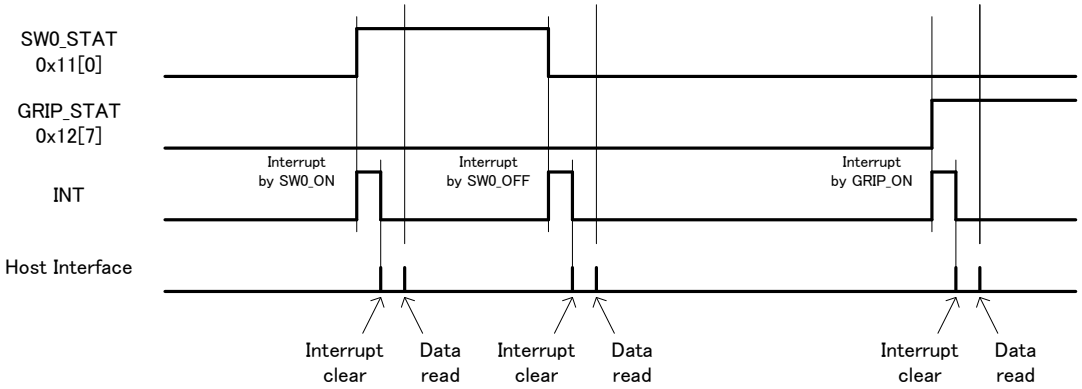


Figure40. Interrupt System Waveform

Power-Off

IC is reset by changing RSTB from high to low. DVDD falls by reset. Please stop power supplying. Please stop power supplying in case of connecting RSTB and VDD. If power supplying is stopped, DVDD voltage falls and IC is reset automatically.