Bytes = 2^8

Cache = 2^3

Block = 2^1

Tag = 5; index = 2; Offset = 1;

1. A)

b)

tag ind offset data

00001 00 1 9

00001 01 1 11

00010 10 1 21

00000 11 1 7

|  |  |  |  |
| --- | --- | --- | --- |
| Address Reference | Binary Address | Hit/Miss | Assigned Cache Block (index) |
| 0 | 0000 0000 | Miss | 00 |
| 1 | 0000 0001 | Miss | 00 |
| 2 | 0000 0010 | Miss | 01 |
| 3 | 0000 0011 | Miss | 01 |
| 7 | 0000 0111 | Miss | 11 |
| 8 | 0000 1000 | Miss | 00 |
| 9 | 0000 1001 | Miss | 00 |
| 2 | 0000 0010 | Miss | 01 |
| 18 | 0001 0010 | Miss | 01 |
| 10 | 0000 1010 | Miss | 01 |
| 11 | 0000 1011 | Miss | 01 |
| 20 | 0001 0100 | Miss | 10 |
| 21 | 0001 0101 | Miss | 10 |
| 11 | 0000 1011 | Hit | 01 |

c) Miss rate = 13 / 14 = 92.857%

Hit rate = 1 / 14 = 7.1425%

Tag = 5; Index = 3; Offset = 0;

|  |  |  |  |
| --- | --- | --- | --- |
| Address Reference | Binary Address | Hit/Miss | Assigned Cache Block (index) |
| 0 | 0000 0000 | Miss |  |
| 1 | 0000 0001 | Miss |  |
| 2 | 0000 0010 | Miss |  |
| 3 | 0000 0011 | Miss |  |
| 7 | 0000 0111 | Miss |  |
| 8 | 0000 1000 | Miss |  |
| 9 | 0000 1001 | Miss |  |
| 2 | 0000 0010 | Hit |  |
| 18 | 0001 0010 | Miss |  |
| 10 | 0000 1010 | Miss |  |
| 11 | 0000 1011 | Miss |  |
| 20 | 0001 0100 | Miss |  |
| 21 | 0001 0101 | Miss |  |
| 11 | 0000 1011 | Hit |  |

Miss rate = 12/14 = 85.715%

Hit = rate = 2/14 = 14.285%

Tag ind offset data

000101 00 n/a 20

000101 01 n/a 21

000010 10 n/a 10

000010 11 n/a 11



|  |  |  |  |
| --- | --- | --- | --- |
| Address Reference | Binary Address | Hit/Miss | Assigned Cache Block (index) |
| 16 | 0001 0000 |  |  |
| 11 | 0000 1011 |  |  |
| 30 | 0001 1110 |  |  |
| 4 | 0000 0100 |  |  |
| 9 | 0000 1001 |  |  |
| 19 | 0001 0011 |  |  |
| 24 | 0001 1000 |  |  |
| 12 | 0000 1100 |  |  |
| 6 | 0000 0110 |  |  |
| 4 | 0000 0100 |  |  |
| 16 | 0001 0000 |  |  |
| 8 | 0000 1000 |  |  |
| 12 | 0000 1100 |  |  |
| 19 | 0001 0011 |  |  |
| 27 | 0001 1011 |  |  |
| 14 | 0000 1110 |  |  |
| 6 | 0000 0110 |  |  |

3.

4B blocks = 2^2 = 2 bit offset

8 bit address length – 2 bit offset = 6 bit tag

|  |  |  |  |
| --- | --- | --- | --- |
| Address Reference | Binary Address | Hit/Miss | Cache line used |
| 3 | 0000 0011 | Miss | 00 |
| 14 | 0000 1110 | Miss | 01 |
| 17 | 0001 0001 | Miss | 10 |
| 12 | 0001 1100 | Miss | 11 |
| 26 | 0001 1010 | Miss | 00 |
| 9 | 0000 1001 | Miss | 01 |
| 21 | 0001 0101 | Miss | 10 |
| 24 | 0001 1000 | Miss | 11 |
| 5 | 0000 0101 | Miss | 00 |
| 11 | 0000 1101 | Miss | 01 |

Miss rate = 100%

Hit rate = 0%

00 5

01 11

10 21

11 24