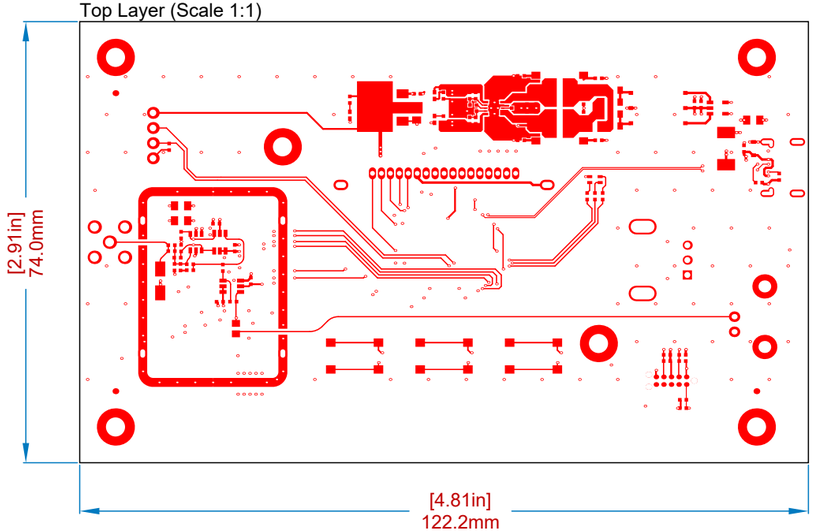
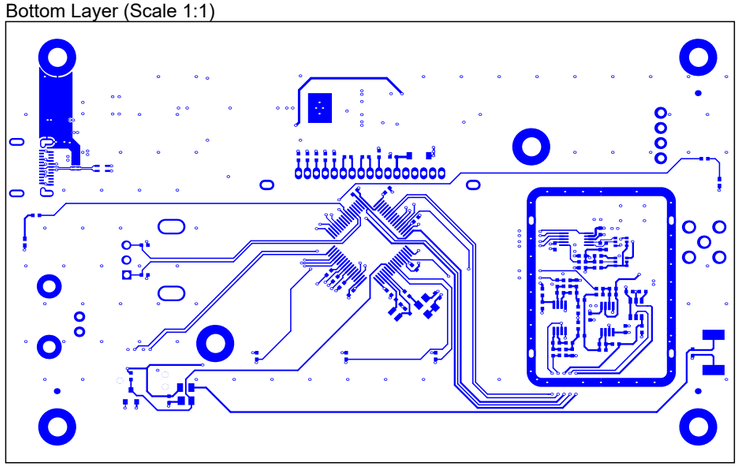
Top Layer (Scale 1:1)



Bottom Layer (Scale 1:1)



PCB Details

1. Minimum Trace/Space: 10/10 mil
2. Stackup: See Page 4
3. Dimensions: 5in x 3in
4. Via Types: Through
5. Hole tolerances are ±3mil unless otherwise noted
6. Epoxy fill and planarize vias of the following sizes:
   N/A

Requirements

7. ELECTRICAL TEST:
   Vendor to perform Electrical Test against provided netlist file.
8. PANELIZATION:
   Vendor to panelize design as 1-up array

△9 HANDLING TABS:
Vendor to add 2 handling tabs to panelized array along indicated edges.
Handling tabs shall be 0.5" in width.
Handling tabs shall include 2x 0.125in tooling holes and 2x 0.31in fiducials

△10 VENDOR LOGO:
Vendor may add their logo on silkscreen at indicated location.

11. THIEVING:
    Vendor shall not add thieving within the PCB outline. Vendor may add thieving as required to the handling tabs to meet manufacturability requirements.

△12 SERIALIZATION:
Vendor to add serial numbers to each board at indicated location.
Serial Number shall be of the following format: YYWWNNNN
YY - 2-digit year of manufacture
WW - 2-digit week of manufacture
NNNN - 4-digit serial number within manufacturing lot.

THIRD ANGLE PROJECTION

APPROVALS	DATE
ENGINEER: Alexander Davis	9/16/2024
PART NO: FL-0004	REV: A
VARIANT: [No Variations]	

Flycatcher

8921 E. Summer Trail
Tucson, AZ 85749
Tucson, AZ 85749
www.flycatcherlabs.com

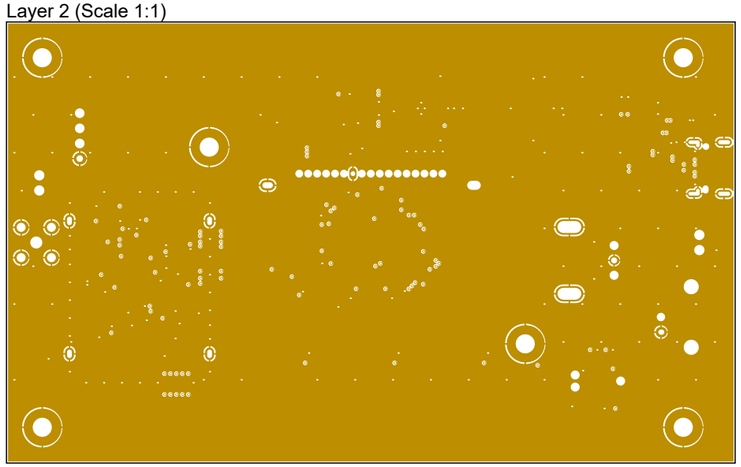
TITLE: Power Rail Probe

Designed For: Public Release

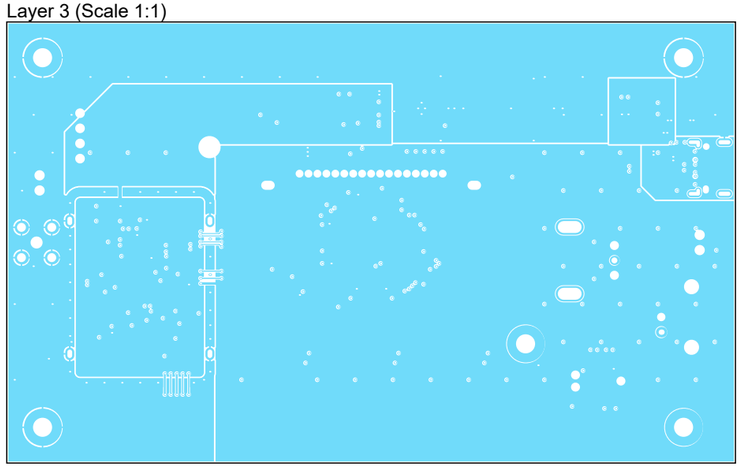
SIZE: B

SCALE:	FILE NAME:	SHEET:
	Fabrication.PCBDwf	1 OF 4

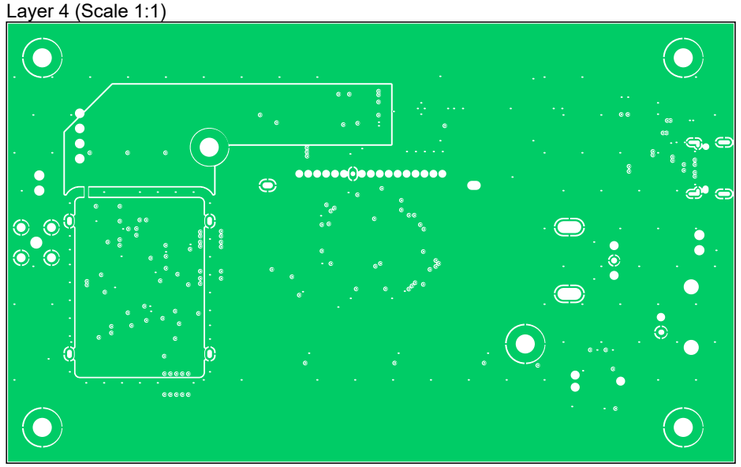
Layer 2 (Scale 1:1)



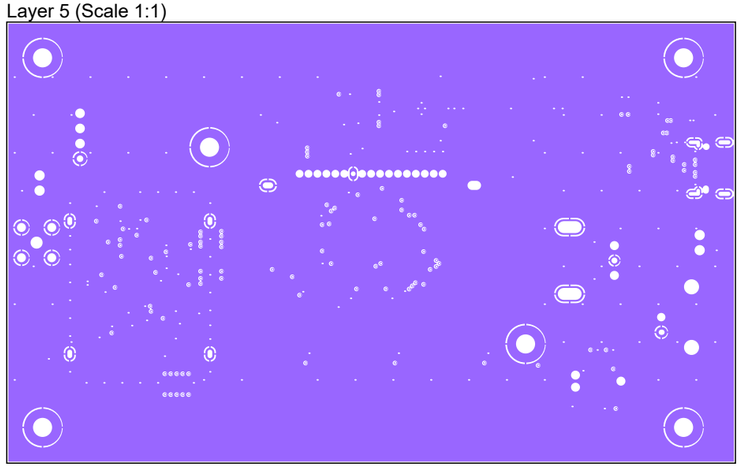
Layer 3 (Scale 1:1)



Layer 4 (Scale 1:1)



Layer 5 (Scale 1:1)



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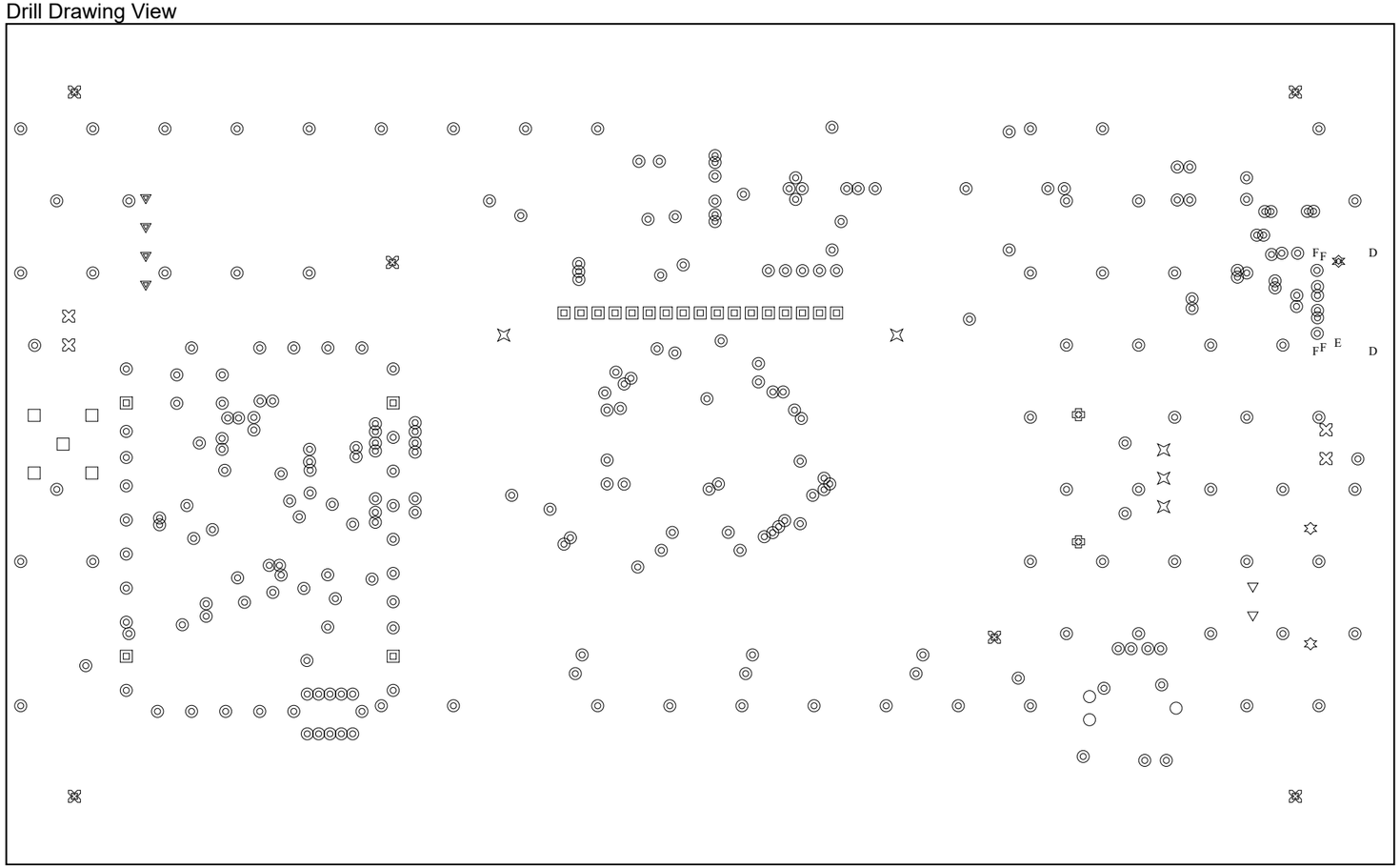
SCALE: | FILE NAME: Fabrication.PCBDwf | SHEET: 2 OF 4

Drill Drawing View



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◎	291	10.00mil(0.25mm)	Plated	
E	1	19.69mil(0.50mm)	Non-Plated	
⧑	1	23.62mil(0.60mm)	Non-Plated	
F	4	23.62mil(0.60mm)	Plated	
D	2	27.56mil(0.70mm)	Plated	
⧈	21	31.50mil(0.80mm)	Plated	
▽	2	35.00mil(0.89mm)	Plated	
○	3	39.00mil(0.99mm)	Non-Plated	
⧖	5	39.37mil(1.00mm)	Plated	
▽	4	43.31mil(1.10mm)	Plated	+0.00mil(0.00mm)/-9.84mil(0.25mm)
⧖	4	47.24mil(1.20mm)	Non-Plated	
□	5	59.06mil(1.50mm)	Plated	
⧈	2	78.74mil(2.00mm)	Plated	
⧑	2	79.00mil(2.01mm)	Plated	
⧑	6	125.98mil(3.20mm)	Plated	

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Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	1.00mil	Solder Resist	Solder Mask	GTS
Nickel, Gold	Top Surface Finish	0.16mil		Surface Finish	
Copper	Top Layer	1.70mil		Signal	GTL
Prepreg		*4.36mil*	*FR408*	*Dielectric*	
CF-004	Layer 2	0.69mil		Signal	G1
Core		*4.00mil*	*FR408*	*Dielectric*	
CF-004	Layer 3	0.69mil		Signal	G2
Prepreg		*36.44mil*	*PP-006*	*Dielectric*	
CF-004	Layer 4	0.69mil		Signal	G3
Core		*4.00mil*	*FR408*	*Dielectric*	
CF-004	Layer 5	0.69mil		Signal	G4
Prepreg		*4.36mil*	*FR408*	*Dielectric*	
Copper	Bottom Layer	1.70mil		Signal	GBL
Nickel, Gold	Bottom Surface Finish	0.16mil		Surface Finish	
Surface Material	Bottom Solder	1.00mil	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 61.63mil

Stackup Information

13. Surface Finish: ENIG
14. Soldermask Color: Blue
15. Silkscreen Color: White
16. Thickness tolerance: ±10%

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Trace layer	Reference layers	Clearance	Target Tolerance
1	Coated Microstrip	50	Top Layer	Layer 2	5.00mil	10%
2	Coated Coplanar Waveguide With Ground	50	Top Layer	Layer 2	6.00mil	10%
3	Edge-Coupled Coated Microstrip	90	Top Layer	Layer 2	5.00mil	10%
4	Offset Stripline	50	Layer 3	Layer 2,Layer 5	0.00mil	10%
5	Offset Stripline	50	Layer 4	Layer 2,Layer 5	0.00mil	10%
6	Coated Microstrip	50	Bottom Layer	Layer 5	5.00mil	10%
7	Coated Coplanar Waveguide With Ground	50	Bottom Layer	Layer 5	6.00mil	10%
8	Edge-Coupled Coated Microstrip	90	Bottom Layer	Layer 5	5.00mil	10%

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