

Ada Zaǵyapan 22401942

EEE102-02

26 February 2025

LAB-3: Combinational Logic Circuit

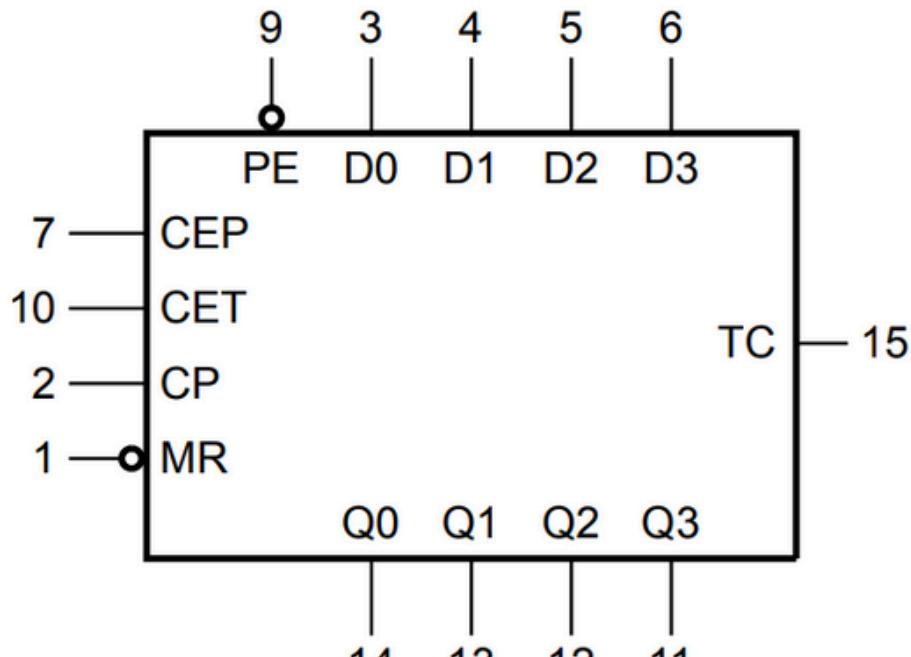
PURPOSE

The purpose of this experiment is to learn how to generate and observe different 3-bit input combinations using a 74HC163 counter and feed those signals into a combinational logic circuit using a breadboard, jumper wires, a counter and logic gates. The circuit was observed and the output waveform was depicted using a function generator and oscilloscope.

DESIGN SPECIFICATIONS

74HC163 4-bit counter: The 74HC163 is a 4-bit binary counter that increases on each rising clock edge whenever both count-enable pins (CEP and CET) are active and parallel enable (PE) is switched off. It provides a synchronous reset (MR), triggered in harmony with the clock, which helps avoid asynchronous disruptions. Furthermore, its data inputs (D0–D3) allow the user to load a predetermined value if PE is enabled, and the terminal count (TC) output along with look-ahead carry logic simplifies chaining several counters together. The Q0–Q3 outputs produce a binary sequence from 0000 up to 1111 (Figure 1.1).¹

¹74HC163PW (Presettable synchronous 4-bit binary counter; synchronous reset) | Nexperia. (2018, October 12.). Retrieved February 25, 2025, from <https://www.nexperia.com/product/74HC163PW>



aaa-012184

Figure 1.1: Pin configuration of 74HC163 counter

74HC02N quad 2-input NOR gate: The 74HC02N is a quad 2-input NOR gate IC that performs logical NOR operations on pairs of inputs and outputs the inverted OR result. Each of its four independent gates offers two inputs and one output, and produces $(A+B)'$ for the respective pair of signals. Its separate VCC (pin 14) and GND (pin 7) pins supply all four gates. Because NOR gates are functionally complete (like NAND gates), the 74HC02N can be used both alone or alongside other logic devices to build more complex digital systems (Figure 1.2).²

² 74HC02; 74HCT02 Quad 2-input NOR gate. (2008, September 18). <https://www.alldatasheet.com/datasheet-pdf/view/255270/NXP/74HC02N.html>

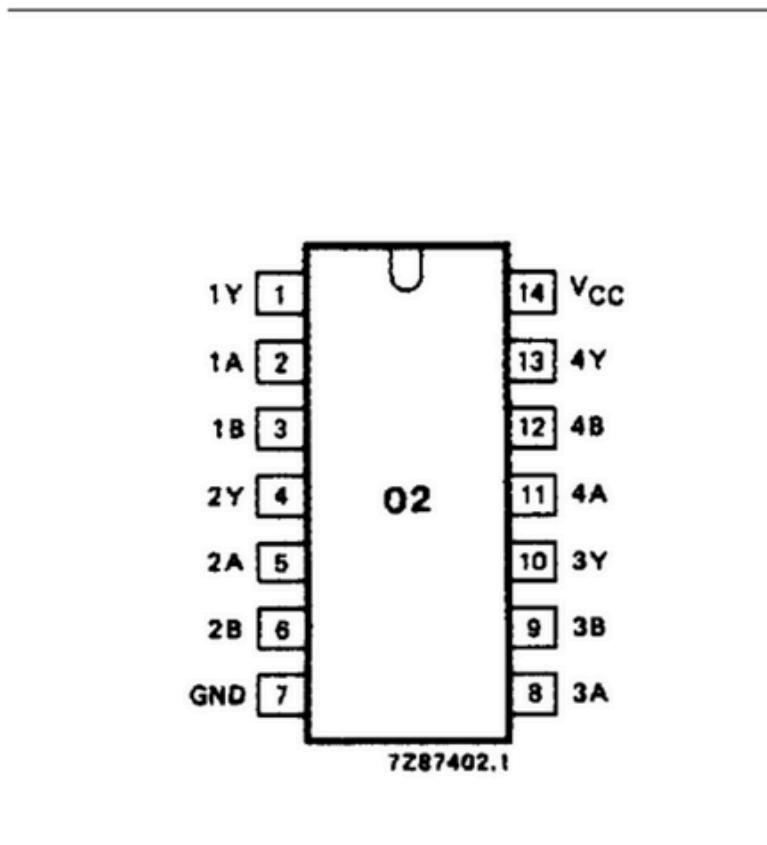


Figure 1.2: Pin configuration of 74HC02N NOR gate

74HC32N quad 2-input OR gate: The 74HC32N is a quad 2-input OR gate that executes the logical OR function on pairs of inputs and produces $(A+B)$ at each output. Each of its four independent gates has two input pins and a single output pin, powered by a standard supply range (often 2 V–6 V, typically +5 V in many labs). Pin 14 (VCC) and pin 7 (GND) supply all four gates (Figure 1.3).³

³ 74HC32; 74HCT32Quad 2-input OR gate. (2012, September 4). <https://www.alldatasheet.com/datasheet/pdf/view/536726/PHILIPS/74HC32N.html>

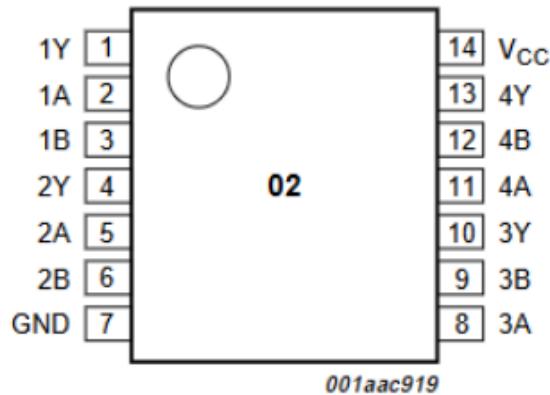


Figure 1.3: Pin configuration of 74HC32N

METHODOLOGY

The 74HC163 synchronous 4-bit counter was first placed on a breadboard, with its VCC (pin 16) tied to +5 V and its GND (pin 8) to ground. Two of the control pins, which are Parallel Enable (PE), Count Enable Parallel (CEP), were all set to +5 V so the counter could freely advance on every clock pulse. A 1 Hz, 0–5 V square wave from a function generator was then applied to the clock input (pin 2), providing a slow, visible increment of the binary outputs Q0, Q1, Q2, and Q3. Four LEDs (each in series with a $500\ \Omega$ resistor) were attached to these outputs so that the progression from 0000 to 1111 could be observed.

A 74HC02N (quad 2-input NOR gate) was also powered by +5 V at pin 14 and grounded at pin 7. One of its NOR gates was used to NOR together Q0 and Q2 from the counter, with the remaining three gates set to known logic levels on their inputs. Meanwhile, a 74HC32N (quad 2-input OR gate) was placed on the same breadboard, similarly powered at pins 14 (VCC) and 7

(GND). One of its OR gates took two inputs: (1) the NOR output from the 74HC02N, and (2) Q1 from the 74HC163. The resulting OR output was designated as the final signal R. The truth table of the circuit can be seen in Table 2.1, and the gate schematic can be observed in Figure 2.1. Another LED and 1 kΩ series resistor were connected to R so that its behavior could be seen. The positive arm of the signal generator was connected to pin 2 (Clock Input) of the counter, and the negative arm was connected to the ground. The positive arm of the power supply was connected to +5 V and the negative arm was similarly connected to the ground. The circuit can be observed in Figure 2.2. After the circuit was working, an oscilloscope was connected to one leg of the 5th LED in order to see the waveform of the circuit.

| Q0 | Q1 | Q2 | Q0+Q2 | (Q0+Q2)' | R=(Q0+Q2)'+Q1 |
|----|----|----|-------|----------|---------------|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 |

Table 2.1: Truth table of $(Q0+Q2)'+Q1$

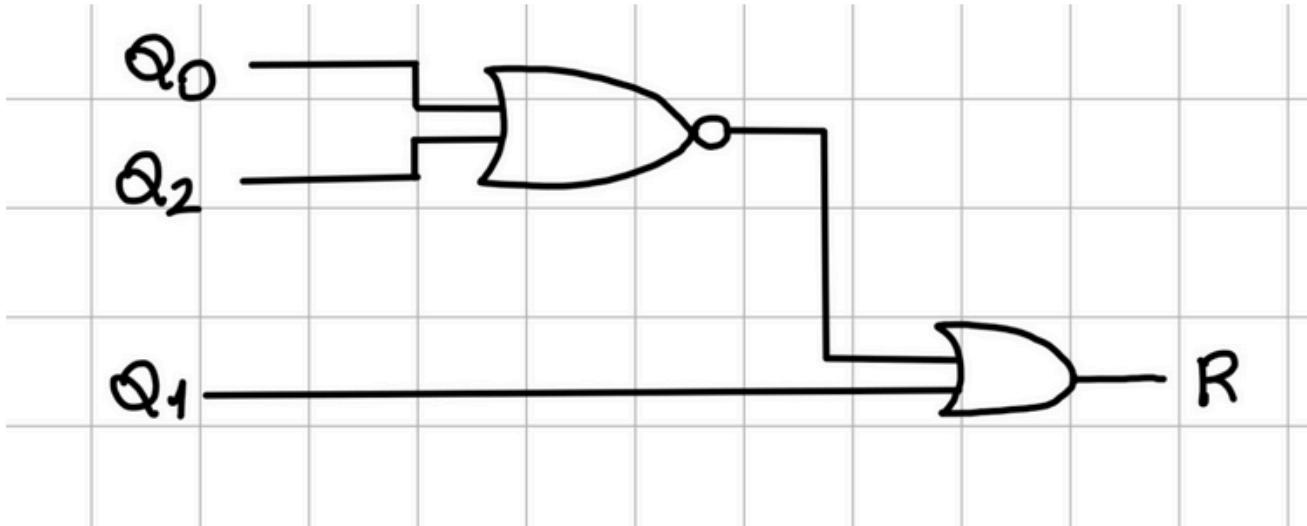


Figure 2.1: Schematic of $(Q_0 \text{ NOR } Q_2) \text{ OR } Q_1$

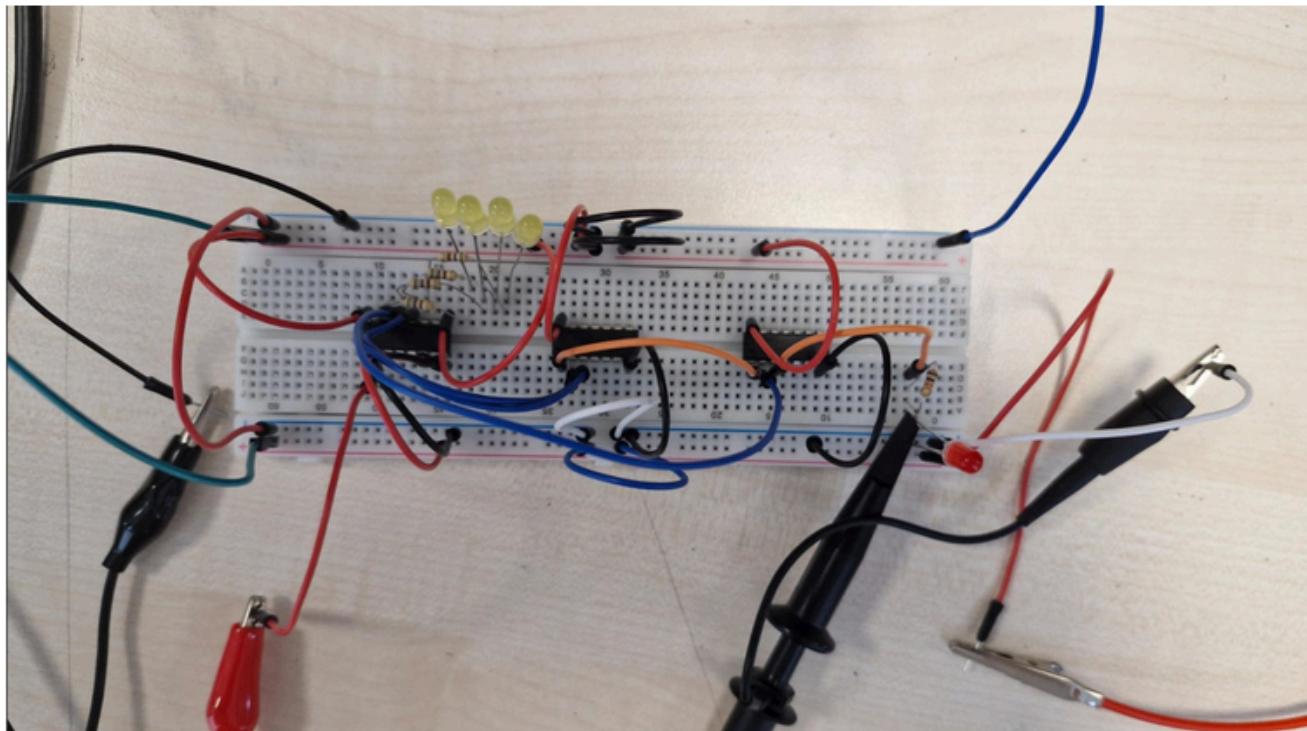


Figure 2.2: Combinational logic circuit including a counter, a NOR gate and an OR gate

RESULTS

Once the function generator began delivering the 1 Hz square wave, the 74HC163 outputs Q_0 – Q_3 stepped through all 16 binary combinations in a predictable sequence, which was

confirmed by the four LEDs turning on and off according to the 4-bit output given by the function generator (Figures 3.1-3.16). The NOR gate output, in conjunction with Q1 through the OR gate, produced the expected final signal R where the LED on R switched states according to the $(Q_0 \text{ NOR } Q_2) \text{ OR } Q_1$ logic, which can again be seen in Figures 3.1-3.16. The oscilloscope showed a stable 1 Hz clock waveform. The waveform was observed to align with the truth table's R values of 0 and 1 (Figure 3.17).

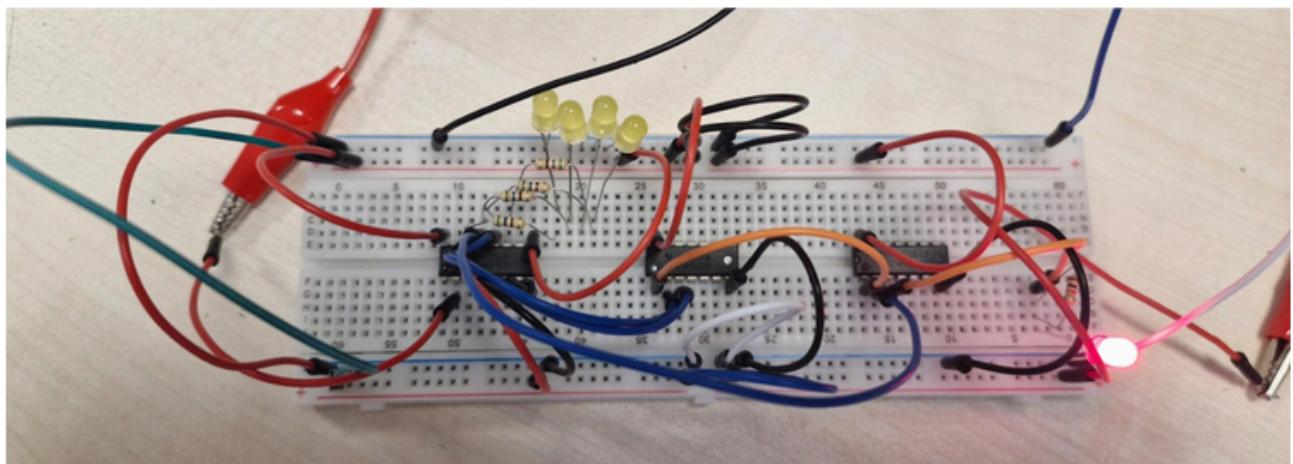


Figure 3.1: 0000, R=0 (LED is off), Q0=0, Q1=0, Q2=0

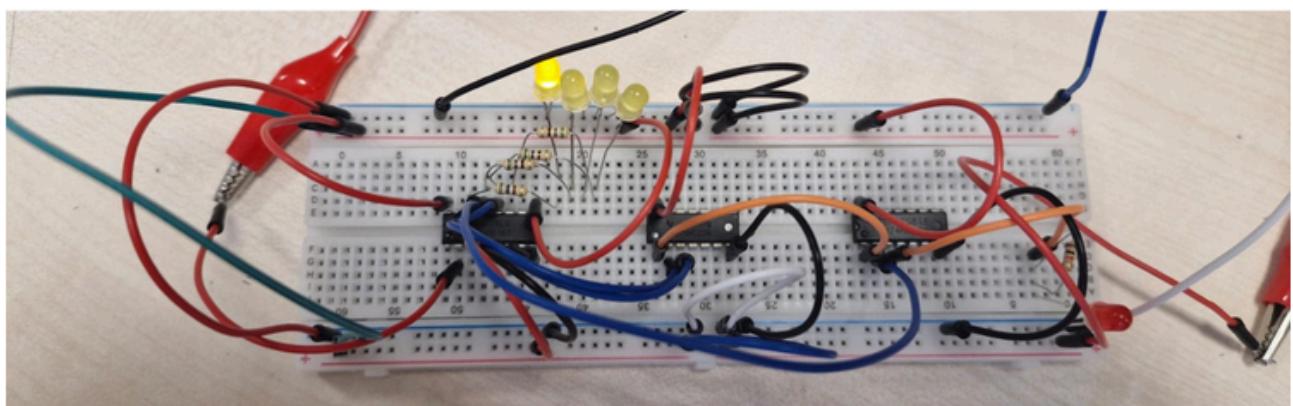


Figure 3.2: 0001, R=0 (LED is off), Q0=0, Q1=0, Q2=1

Zaǵyapan 8

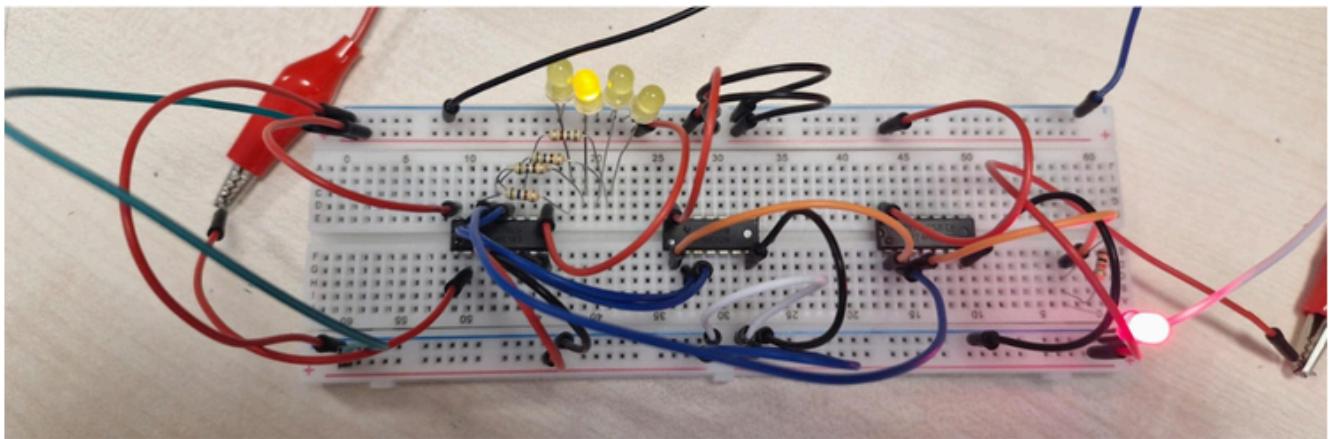


Figure 3.3: 0010, R=1 (LED is on), Q0=0, Q1=1, Q2=0

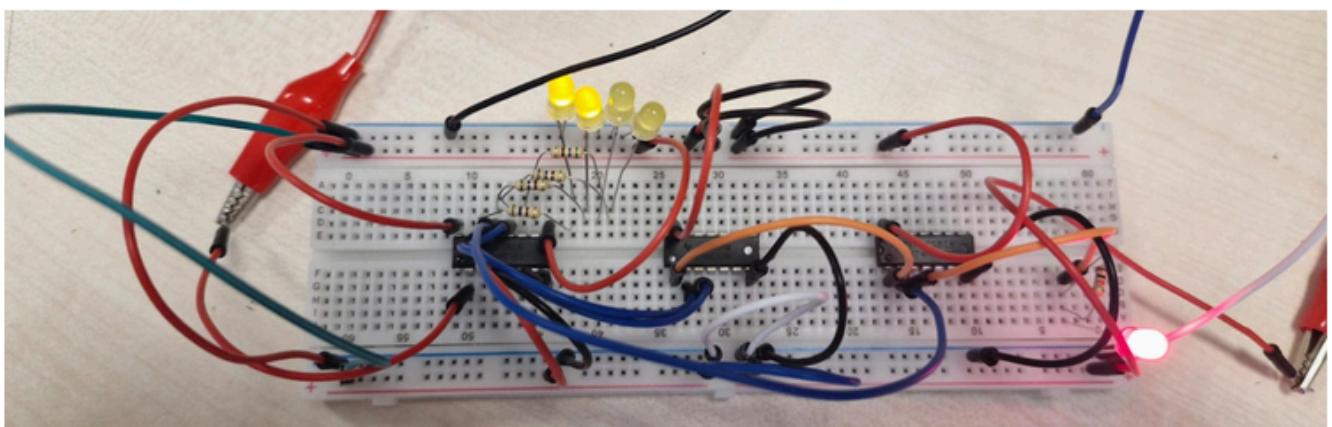


Figure 3.4: 0011, R=1 (LED is on), Q0=0, Q1=1, Q2=1

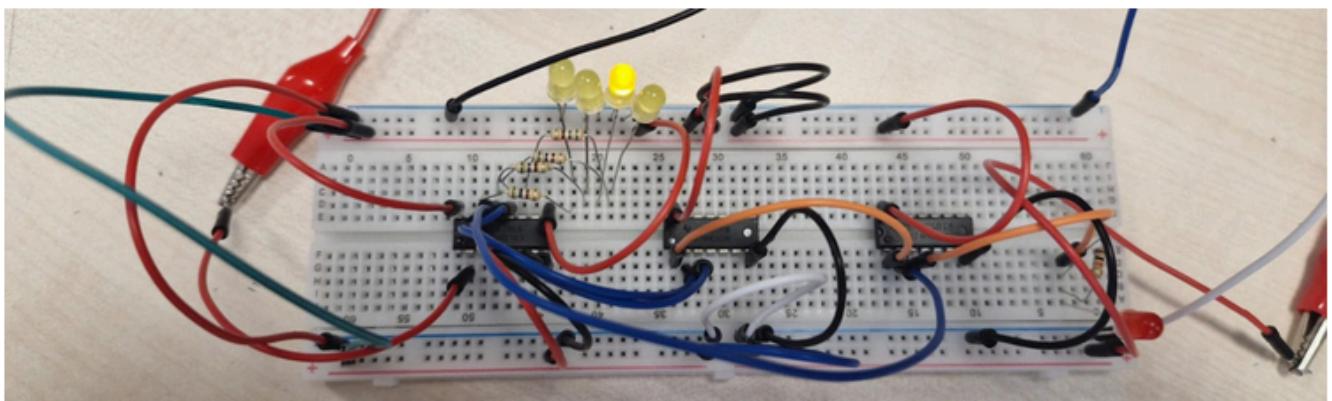


Figure 3.5: 0100, R=0 (LED is off), Q0=1, Q1=0, Q2=0

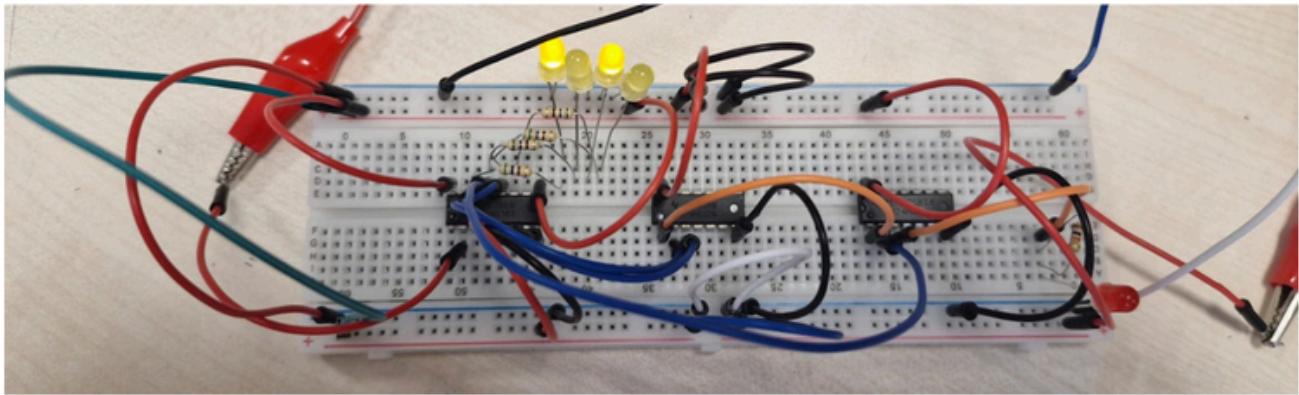


Figure 3.6: 0101, R=0 (LED is off), Q0=1, Q1=0, Q2=1

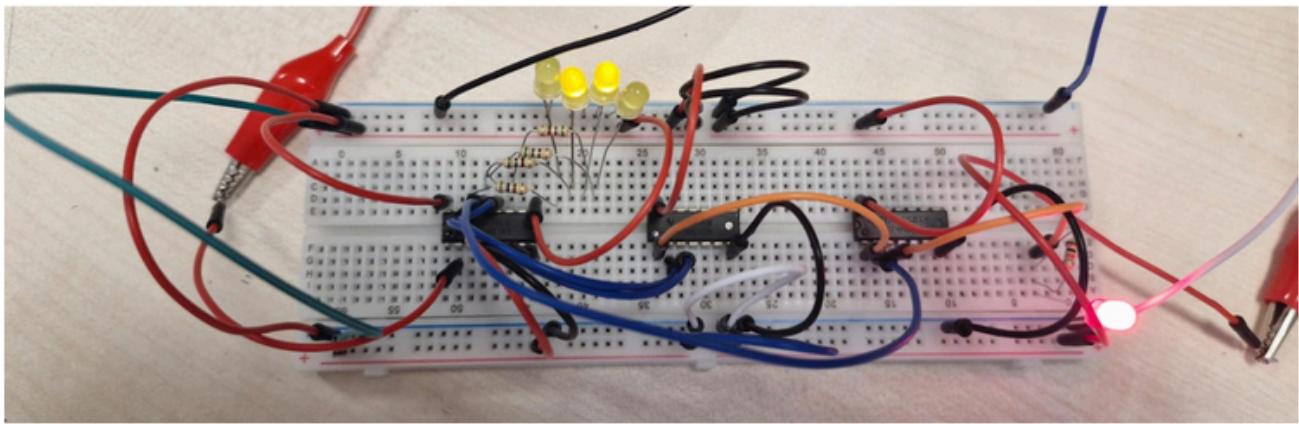


Figure 3.7: 0110, R=1 (LED is on), Q0=1, Q1=1, Q2=0

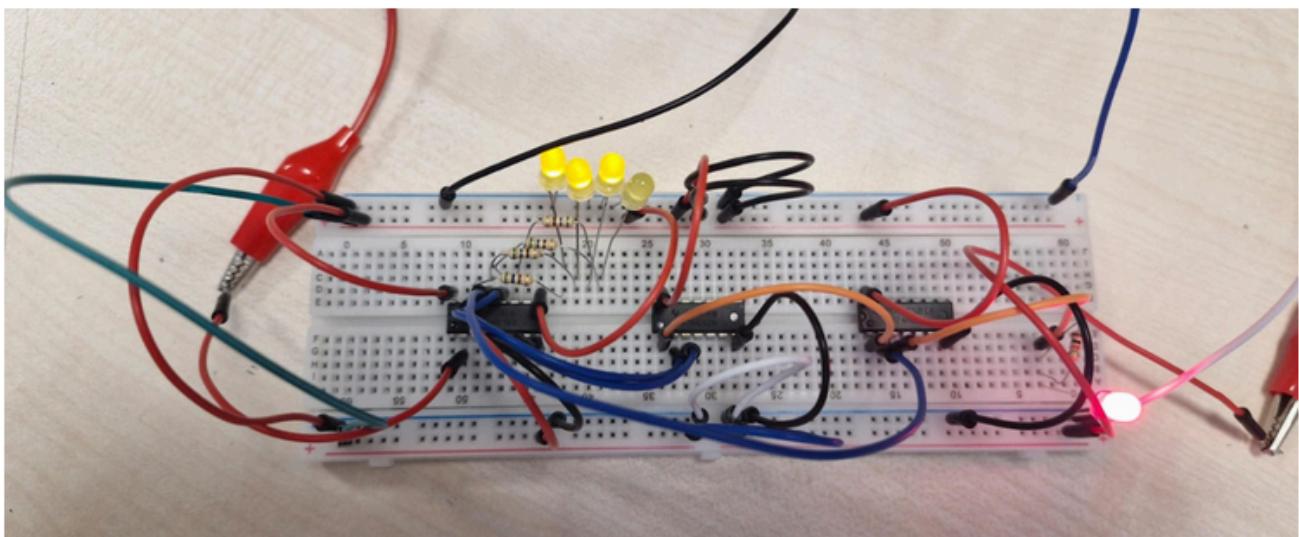


Figure 3.8: 0111, R=1 (LED is on), Q0=1, Q1=1, Q2=1

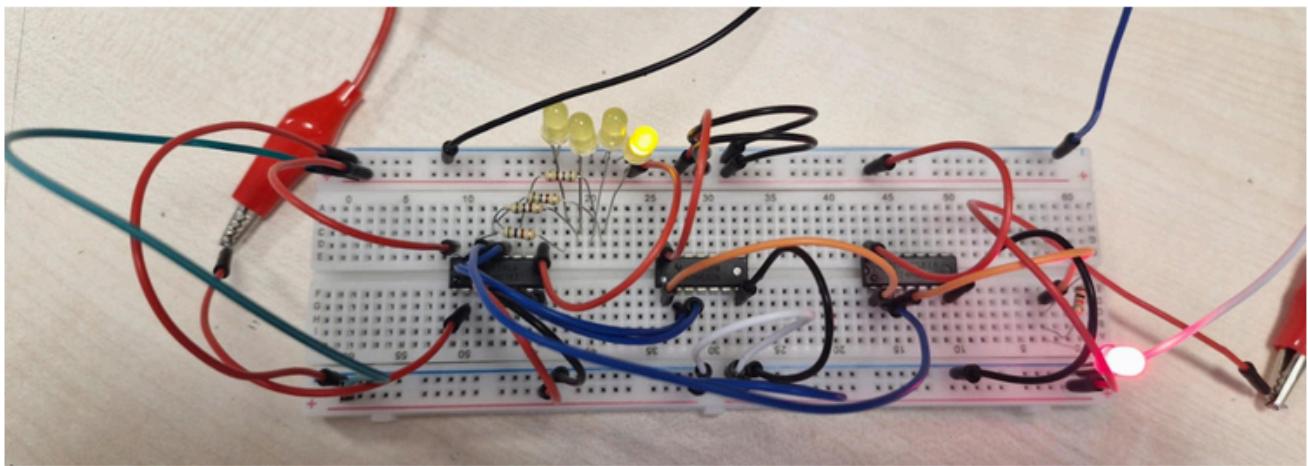


Figure 3.9: 1000, R=1 (LED is on), Q0=0, Q1=0, Q2=0

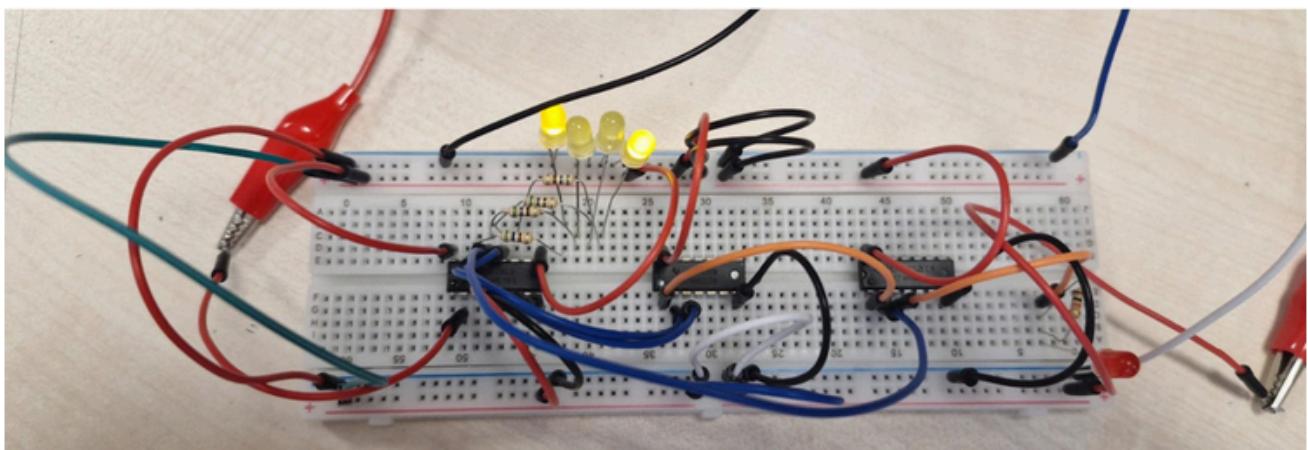


Figure 3.10: 1001, R=0 (LED is off), Q0=0, Q1=0, Q2=1

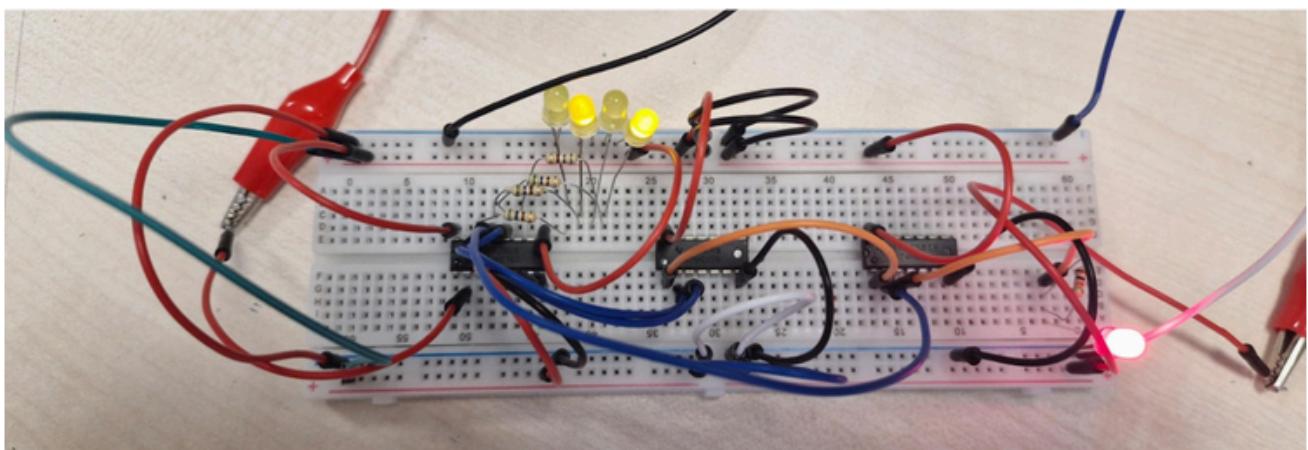


Figure 3.11: 1010, R=1 (LED is on), Q0=0, Q1=1, Q2=0

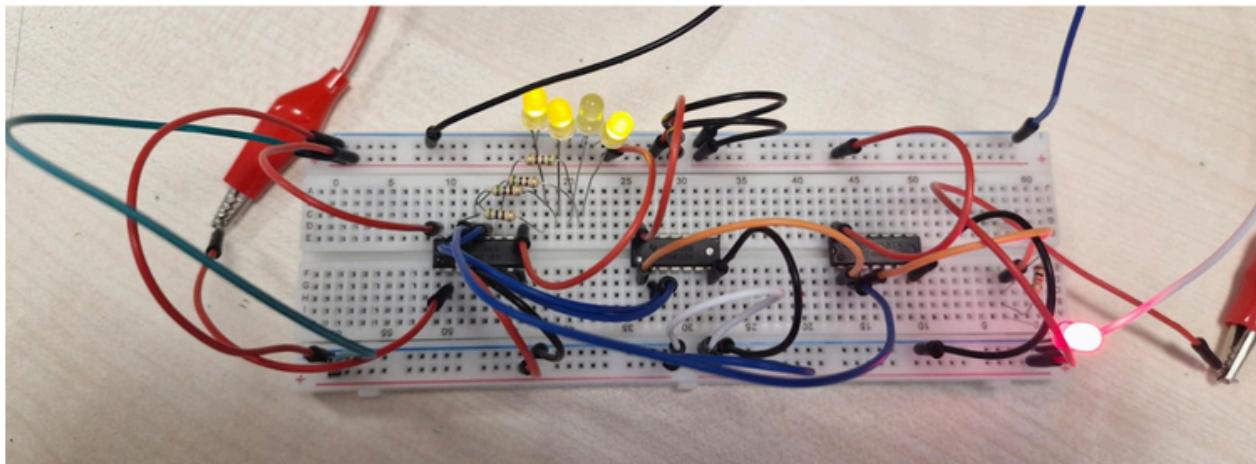


Figure 3.12: 1011, R=1 (LED is on), Q0=0, Q1=1, Q2=1

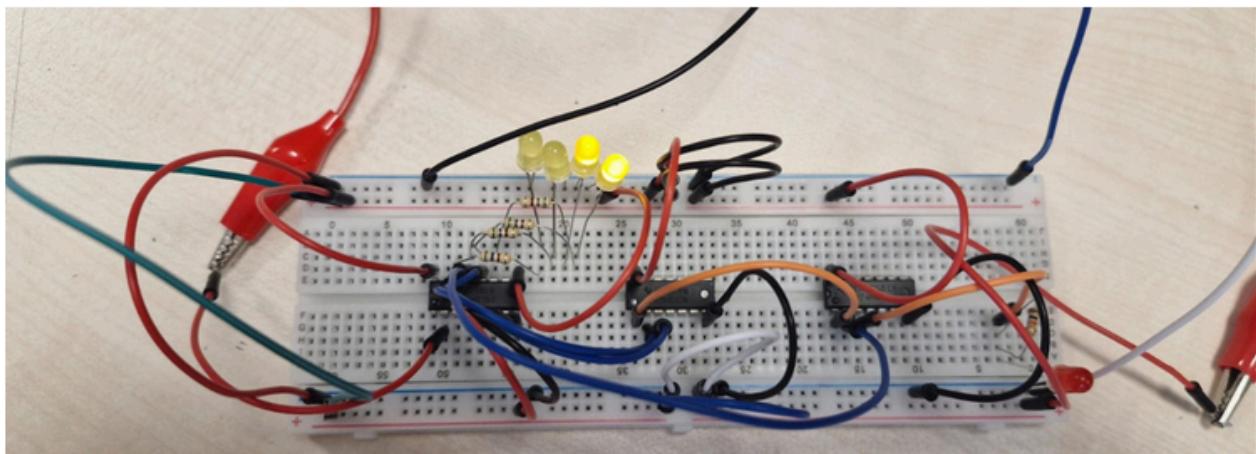


Figure 3.13: 1100, R=0 (LED is off), Q0=1, Q1=0, Q2=0

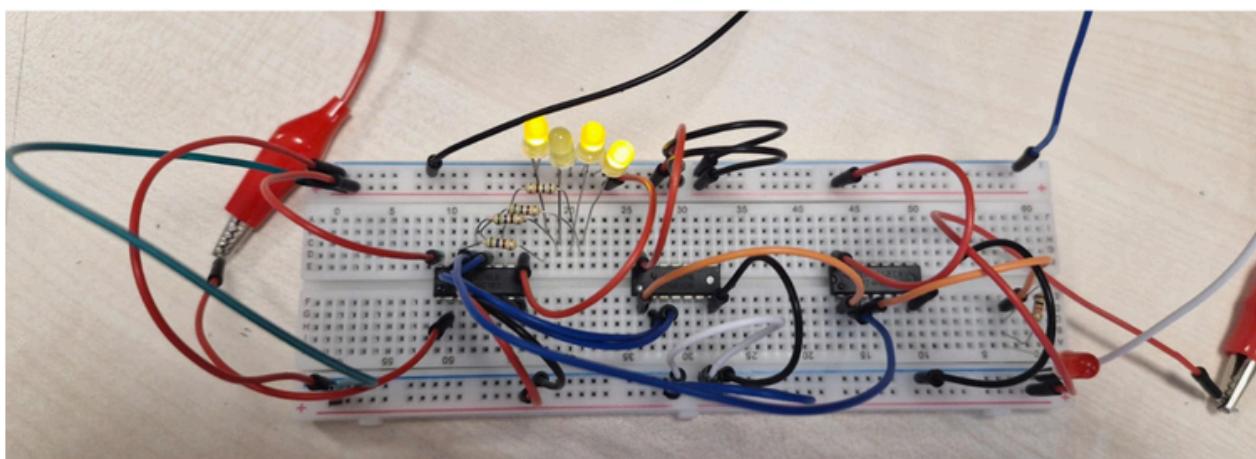


Figure 3.14: 1101, R=0 (LED is off), Q0=1, Q1=0, Q2=1

Zaňyapan 12

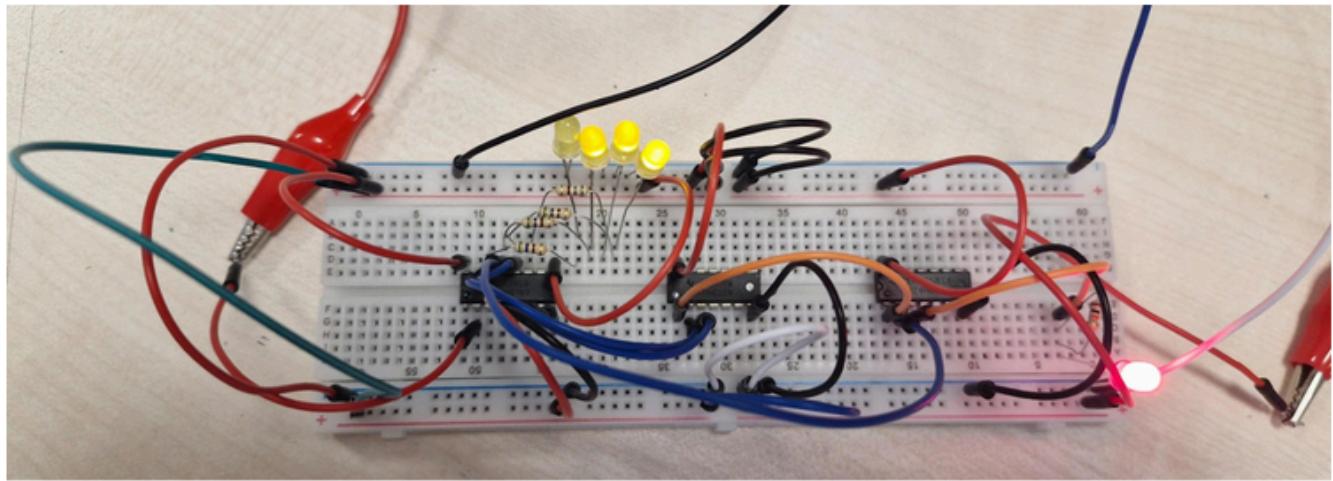


Figure 3.15: 1110, R=1 (LED is on), Q0=1, Q1=1, Q2=0

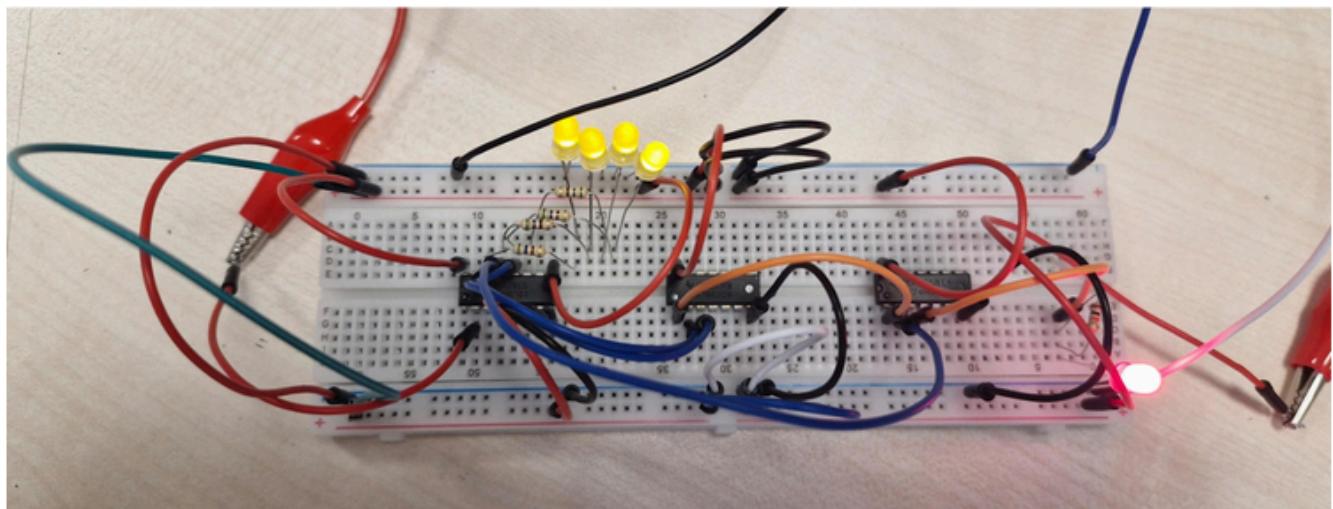


Figure 3.16: 1111, R=1 (LED is on), Q0=1, Q1=1, Q2=1



Figure 3.17: Waveform on the oscilloscope

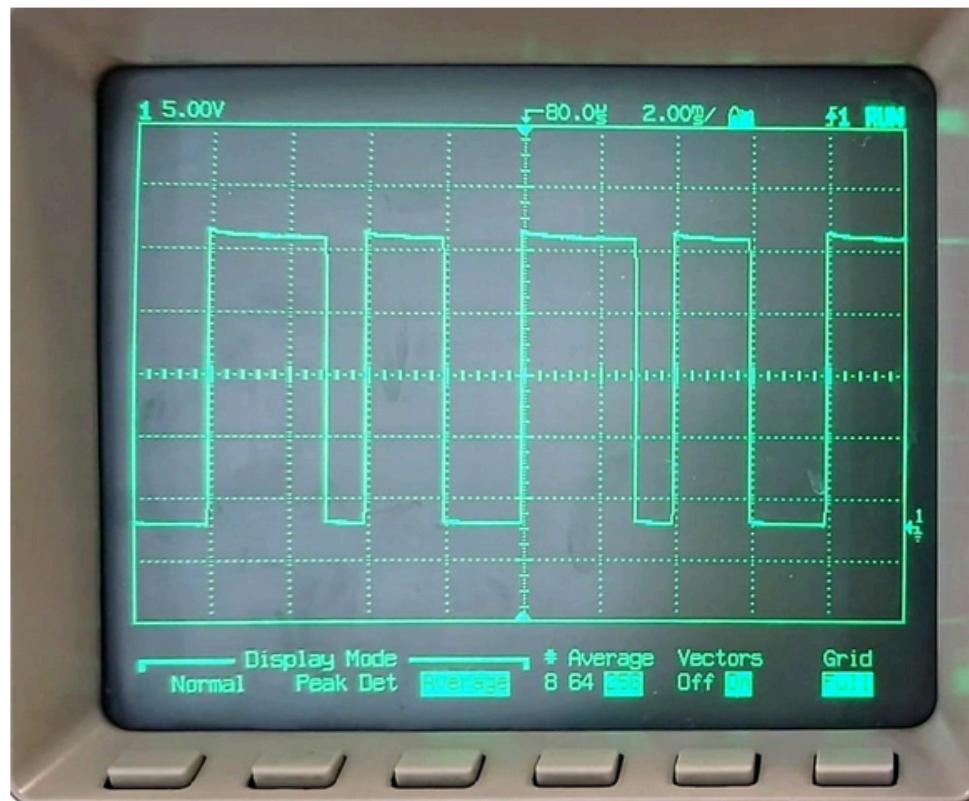


Figure 3.18: Waveform on the oscilloscope (close up)

CONCLUSION

The objective of this experiment was to show how integrated circuits, specifically circuits that included a 74HC163 synchronous counter and 74HC02N NOR and 74HC32N OR gates, can be combined to implement a defined logic function. There was no fixed value to compare my values with, and this setup was designed to show a pattern rather than a single fixed numeric value. Therefore, the most effective way to confirm correct operation was by comparing the observed outputs to the logic function's truth table, which was fully satisfied by the outputs of the LEDs and the waveform produced by the oscilloscope.

Works Cited

74HC02; 74HCT02 Quad 2-input NOR gate. (2008, September 18).

<https://www.alldatasheet.com/datasheet-pdf/view/255270/NXP/74HC02N.html>

74HC163PW (Presetable synchronous 4-bit binary counter; synchronous reset). *Nexperia.*

(2018, October 12.). Retrieved February 25, 2025, from

<https://www.nexperia.com/product/74HC163PW>

74HC32; 74HCT32 Quad 2-input OR gate. (2012, September 4).

<https://www.alldatasheet.com/datasheet-pdf/view/536726/PHILIPS/74HC32N.html>