Total points: 40

Computer Architecture Mid Term

Form description

i. Assume we have a processor having 64 instructions and 16 addressing modes. The memory interfaced with this processor is 16 K. Assume machine code length is 24 bits. 2 points

- [x] Op-Code=6 bits, Mode field=4 bits, Address Field=14 bits
- [ ] Op-Code=1 bits, Mode field=9 bits, Address Field=14 bits
- [ ] Op-Code=2 bits, Mode field=8 bits, Address Field=14 bits
- [ ] Op-Code=7 bits, Mode field=3 bits, Address Field=14 bits

ii. The machine code of ISZ instruction having Op-Code 110 in the direct and Indirect addressing mode respectively are (Answer in Hexadecimal number system): 2 points

- [ ] EXXX and 6XXX
- [ ] 6XXX and DXXX
- [x] 6XXX and EXXX
- [ ] 6XXX and FXXX

iii. The machine code of INC instruction in the basic computer assuming its micro-operation in RTL is given as rB7:AC ← AC+1 : 2 points

- [ ] 7100
- [x] 7080
- [ ] 7040

F040

iv. The machine code of INP instruction in the basic computer assuming its micro-operation in RTL is given as pB10:AC(0-7) ← INPR is: 2 points

F800

F400

7800

7400

v. Assume bus is designed using MUX for 8 registers of 16 bit each. The number and size of MUX used in the design will be: 2 points

No of Mux= 8 ; Size of MUX= 8x1

No of Mux= 8 ; Size of MUX= 16x1

No of Mux= 16 ; Size of MUX= 16x1

No of Mux= 16 ; Size of MUX= 8x1

vi. Assume following micro-operation is designed in the CPU:D2T4: IF (AC < 0), then DR ← DR+1Increment Control input of the DR register will be "1" when: 2 points

An instruction having op-code=000 will go in T3 timing signal

An instruction having op-code=001 will go in T4 timing signal

An instruction having op-code=010 will go in T3 timing signal

An instruction having op-code=010 will go in T4 timing signal

vii. Memory Reference (in the direct addressing mode) instructions' execution is started in -------- and register reference instructions' execution is started in -------- in the CPU designed in chapter 5. 2 points

T4 and T3

T4 and T4

- T3 and T3
- T3 and T4

viii. Assume op-codes “001” through “111” are assigned to 7 Memory Reference instructions. Op-code “000” is assigned to Non-Memory Reference instructions with Mode filed =0 for input-output instructions and Mode field=1 for register reference instructions. The control variables D0=1 and I=1 will be for the following type of instructions: 2 points

- Memory Reference in the Direct Addressing Mode
- Memory Reference in the Indirect Addressing Mode
- **Register Reference Instructions**
- Input Output Instructions

ix. RTL “D5T4:M[AR] ←AC” is designed for the following instruction” 2 points

- Load instruction
- **Store instruction**
- BUN instruction
- BSA instruction

x. RTL “D5T4: if AC(15)=1 then PC←AR” is designed for the following instruction: 2 points

- BUN instruction
- BSA instruction
- **BNA (branch if negative AC) instruction**
- SNA (skip if negative AC) instruction

xi. RTL “D0T4: DR M[AR] ” followed by “D0T5: AC ← AC ∧ DR,SC← 0” is designed for the following instruction: 2 points

- OR instruction

- [x] AND instruction
- [ ] LDA instruction
- [ ] STA instruction

xii. RTL “rB10: if AC(15)=0 then PC←PC+1” is designed for the following instruction: 2 points

- [ ] BUN instruction
- [ ] BSA instruction
- [ ] SNA (skip if negative AC) instruction
- [x] SPA (skip if positive AC) instruction

xiii. Assume we have a 16-bit register. The range of signed data that can be stored in this register is: 2 points

- [ ] -128→127
- [ ] -256→255
- [ ] -32768→32768
- [x] -32768→32767

xiv. Following is not a type of micro-operation: 2 points

- [ ] Arithmetic
- [ ] Logic
- [ ] Register Transfer
- [x] Register Level

xv. RTL “rb7:AC← Shr AC, AC(15) ←E, E←AC(0)” is designed for the following instruction: 2 points

- [ ] ROR instruction having machine code=7080
- [ ] RCR instruction having machine code=7100

- ROR instruction having machine code=7100
- [x] RCR instruction having machine code=7080

xvi. Assume an instruction stored at address 040 (PC=040) has mode =1; opcode = 010 and address part=120. The value at 120 is 270. The value at 270 is 45AB. The initial value of AC=1234. Go over the instruction cycle and find out the contents of IR and AR registers at the end of T3 timing signal are: 2 points

- IR=A120,AR=120
- [x] IR=A120,AR=270
- IR=2120,AR=120
- IR=2120,AR=270

xvii. Assume an instruction stored at address 030 (PC=030) has mode =0; opcode = 001(ADD instruction) and address part=120. The value at 120 is 270. The value at 270 is 1234. The initial value of AC=1000. Go over the instruction cycle and find out the contents of AC and DR registers at the end of execution phase are: 2 points

- [x] AC=1270, DR=270
- AC=2234, DR=1234
- AC=1270, DR=1234
- AC=2234, DR=270

xviii. Assume an instruction stored at address 030 is CLA having micro-operation “rB11:AC 0”. Initial contents of AC are1234. Go over the instruction cycle and the contents of AC and PC registers at the end of execution phase are: 2 points

- AC=1234,PC=031
- AC=0000,PC=032
- AC=1234,PC=032
- AC=0000,PC=031

xix. Assume an instruction stored at address 040 (PC=040) has mode =1; opcode = 110 and address part=120. The value at 120 is 270. The value at 270 is 45AB. The initial value of AC=1234. The effective address in this case is: 2 points

- Effective Address=040
- Effective Address=120
- **Effective Address=270**
- Effective Address=5AB

xx. Assume Bus is designed in some CPU having four registers A,B,C and D of 16 bits each with the following configuration: S1S0=00 (Register A selected for the Bus); S1S0=01 (Register B selected for the Bus); S1S0=10 (Register C selected for the Bus) ; S1S0=11 (Register D selected for the Bus); What control variables should be active when MOV B,D instruction will be executed? 2 points

- **LD input of B register; S1S0=11**
- LD input of D register; S1S0=01
- LD input of B register; S1S0=01
- LD input of D register; S1S0=11