PIPELINE ARCHITECTURE

Legal Disclaimer

General Disclaimer:

FTC Disclaimer:

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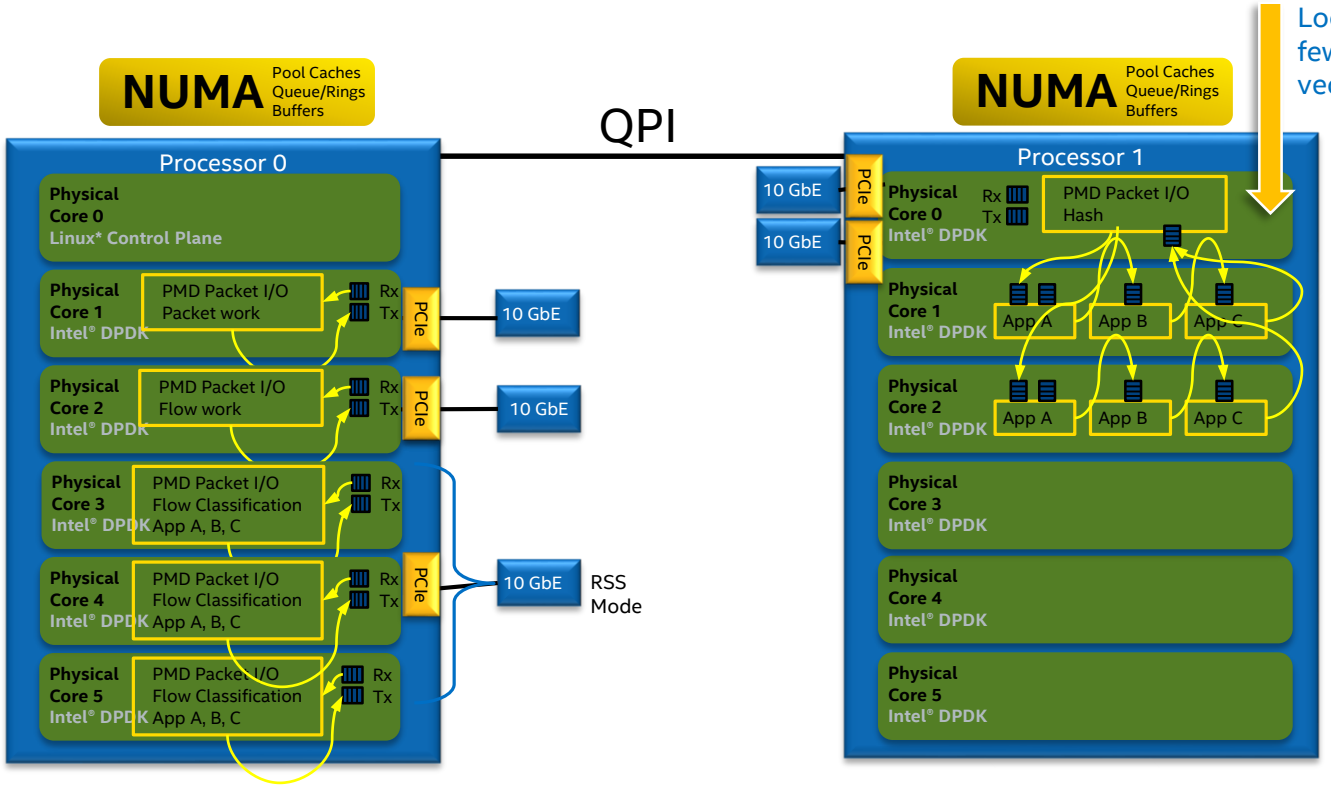
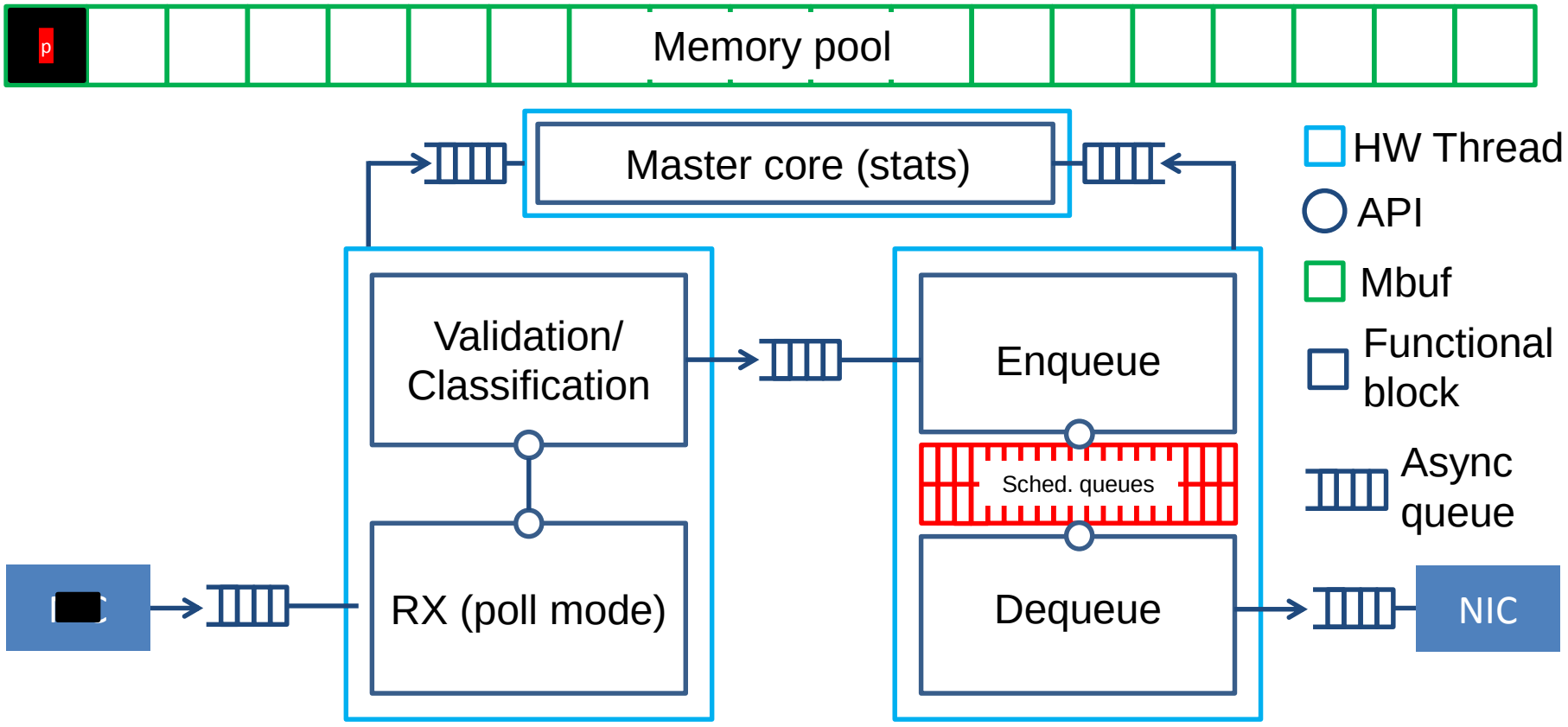
Run-to-completion vs pipeline software models



Run to Completion model
- I/O and Application workload can be handled on a single core
- I/O can be scaled over multiple cores

Pipeline model
- I/O application disperses packets to other cores
- Application work performed on other cores

Simple Pipeline application



Pipeline applications

DPDK Packet Framework

- development framework for building packet processing applications using standard pipeline blocks

DPPD: Data Plane Performance Demonstrators

- Linux user space applications based mainly intended for performance analysis purposes

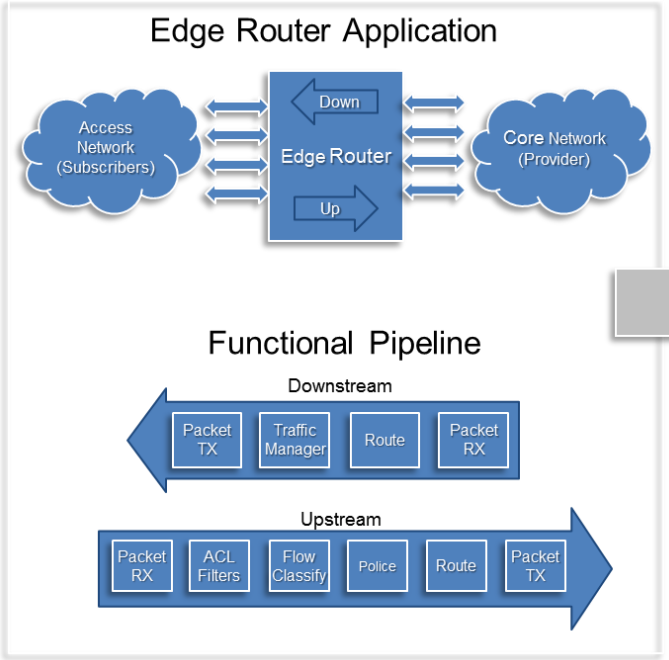
DPDK PACKET FRAMEWORK

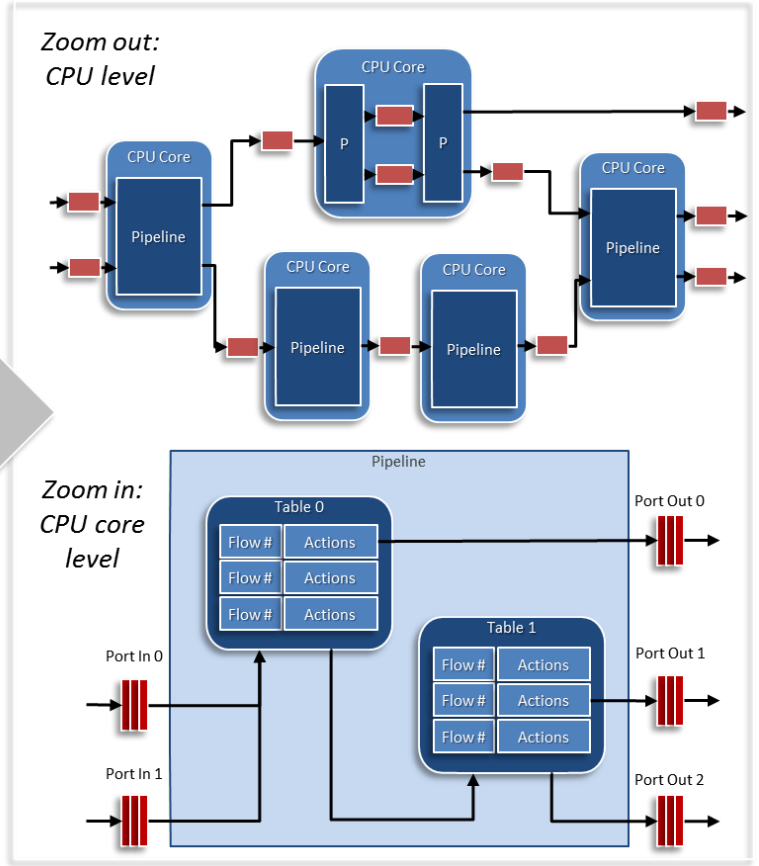
DPDK Programmer's Guide, Packet Framework

DPDK Sample Applications User Guide, Internet Protocol (IP) Pipeline Sample Application

Rapid Development of Packet Processing Apps

DPDK Packet Framework quickly turns requirements into code





Packet Framework Components

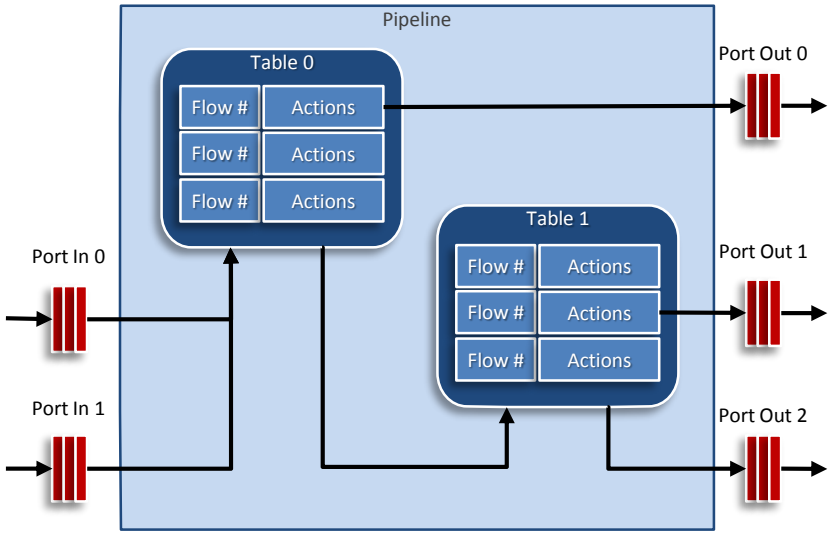
#	Component	
1	Port library	Port abstract interface API Basic ports: HWQ, SWQ Advanced ports: IP frag, IP ras, Traffic Mgr, KNI, QAT
2	Table library	Table abstract interface API Tables: Hash (Extendible bucket, LRU), ACL, LPM, Array
3	Pipeline library	Pipeline configuration and run-time API Configuration API implementation Run-time API implementation
4	IP Pipeline example	The Internet Protocol (IP) Pipeline application illustrates the use of the DPDK Packet Framework tool suite by implementing functional blocks such as packet RX, packet TX, flow classification, firewall, routing, IP fragmentation, IP reassembly, etc which are then assigned to different CPU cores and connected together to create complex multi-core applications.

DPDK Packet Framework, Pipeline Level

librte_port

Ports
HW queue
SW queue
IP Fragmentation
IP Reassembly
Traffic Mgr
KNI
Source/Sink

Zoom in: Pipeline level



librte_table

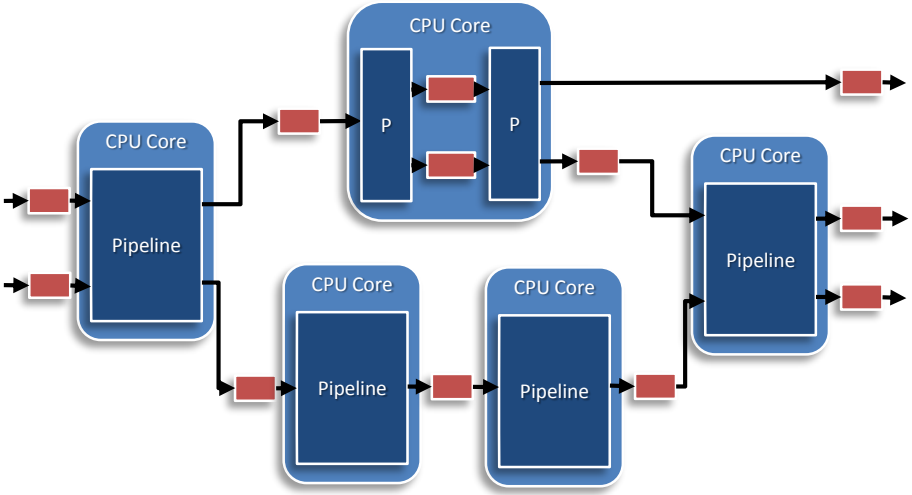
Tables
Exact Match / Hash
Access Control List (ACL)
Longest Prefix Match (LPM)
Array
Pattern Matching

Actions
Reserved actions: Send to port, Send to table, Drop
Packet edits: push/pop labels, modify headers (NAT, TTL update)
Flow-based: meter, stats, app ID
Accelerators: crypto, compress
Load Balancing

Standard methodology for ***pipeline*** development.
Ports and ***tables*** are connected together in tree-like topologies , with tables providing the ***actions*** to be executed on input packets.

DPDK Packet Framework, App Level

Zoom out: Multi-core application level



librte_pipeline

Pipelines
Packet I/O
Flow Classification
Firewall
Routing
Traffic Mgmt

The Framework breaks the app into multiple pipelines, assigns each pipeline to a specific core and chains the pipelines together

Multi-core scaling

A complex application is typically split across multiple cores, with cores communicating through SW queues

There is usually a performance limit on the number of table lookups and actions that can be fit on a single a single core (due to cache memory size, cache BW, memory BW, etc.)

The Framework breaks the app into multiple pipelines, assigns each pipeline to a specific core and chains pipelines together

One core can do more than one pipeline, but a pipeline cannot be split across multiple cores

INTEL® DATA PLANE PERFORMANCE DEMONSTRATORS

https://01.org/intel-data-plane-performance-demonstrators

Intel® DPPD: Data Plane Performance Demonstrators

An open source application

- BSD3C license

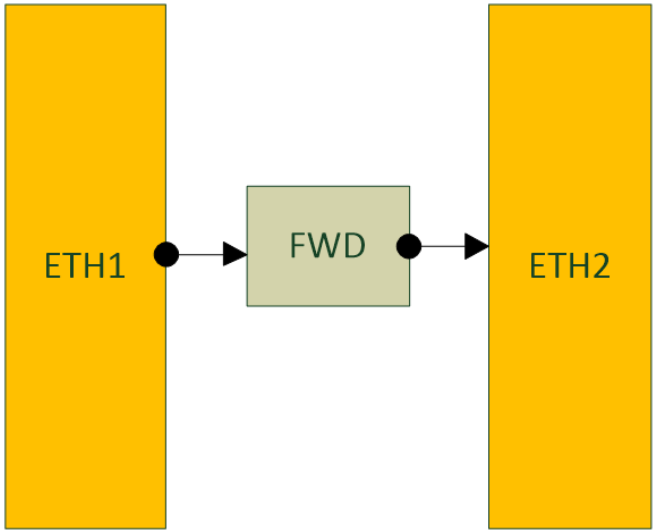
Config file defines

- Which cores are used
- Which interfaces are used
- Which tasks are executed and how configured

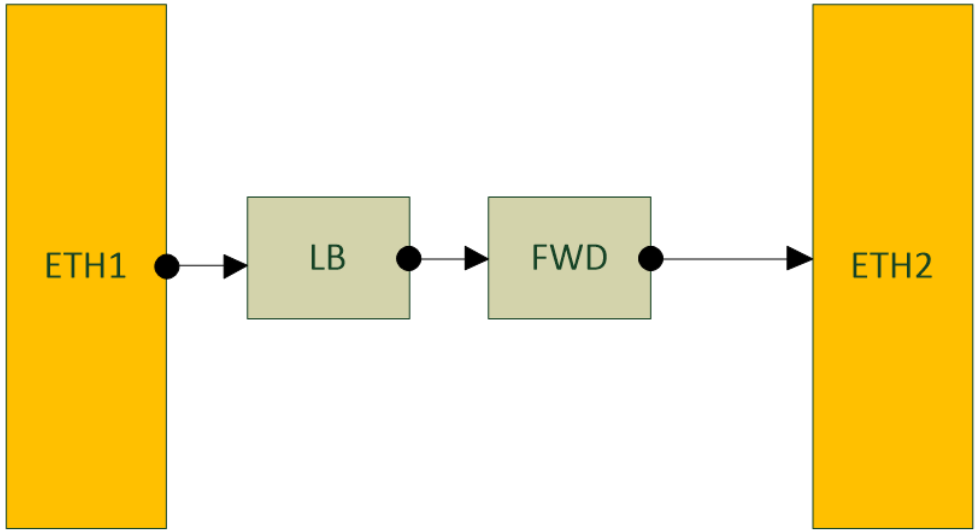
Allows to

- Find bottlenecks and measure performance
- Try and compare different core layouts without changing code
- Reuse config file on different systems (CPUs, hyper-threads, sockets, interfaces)

DPPD: Sample Configurations

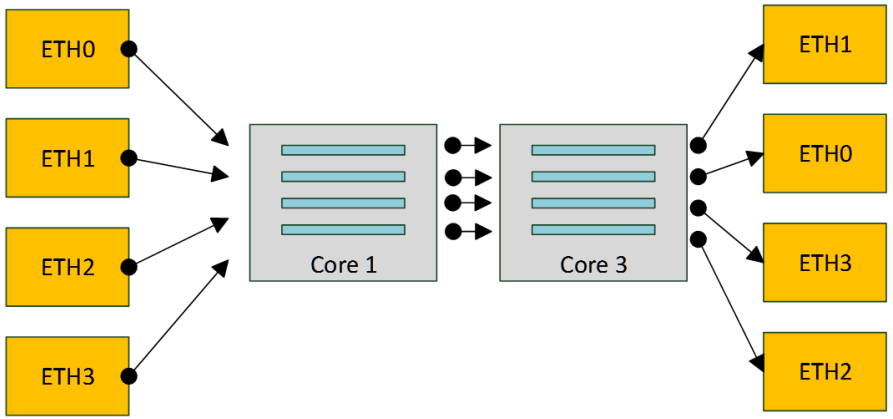


Very simple port forwarding



Simple load balancer and worker thread

Finding bottlenecks



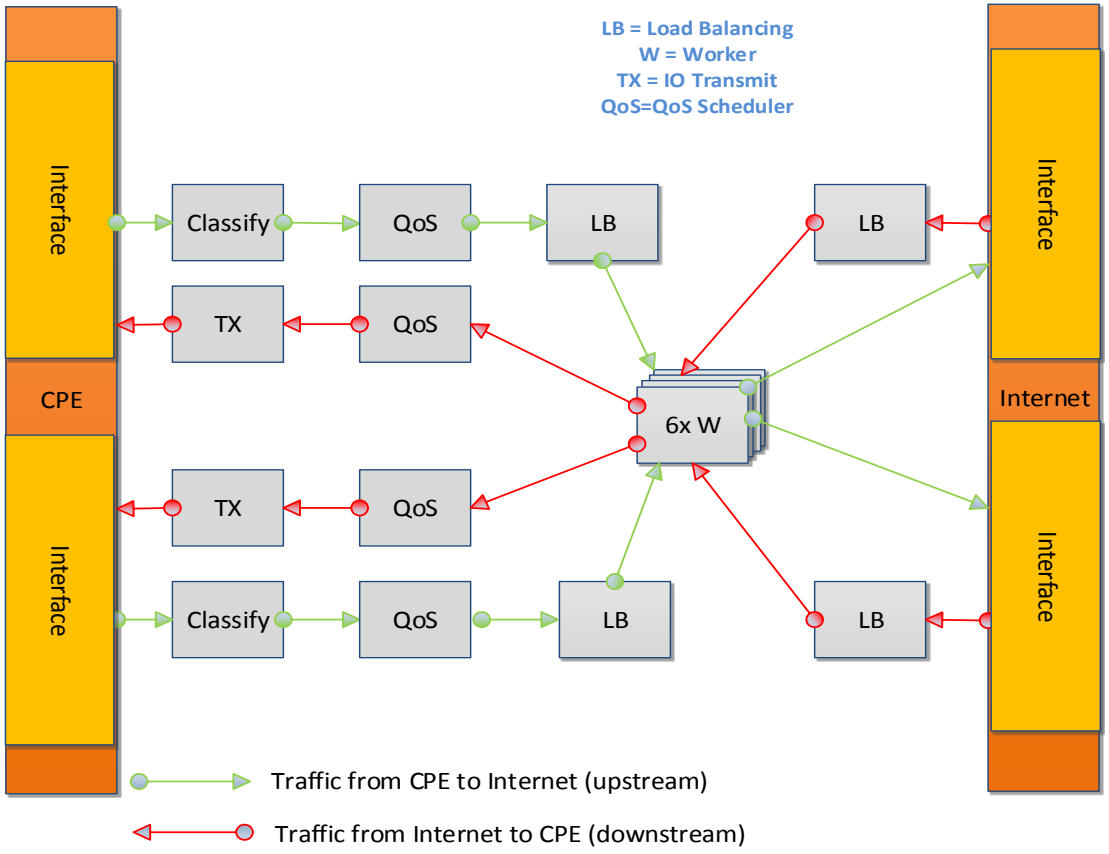
Time: 34 %: 98.7418
Rx: 52159680 pps (52143267 avg)
Tx: 51315065 pps (51539278 avg)

DPPD v0.12: Receive-Transmit (4x)

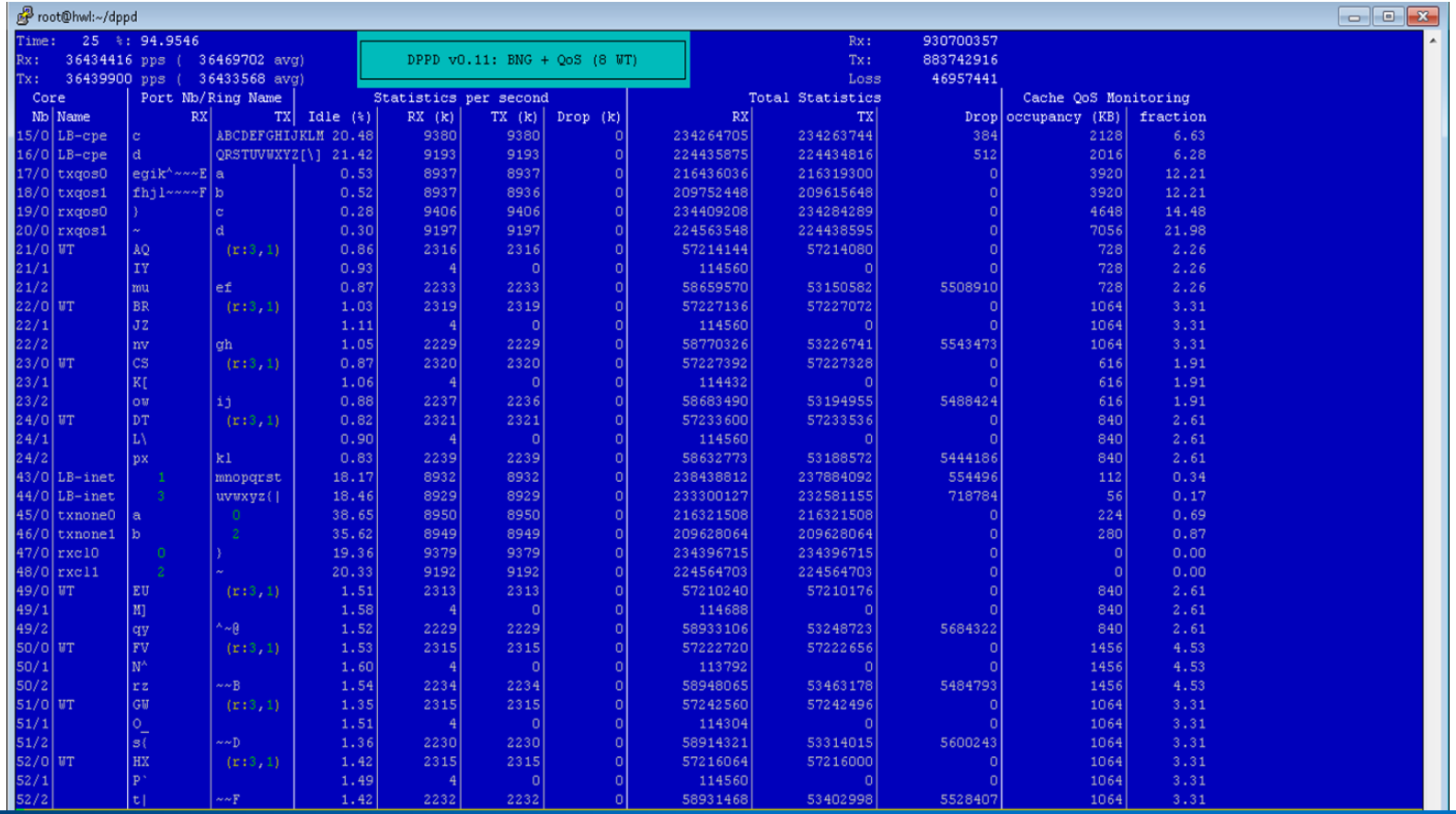
Rx: 1744146352
Tx: 1722201805
Loss 21944547

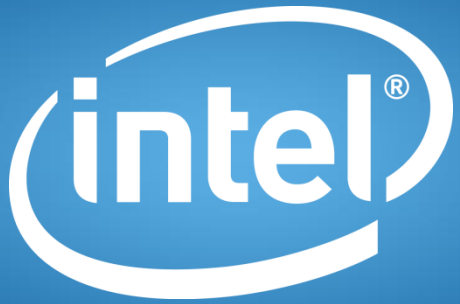
Core		Port Nb/Ring Name		Statistics per second				Total Statistics		
Nb	Name	RX	TX	Idle (%)	RX (k)	TX (k)	Drop (k)	RX	TX	Drop
1/0	RX	0	A	0.12	13058	12815	242	440222864	435080482	5142382
1/1		1	B	0.12	13058	12815	242	437906292	432765762	5140530
1/2		2	C	0.12	13021	12815	205	439244652	432628611	6616041
1/3		3	D	0.12	13021	12815	205	426772544	421688092	5084452
3/0	TX	A	1	0.00	12828	12828	0	435090172	435090172	0
3/1		B	0	0.00	12828	12828	0	432775474	432775474	0
3/2		C	3	0.00	12828	12828	0	432638328	432638328	0
3/3		D	2	0.00	12828	12828	0	421697831	421697831	0

QoS and BNG(simplified view)



DPPD Display

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