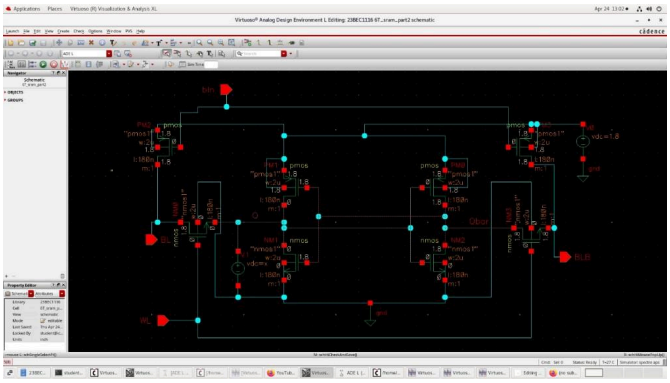
DESIGN AND SIMULATION

- Utilized Cadence Virtuoso for schematic design and simulation of each SRAM topology.
- Performed DC analysis to determine SNM using the butterfly curve method.
- Conducted transient simulations to assess dynamic power consumption during read/write operations.

1) 6T SRAM:

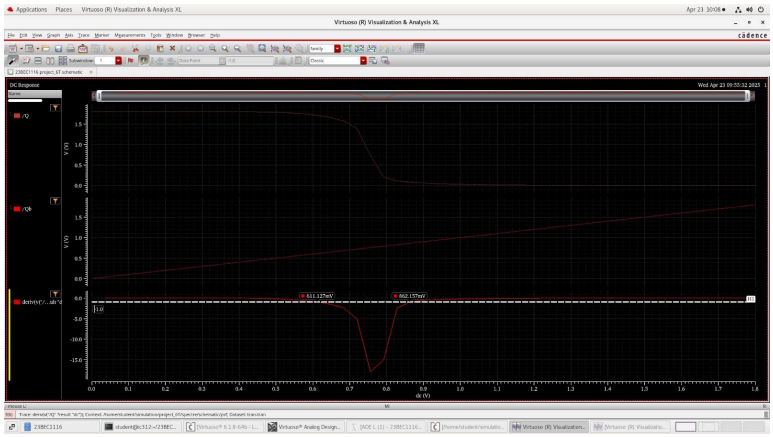
1.1) CIRCUIT:



Schematic structure:

- Two **cross-coupled inverters** formed by **M1-M4** (2 PMOS and 2 NMOS).
- Two **access NMOS transistors** (M5, M6) controlled by the **word line (WL)**.
- **Bit lines**: `BL` and `BLB` are used for read/write.
- VDD = 1.8V and GND lines are defined.
- Proper node labeling (`Q`, `Qbar`, WL, BL, BLB) helps with analysis.

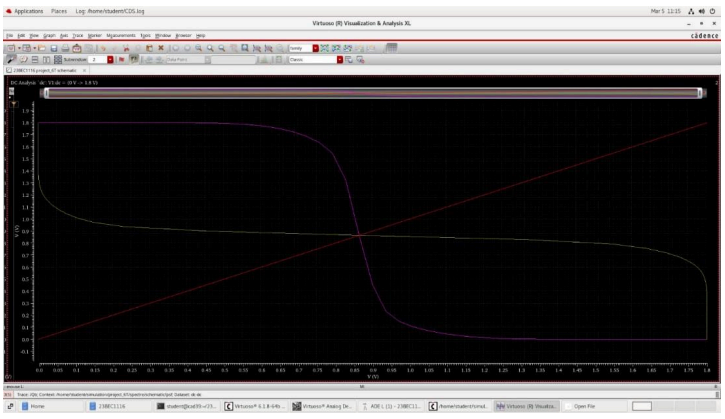
1.2) DC CURVE:



This DC curve represents the **Voltage Transfer Characteristic (VTC)** of the SRAM cell:

- Likely sweeping input voltage at one node (say `Q`) and plotting the voltages at `Q` and `Qbar`.
- Cross point (where V(Q) = V(Qbar)) indicates the **trip point**.
- This curve helps verify **bistability** — two stable states.

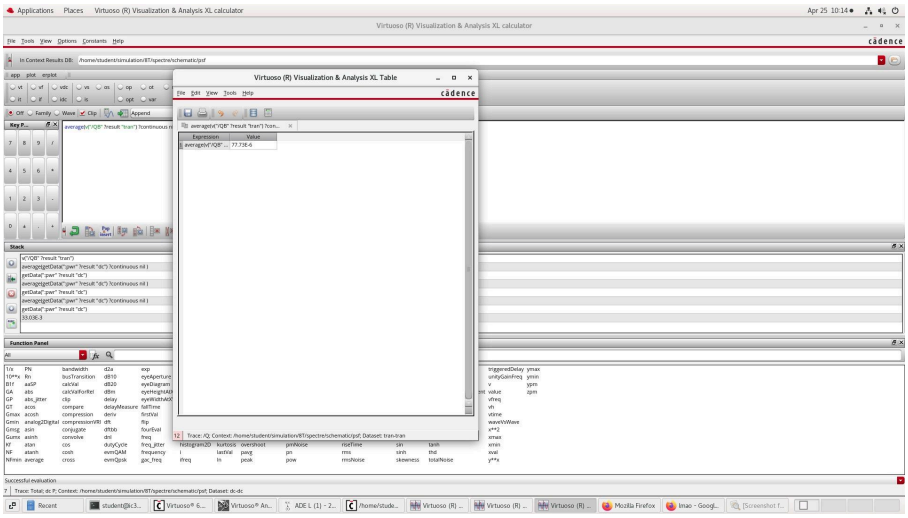
1.3) BUTTERFLY CURVE:



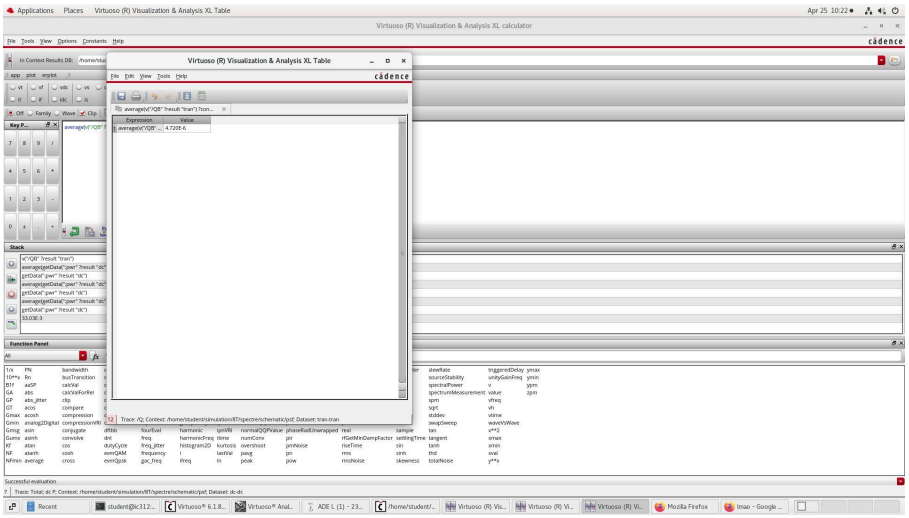
This is the **Static Noise Margin (SNM) analysis**:

- Generated by superimposing the VTC of the two cross-coupled inverters, one flipped horizontally.
- The largest square that can fit between the two curves represents **SNM**.
- Bigger square = **more robust SRAM cell**.

1.4) Trans Power

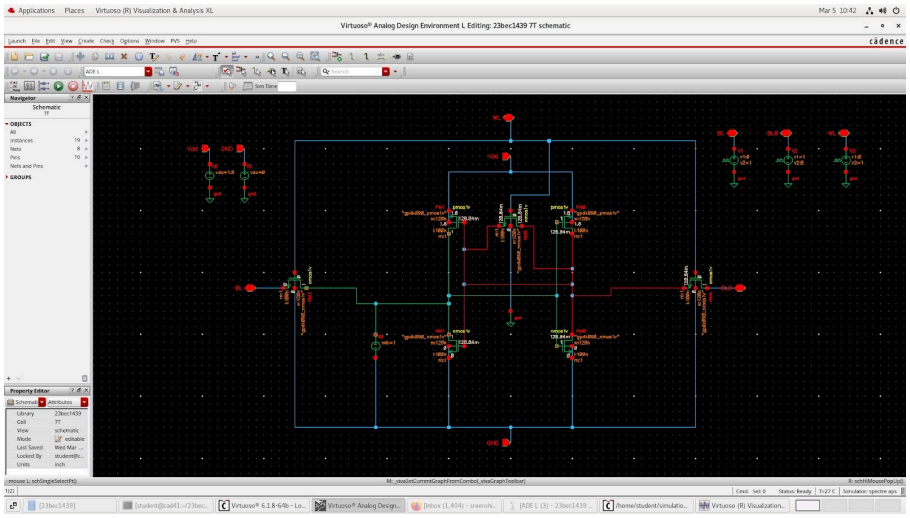


1.5) DC Power



2) 7T SRAM:

2.1) CIRCUIT:



Schematic structure:

- Two cross-coupled inverters formed by **M1-M4** (2 PMOS and 2 NMOS) store the data (like in 6T).
- **One additional NMOS transistor (M7)** is inserted between the inverter loop and GND to improve read stability or isolate during read operation.
- **Two access NMOS transistors (M5, M6)** for **write and read** operations.
  - **M5** is controlled by **WLwrite**, connected to **BL**. ○ **M6** is

controlled by **WLread**, connected to **a read bitline (RBL) 2.2) DC**

CURVE AND POWER:

Top-left: Power Dissipation vs Input Voltage

- Shows **power peak** around mid-supply (0.9V), where both pull-up and pull-down paths can conduct.
- Used to estimate **static power dissipation**.

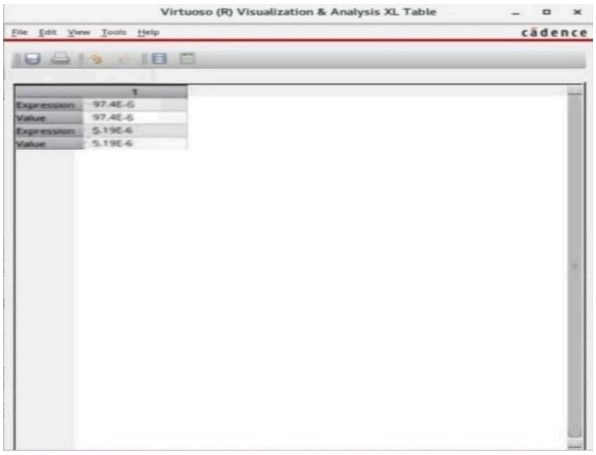
Top-right: Butterfly Curve & DC Transfer Characteristics

- This combines:
  - Inverter VTCs (forward and mirrored) – used for **SNM**.
  - Qbar, Q, and n2 voltages shown — confirms **bistability**. • Ideal butterfly shape = symmetric = robust.

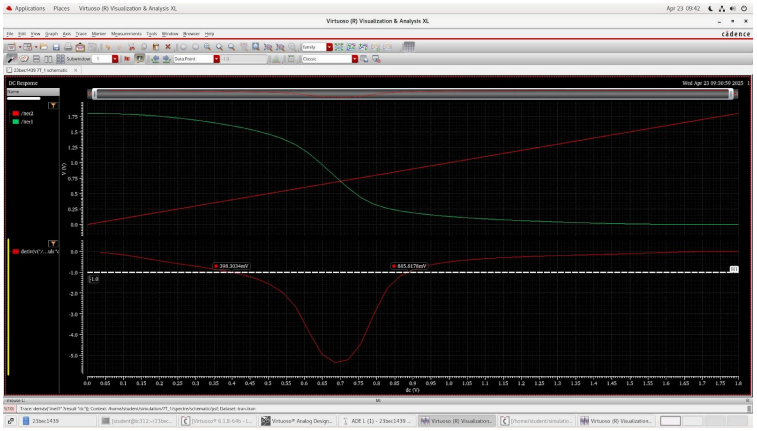
Bottom-left: Voltage Transfer Curve

- Standard inverter response.
- Helps analyze **trip point** and VTC slope.

2.3) POWER TABLE:



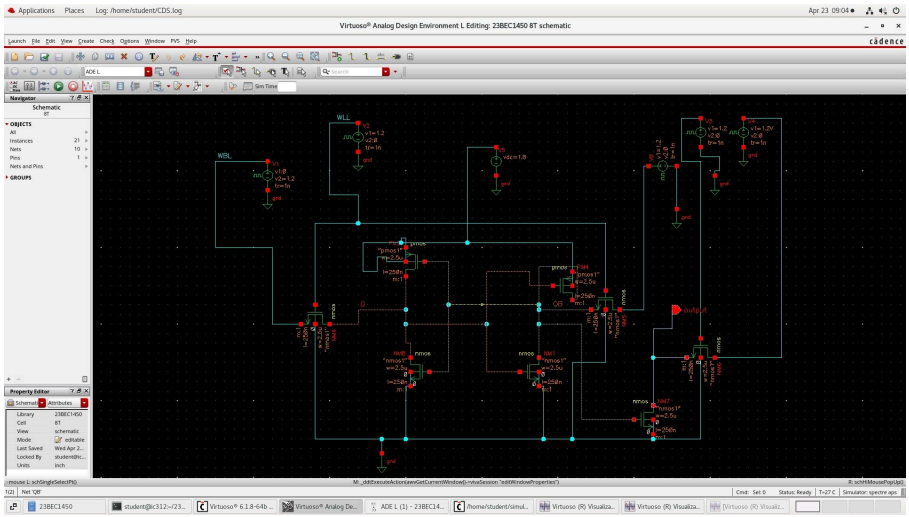
2.4) SNM:



- **Red Curve** - Voltage transfer characteristic in **hold mode**.
- **Green Curve** - Voltage transfer characteristic in **read mode**.
- **X-axis** - Voltage (V) ranging from **0 to 2.0V**.
- **Y-axis** - Voltage (V) ranging from **-1.0 to 2.0V**.
- The **intersection points** of the curves indicate the **stability points** of the SRAM cell.
- The **SNM value** is determined by the **largest square** that fits between the curves—this represents the **maximum noise voltage** the SRAM cell can tolerate **without flipping its state**.

3) 8T SRAM:

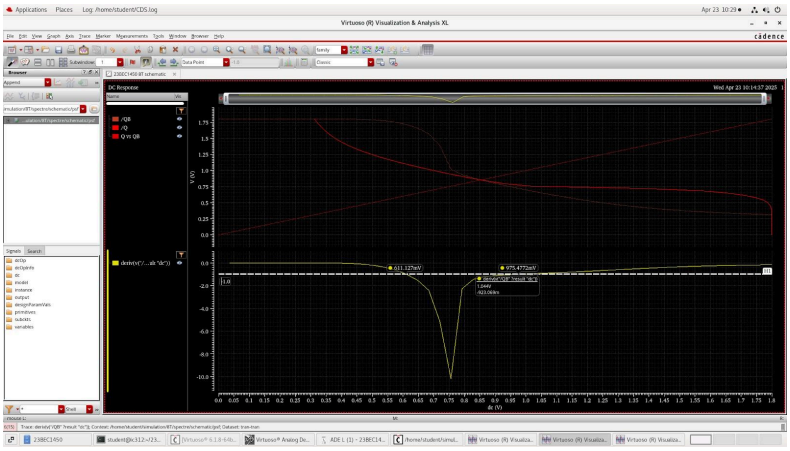
3.1) CIRCUIT:



Schematic structure:

- Two cross-coupled inverters formed by **M1-M4** (2 PMOS and 2 NMOS) for data storage.
- Two access NMOS transistors:
  - **M5** for **write** access (controlled by **WL**, connected to BL).
  - **M6, M7** form a **read buffer** stage to isolate the internal node during a read.
    - **M6** connects storage node to the gate of **M7**.
    - **M7** is a read pass transistor connected to **RBL**, controlled by **RWL (Read Word Line)**.
- **M8** is a pull-down NMOS to discharge RBL during read (optional depending on design style).

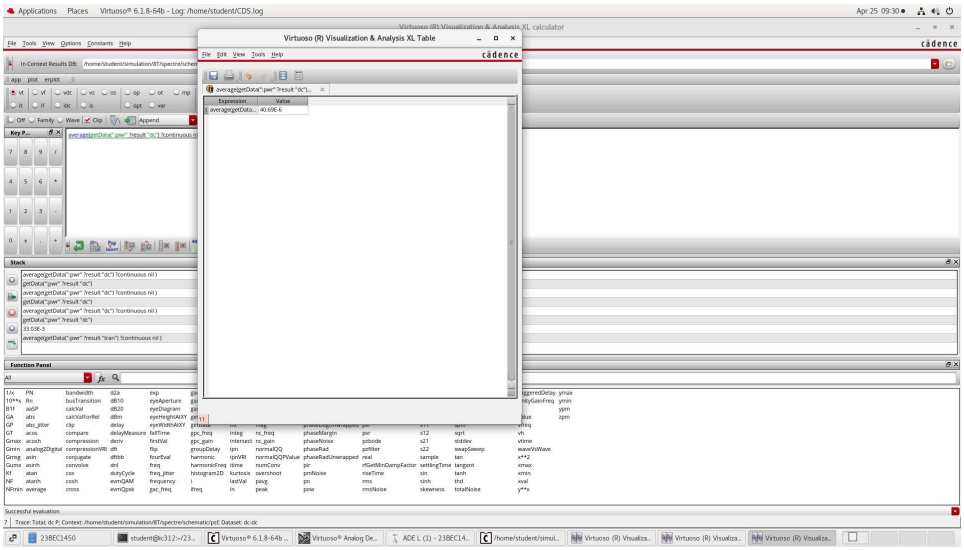
3.2) DC CURVE:



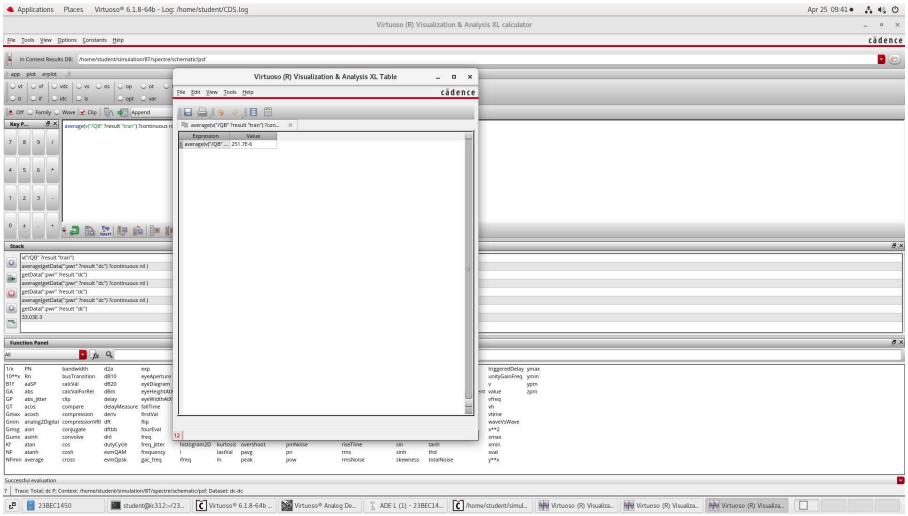
- **Red Curves** - Voltage Transfer Characteristics (VTC) of the SRAM cell.
- **Yellow Curve** - Derivative of the voltage transfer characteristics (**dV/dV**).
- **White Dashed Line** - Indicates the **SNM value**, which determi
- nes the stability of the SRAM cell.
- **Annotated Points**:

- **611.127mV** (likely a key stability point).
- **975.477mV** (another critical voltage level).

3.3) DC Power

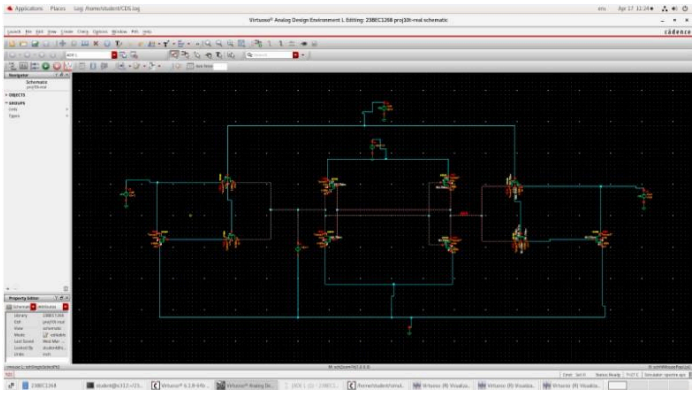


3.4) Transient Power



4) 10T SRAM

4.1) CIRCUIT:

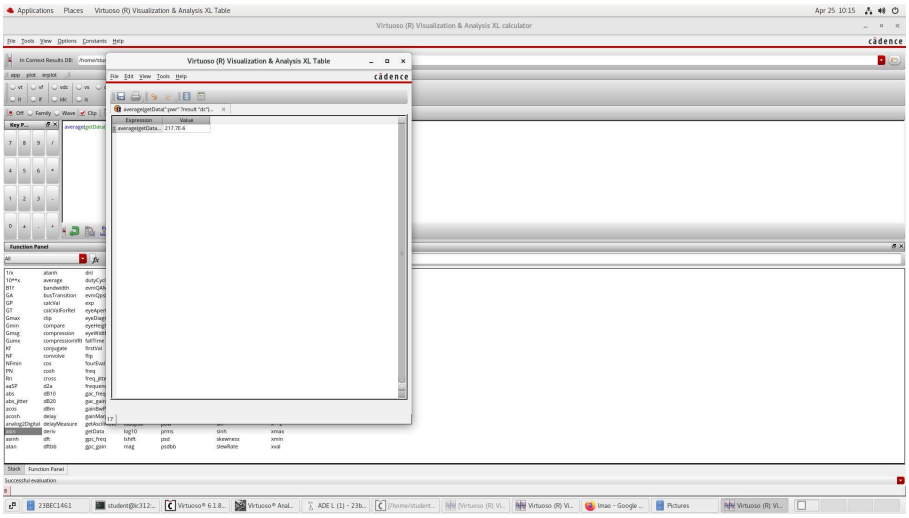


Schematic structure:

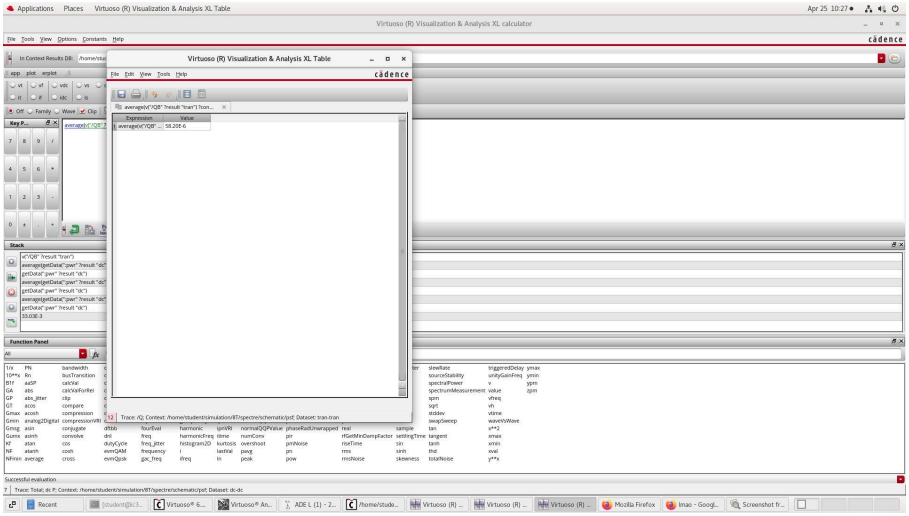
- Two cross-coupled inverters using **M1-M4** (PMOS and NMOS).
- Write path:
  - **M5, M6** NMOS access transistors (controlled by **WWL**) connected to **WBL** and **WBLB**.
- Read path:
  - **M7–M10** form a **fully differential read buffer**:
    - Separate **read word line (RWL)** controls **M7, M8**.
    - **M9, M10** act as the differential read load.
      - Provides improved read SNM and eliminates read disturbance.

4.2) DC CURVE:

4.3) Transient power

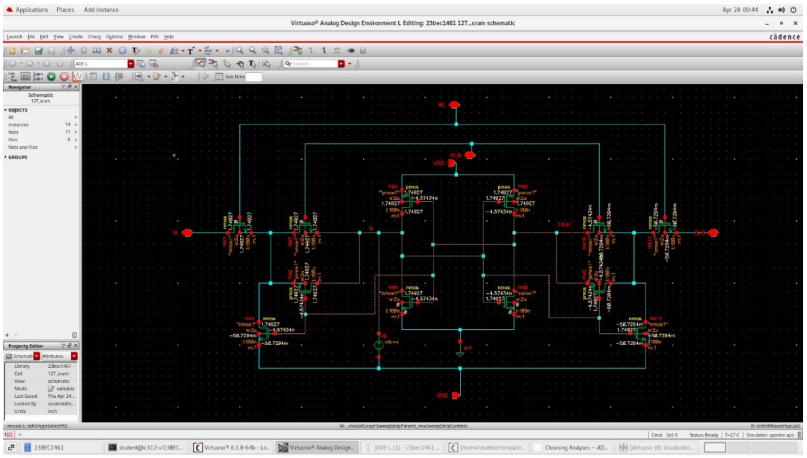


4.4) DC power



5) 12T SRAM:

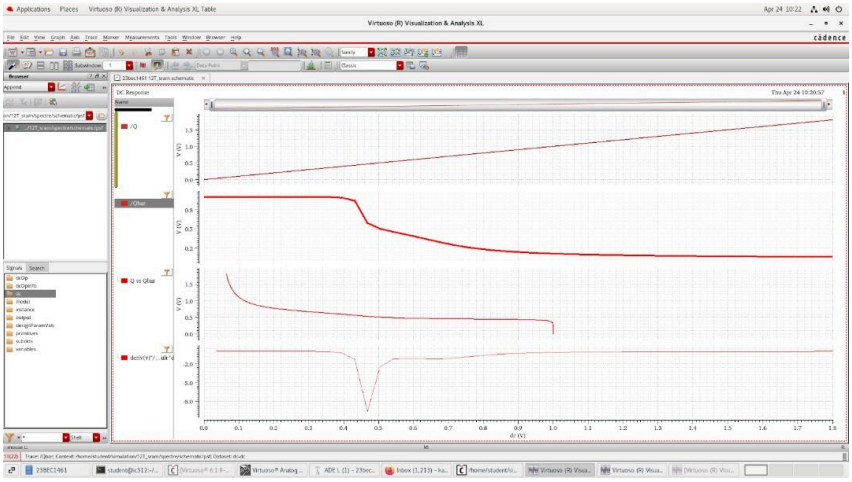
5.1) CIRCUIT:



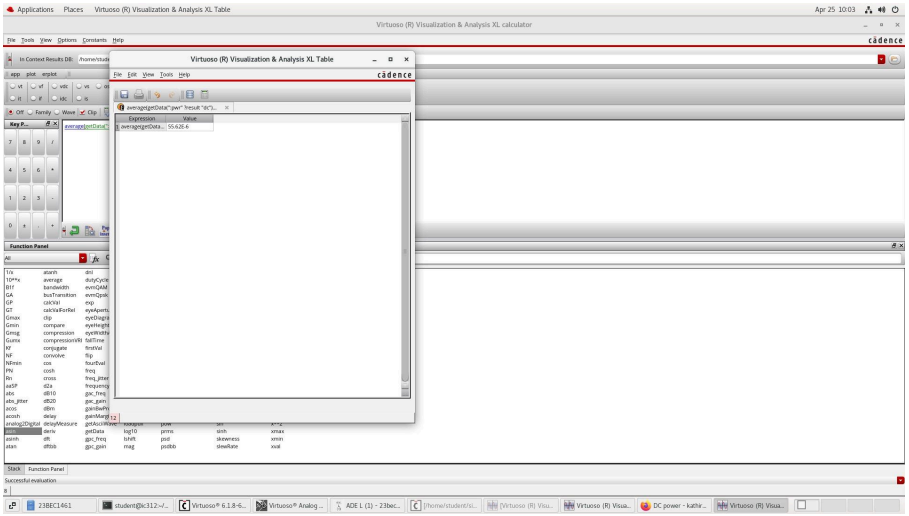
Schematic structure:

- Storage via two cross-coupled inverters: **M1–M4**.
- **Read and Write are completely decoupled.**
- **Write path:**
  - NMOS pass gates **M5, M6** (controlled by **WWL**) connected to **WBL, WBLB**.
- **Read path:**
  - Buffer stage (typically 4 transistors: **M7–M10**) similar to sense amplifier, with **M7, M8** controlled by **RWL**.
  - **M11, M12** as pull-down or pull-up transistors in read path (can be asymmetric depending on optimization).

5.2) SNM:



5.3) DC Power



5.5) Transient Power