Fully Integrated UWB Impulse Transmitter and 402-to-405MHz Super-regenerative Receiver for Medical Implant Devices

M. Anis[1] , M. Ortmanns[1] , N. Wehn[2]
[1] Institute of Microelectronics, University of Ulm, 89081 Ulm, Germany
[2]Microelectronic Systems Design Research Group, University of Kaiserslautern, 67663 Kaiserslautern, Germany
{syed.anis, maurits.ortmanns } @ uni-ulm.de , wehn @ eit.uni-kl.de

Abstract— **This paper proposes a multi-standard transceiver architecture, based on UWB impulse transmitter and 402-to-405MHz super-regenerative receiver for medical implant devices. This architecture eliminates the requirement of frequency synthesizer and power amplifier at transmitter side and LNA, mixers, IF amplifiers and ADCs at receiver side of implant transceiver. The test structure of transceiver has been implemented on 0.18µm CMOS technology. The UWB impulse transmitter consumes 0.3mW from 1.5V supply at the data rate of 500Kbits/s. The 402-to-405MHz super-regenerative receiver consumes 0.5mW at the data rate of 120Kbits/s and sensitivity of -95dBm.**

Index Terms — Low power, MICS band, UWB, super-regenerative receiver, UWB transmitter, LC oscillator.

I. Introduction

Implant ultralow power radio technology for in-body communication systems is one of the most active areas of research at academic and industrial level. High performance wireless devices are required to provide two way non voice communications between the base station and an active medical implant transceiver. The FCC allocated the Medical Implant Communication Service (MICS) band in the range of 402-405MHz in 1999 [1]. The main challenge in implant device is its ultra low power requirement to increase the battery life over a decade. Many research papers on implant transceiver design have been published but still critical problems need to be solved. The commercially available unit consists of a complex transceiver architecture which consumes more than 10mW during operation [2]. The system presented in [3] also consumes around 5.5mW. In this paper, low power implant multi-standard transceiver architecture is proposed which is based on UWB impulses transmitter and 402-to-405MHz MICS band super-regenerative receiver. The complex UWB receiver and 402-405MHz transmitter circuitry, which require LNA, mixer, ADCs and frequency synthesizer, are shifted to base station transceiver, as shown in figure 1. The UWB impulse transmitter generates very short pulses at discrete time intervals instead of continuous sinusoidal signals like in narrow band transmitters. This eliminates the requirement of frequency synthesizer and power amplifier from transmitter side. Due to this reason, power consumption of UWB transmitters is lower than the narrow band MICS transmitters which make them attractive for implant devices. The low power 402-to-405MHz super-regenerative receiver with voltage controlled DSSS quenching scheme is proposed for multiuser environment. The transmitter and receiver are time division multiplexed to transmit UWB impulses and receive 402-to-405MHz on-off keying modulated data pattern.

Section II describes the architecture of UWB impulse transmitter. Section III describes the architecture of 402-to-405MHz super-regenerative receiver. At the end, in section IV, the experimental results are presented.

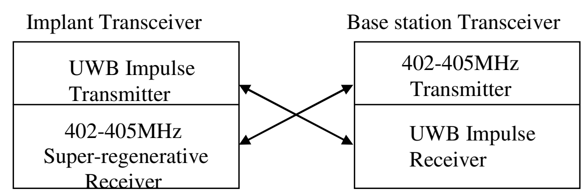

Fig.1 The proposed communication system for multi-standard implant transceiver

II. UWB Transmitter

The conceptual diagram of UWB transmitter is shown in figure 2. It consists of four main parts: pseudo random (PN) pattern generator, glitch generator, delay stages and UWB pulse generator. On-off keying modulation scheme is used to transmit data pattern. The PN pattern generator is enabled during switch-on time to transmit 1s in data pattern and disabled during switch-off time to transmit 0s in data pattern. The main purpose of PN sequence of UWB pulses is to flatten the spectrum by removing the large spectral peaks [4]. Glitch generator is used to generate the small rectangular pulses at each rising edge of PN pattern. Delay stages are used to generate multiple rectangular pulses in time interleaved fashion. The pulse generator is the critical part of the transmitter. This pulse generator is based on combination of three pulse shapers. The pulse shaper consists of pair of

NMOS and PMOS transistors and a second order differentiator. The inverter is connected between the gates of NMOS and PMOS transistors. The input at the gate of NMOS and PMOS transistors is high and low for short duration of time, which is equal to the width of the output of glitch generator. The drain of NMOS and PMOS transistors is connected to the second order differentiator. The outputs of three differentiators are combined by capacitors and applied to 50 Ω antenna. The circuit diagram of impulse generator is shown in figure 2. Multiple number of chirped UWB pulses are generated in pseudo random pattern during 1s in OOK modulated data pattern.

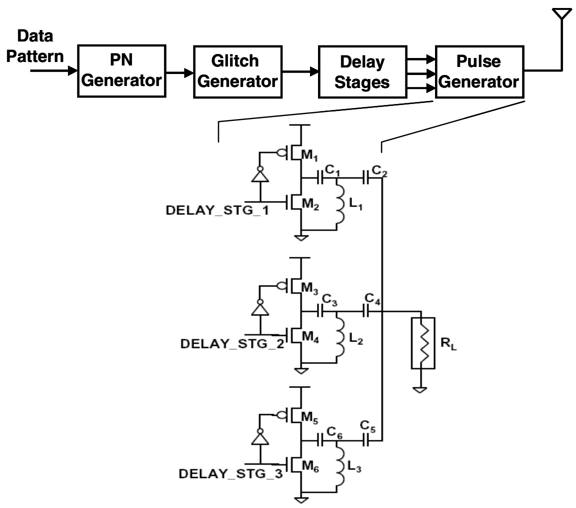

Fig 2. The block diagram of UWB transmitter and circuit diagram of impulse generator

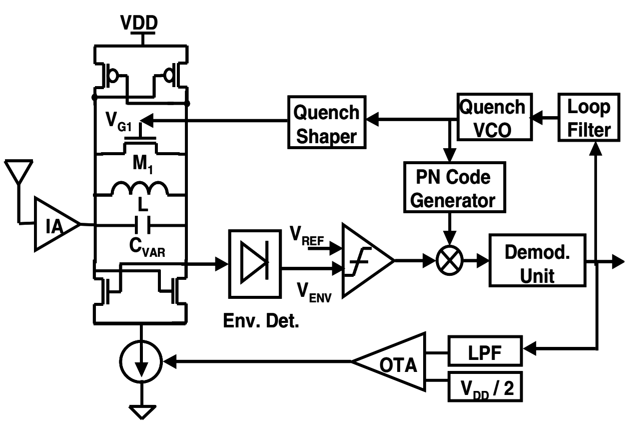

Fig 3. The block diagram of 402-to-405MHz receiver

III. 402-405MHz Super-regenerative Receiver

The block diagram of low power MICS super-regenerative receiver is shown in fig 3. The oscillator, tuned near to 403MHz, is periodically turned on and off by quench signal. The amplitude of oscillations reaches the saturation level quickly in the presence of RF signals having the frequency near to the tuned frequency of oscillator and slowly in the absence of incoming RF signals. Without the RF signals, the oscillations are shut off by quench signal before reaching the reference level. The amplitude of oscillation envelope is compared to the reference level just before the positive edge of quench signal. The quenching is made by another oscillator called quench oscillator which is independent of the strength and frequency of external RF signals. The frequency of quench oscillator is very low compared to the frequency of RF signals but higher than the data modulation frequency. According to the Nyquist criteria, the quenching frequency must be at least twice the data modulation frequency. The shape and frequency of quench pattern, bias current of the oscillator and threshold level of comparator are adjusted to shutdown the oscillation before its amplitude reaches the saturation level. The quench frequency is adjusted by loop filter and quench VCO [5]. The bias current of oscillator is adjusted according to the quench rate. If the quench frequency is high, short time duration is available for the oscillation amplitude to reach the reference level and requires high DC-bias current of oscillator. If the quenching frequency is low, long time duration is available for the oscillation amplitude to reach the reference level and requires low DC-bias current of oscillator. The voltage controlled DSSS quenching scheme is used for multiuser environment The PN code generator and multiplier are required to perform correlation between the baseband spread spectrum signal, which is provided by the clocked comparator, and the locally generated code. The output of the quench VCO is applied to the quench shaper to select the shape of quench signal at the gate terminal of transistor M_1. The sawtooth shape of the quench pattern is selected to control the bandwidth and sensitivity in an efficient manner. In this architecture, quenching of super-regenerative oscillator is made by changing the channel conductance of transistor M_1 across the critical level. The amplitude of oscillation envelope, V_{ENV} is higher than V_{REF} at the end of quench cycle in the presence of the RF signal and V_{ENV} is lower than V_{REF} at the end of quench cycle in the absence of the RF signal. DC free on-off keying modulated scheme is used to adjust the bias current of the oscillator at critical level by current control loop. The output pattern is recovered by the demodulation unit. The simple design of demodulation unit is made by comparing the average voltage of the multiplier output to the threshold level. External bias control loop and complex automatic current calibration unit are proposed in [6-8] for narrow band systems. The simple architecture of feedback current control loop is used in this work [9-10]. The average of digital demodulated output pattern is compared to the reference voltage. DC free on-off keying modulation pattern is required to fix the reference voltage at V_{DD} /2. Initially the transconductance amplifier provides a large current, which results in oscillation amplitude to reach the saturation level in each quench cycle and high level voltage is received at the output of comparator. The output of low pass filter starts to increase, which causes the decrease in bias current of oscillator. The bias current is settled at the critical current level due to dc-free data pattern. The critical level of bias current depends on the on-off keying modulated data rate and the strength and frequency offset of injected RF signals. The maximum number of continuous ones and zeros in on-off keying modulated scheme is limited due to the RC time constant of the current regulation loop.

IV. Experimental Results

The test structure of multi-standard transceiver has been implemented on 0.18μm CMOS technology with an active area of 1.44mm^2. The die photo of our reconfigurable test structure is shown in figure 4. In UWB transmitting mode, power consumption is 0.3mW from 1.5V at the data rate of 500Kbits/s. The measured UWB impulse pattern is shown in fig.5. The pulse width of around 500ps with amplitude of 150mV pp is measured at the load of 50Ω. In receiving mode, the power consumption is 0.5mW at 1.5V supply at data rate of 120Kbits/s. The performance of 402-to-405MHz MICS receiver is measured by injecting the on-off keying modulated signal tuned at 403MHz to the super-regenerative receiver. Figure 6 shows the injected on-off keying modulated RF signal tuned at 403MHz and received pattern at the output of digital demodulation unit. The sensitivity level of -95dBm is achieved for BER<10^{-3}. The measured bandwidth varies from 500KHz to 1.5MHz for -95dBm to -40dBm signals respectively, with sawtooth quenching rate of 400KHz. Due to inherent wide bandwidth of super-regenerative architecture, time scheduled direct spread spectrum coding scheme is proposed to enable all MICS channels (10 channels, 300KHz bandwidth) in multi-user environment.

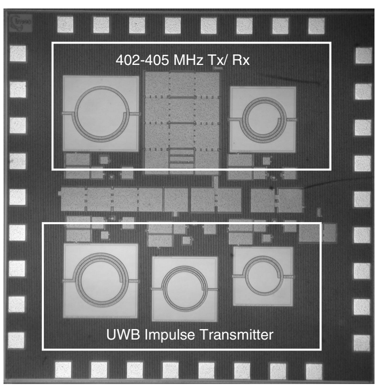

Fig 4. The die photograph of multi standard transceiver UWB Tx / MICS Rx

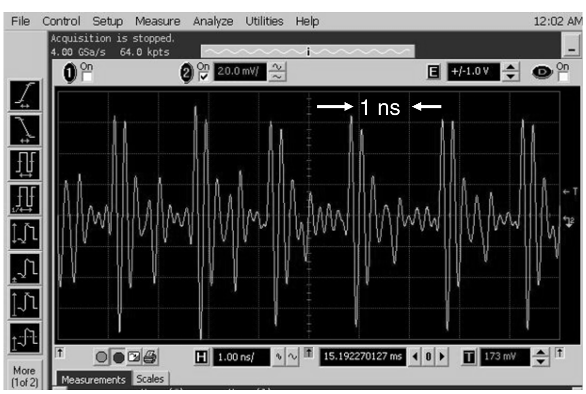

Fig 5. The measured transmitted UWB impulse pattern

V. Conclusion

Low power fully integrated multi-standard transceiver based on UWB impulse transmitter and 402-to-405MHz super-regenerative receiver is presented for medical implant devices. The complex design of UWB receiver and 402-405MHz transmitter is shifted to the base station. The chirped UWB signal is achieved by combination of three impulse generators. The voltage controlled DSSS quenching scheme is used in 402-405MHz super-regenerative receiver for multiuser environment

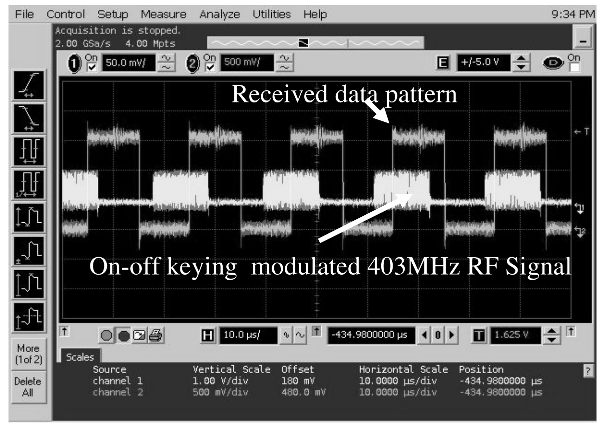

Fig 6. The measured transmitted and received 402-405MHz on-off keying data pattern data

References

[1] MICS Band Plan Federal Commun. Comm., Part 95, FCC Rules and Regulations.

[2] http://www.zarlink.com/zarlink/ieee_bcas_cp_jan06.pdf

[3] Ching-Jen Tung; Yao-Hong Liu; Hui-Hsien Liu; Tsung-Hsien Lin "A 400-MHz super-regenerative receiver with digital calibration for capsule endoscope systems in 0.18-μm CMOS" VLSI Design, Automation and Test, 2008. VLSI-DAT 2008.

[4] G. Maggio, N. Rulkov, and L. Reggiani. Pseudo-chaotic time hopping for UWB impulse radio. Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on], 48(12):1424–1435, Dec. 2001.

[5] Moncunill-Geniz, F.X. Pala-Schonwalder, P. Dehollain, C. Joehl, N. Declercq, M. "A 2.4-GHz DSSS superregenerative receiver with a simple delay-locked loop" Microwave and Wireless Components Letters, IEEE Volume 15, Issue 8, Aug. 2005 Page(s): 499 - 501

[6] A. Vouilloz et al., "A Low-Power CMOS Super-Regenerative Receiver at 1GHz," *IEEE JSSC*, vol.36, no.3, pp. 440-451, Mar. 2001.

[7] Farve P. et al., "A 2-V 600uA 1 GHz BiCMOS Super- Regenerative Receiver for ISM Application," *IEEE JSSC*, vol. 33, no. 12, Dec. 1998.

[8] J.-Y. Chen, M. P. Flynn, and J. P. Hayes, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver," *IEEE ISSCC*, pp.376-377, 2006.

[9] Anis, M.; Tielert, R.; Wehn, N "Low power complementary-colpitts self-quenched super-regenerative ultra-wideband bandpass (UWB) filter in CMOS technology" Microwave Symposium Digest, 2008 IEEE MTT-S International Volume , Issue , 15-20 June 2008 Page(s):1047 – 1049.

[10] Anis, M.; Tielert, R.; Wehn, N. " Super-regenerative UWB impulse detector with synchronized quenching mechanism" Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European Volume , Issue , 15-19 Sept. 2008 Page(s):390 - 393