Module 3: Lab 3

1 DESIGN

Our Design in this Lab is a simpler arbiter.

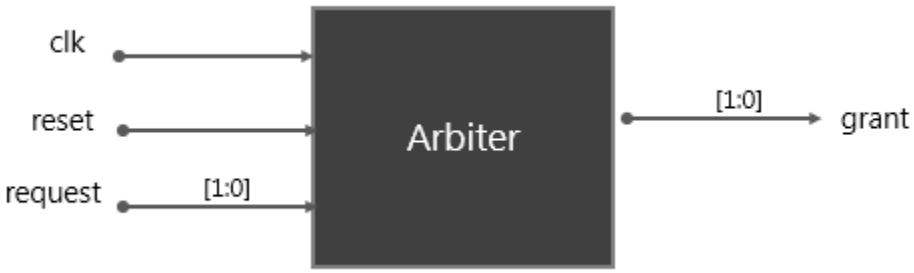

Figure1: Arbiter DUT

Request	Grant (next clock cycle)
2'b00	2'b00
2'b01	2'b01
2'b10	2'b10
2'b11	2'b11
At reset grant is 2'b00	

Figure2: Truth Table for DUT functionality

2 TESTBENCH

A simple testbench has been provided. The test bench sends random transactions in and checks the output using a golden reference model.

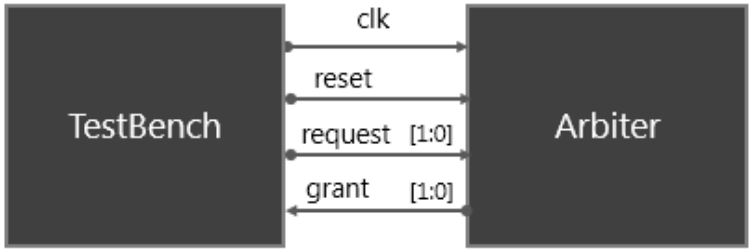

Figure3: Integrate Testbench and Arbiter

3 LAB EXERCISE

1. Write a clocking block in the interface file to integrate the DUT and the testbench. The grant and the request signal should be a part of the clocking block. Also define a TEST modport with clocking block as the input and directions associated with the signals with respect to the testbench. Change the default values to input #3 output #2 and notice the difference in timing in the simulation waves. Under default conditions how quickly can the testbench send in signals and monitor the output.