Code Examples

1 DESIGN

Lets design a simple bit, byte and word addressable memory.

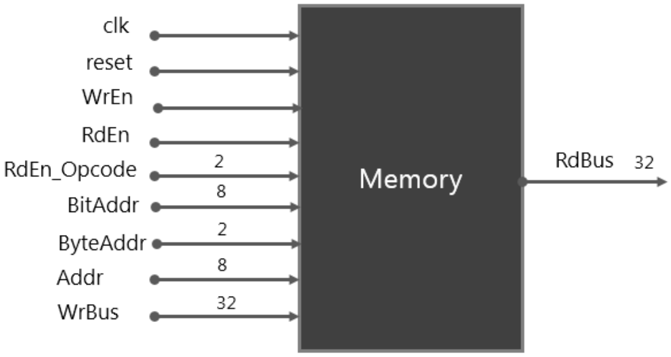

Figure1: Memory DUT

	3								2								1								0							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																																
1																																
2																																
255																																

Figure2: Bit, Byte and Word Addressable Memory

Memory IO description

Signal	Function
clk	input clk to the DUT
reset	reset the system RdBus=0 on reset
WrEn	Write data to the memory, takes 1 clock cycle. Either write or read can be active at any given time.
RdEn	Read data from memory takes 2 clock cycle. Either write or read can be active at any given time.
RdEn_Opcode	0- word read, 1-bit read, 2-byte read, default- word read
BitAddr	Address of the bit in the memory word to be read
ByteAddr	Address of the byte in the memory word to be read
WrBus	32 bit write bus
RdBus	32 bit read bus

2 TESTBENCH

A simple testbench has been provided. The test bench writes to the memory sequentially and reads from the memory sequentially. You are required to write a testbench that can do the following:

1. Generate random write addresses for 500 simulations.
2. Write random data at the above generated addresses
3. Create a golden reference model using packed arrays to mimic the memory above and store all the inputs that are written to the memory DUT into the packed array.
4. Read the entire contents of the memory and compare it with the data in the golden reference memory

3 LAB EXERCISE

1. Is there a bug in the design?
2. Can you analyze the bug?