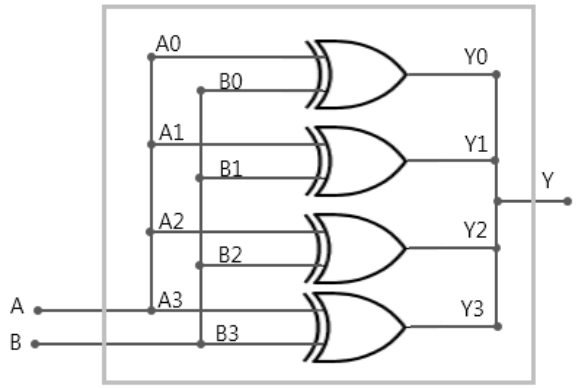
Code Examples

1 DESIGN

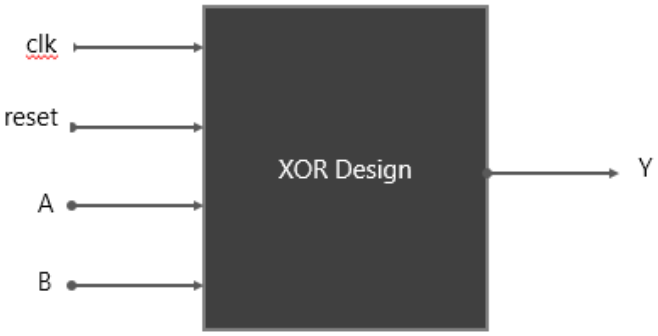
Lets design a simple synchronous 4 bit XOR circuit



A	B	Y=A^B
0000	0000	0000
0001	0000	0001
0010	0001	0011
0100	0010	0110
1000	1011	0011
1111	1010	0101
1111	0110	1001

XOR Sample Truth Table

A 4 bit XOR Circuit



XOR Design

Lets now write code for a 4 bit XOR circuit.

```
//////////////////////////////////////////////////////////////////////
//  AUTHOR: Engineering Design Institute/ASIC Design and Verification
//  DESCRIPTION: 4 bit XOR
//  MODULE NAME: xor_design
//////////////////////////////////////////////////////////////////////
 `timescale 10 ns / 1 ps

  module xor_design(clk,
                    reset,
                    a,
                    b,
                    y);
input clk;
input reset;
input [3:0] a, b;
output reg [3:0]  y;

always @(posedge clk)
      begin
            if(!reset)
                begin
                   y<=a^b;
                end
            else
                begin
                   y<=0;
                end
      end
endmodule
```

2 TESTBENCH

Lets write a simple testbench to do the following:

1. Send random input in using $random function.
2. Measure coverage on input A by defining 8 coverage bins.
3. Run 100 different tests and report coverage

3 LAB EXERCISE

Download the xor_design.vp file and enhance the testbench and run the tests and do the following:

1. Change the coverage bins to show different combinations of A and B coverage.
   0<=A<=64 && 0<=B<=64

Coverage Bin Name	Coverage Point A	Coverage Point B
covbin_0_1	A is 0 or 1	B is 0 or 1
covbin_2_3	A is 2 or 3	B is 2 or 3
covbin_4_5	A is 4 or 5	B is 4 or 5
covbin_6_7	A is 6 or 7	B is 6 or 7
covbin_8_9	A is 8 or 9	B is 8 or 9
covbin_10_11	A is 10 or 11	B is 10 or 11
covbin_12_13	A is 12 or 13	B is 12 or 13
covbin_14_15	A is 14 or 15	B is 14 or 15

2. Run the tests enough number of times to achieve 100% coverage.

4 SUBMISSION

1. Fill in the table below.

Coverage Bin Name	Coverage Point A	Coverage Point B	Time in Simulation when coverage bin was filled
covbin_0_1	A is 0 or 1	B is 0 or 1	
covbin_2_3	A is 2 or 3	B is 2 or 3	
covbin_4_5	A is 4 or 5	B is 4 or 5	
covbin_6_7	A is 6 or 7	B is 6 or 7	
covbin_8_9	A is 8 or 9	B is 8 or 9	
covbin_10_11	A is 10 or 11	B is 10 or 11	
covbin_12_13	A is 12 or 13	B is 12 or 13	
covbin_14_15	A is 14 or 15	B is 14 or 15	