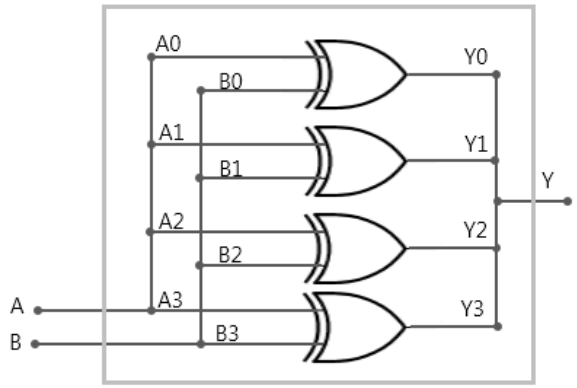
Code Examples

1 DESIGN

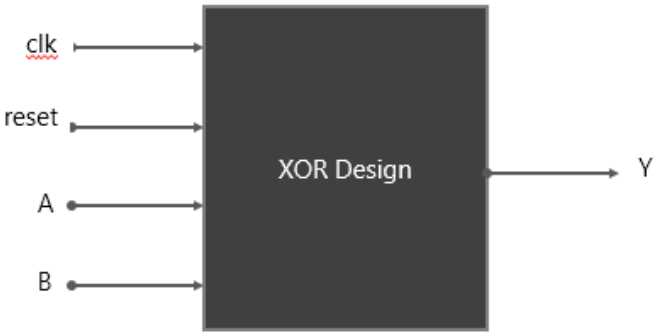
Lets design a simple synchronous 4 bit XOR circuit



A	B	Y=A^B
0000	0000	0000
0001	0000	0001
0010	0001	0011
0100	0010	0110
1000	1011	0011
1111	1010	0101
1111	0110	1001

XOR Sample Truth Table

A 4 bit XOR Circuit



XOR Design

Lets now write code for a 4 bit XOR circuit.

```
//////////////////////////////////////////////////////////////////////
//  AUTHOR: Engineering Design Institute/ASIC Design and Verification
//  DESCRIPTION: 4 bit XOR
//  MODULE NAME: xor_design
//////////////////////////////////////////////////////////////////////
 `timescale 10 ns / 1 ps

  module xor_design(clk,
                    reset,
                    a,
                    b,
                    y);
 input clk;
 input reset;
 input [3:0] a, b;
 output reg [3:0]  y;

 always @(posedge clk)
       begin
              if(!reset)
                  begin
                     y<=a^b;
                  end
              else
                  begin
                     y<=0;
                  end
       end
 endmodule
```

2 TESTBENCH

Lets write a simple testbench to do the following:

1. Iterate over all the 256 combinations of the inputs
2. Compute the golden reference output
3. Compare the DUT output to golden reference output
4. Calculate the total number of successful tests vs total number of tests

3 LAB EXERCISE

Download the xor_design.vp file and run the tests and answer the following questions.

1. How many successful tests were you able to run?
2. Is there a bug in the design? If yes, what do you think it is?

4 SUBMISSION

1. In a single line write the logic to describe the bug you found
2. How many successful tests did you have?