

Module 3: Lab2

1 DESIGN

Our Design in this Lab is a simpler arbiter.

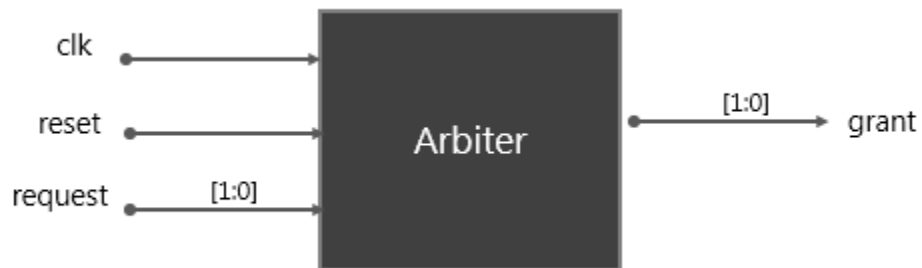


Figure1: Arbiter DUT

Request	Grant (next clock cycle)
2'b00	2'b00
2'b01	2'b01
2'b10	2'b10
2'b11	2'b11
At reset grant is 2'b00	

Figure2: Truth Table for DUT functionality

2 TESTBENCH

A simple testbench has been provided. The test bench sends random transactions in and checks the output using a golden reference model.

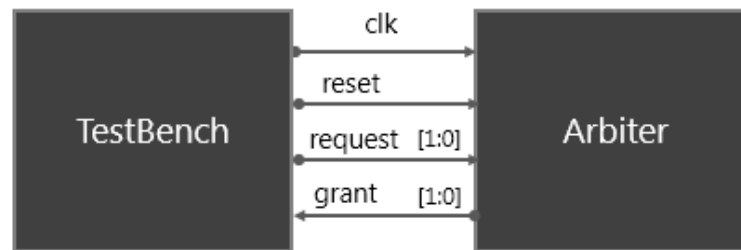
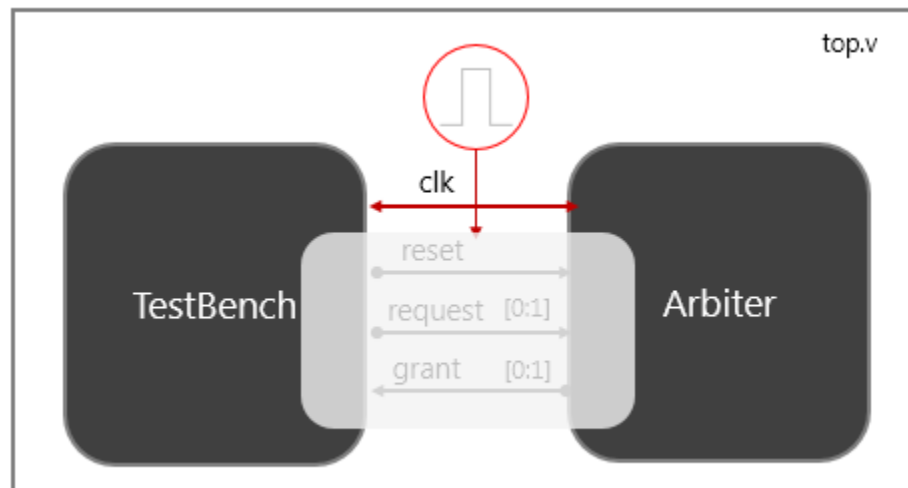


Figure3: Integrate Testbench and Arbiter

3 LAB EXERCISE

1. Write an interface file to integrate the DUT and the testbench. The clock should be generated in the top level file and passed to the Testbench and the Arbiter.



2. Is there a bug in the design?