Module4: Lab1

1 DESIGN

The design is a simple execute block. Figure 1 shows the block diagram of the block and table 1 gives the signal description.

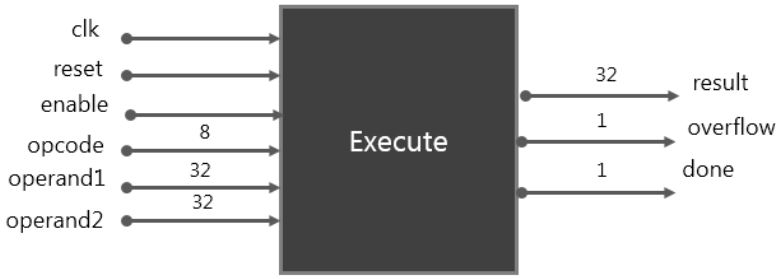

Figure1: Execute DUT

Signal	Function
clk	input clk to the DUT
reset	reset the system result=0 on reset
enable	Enable signal enables the computations in the execute unit
opcode	0: none, 1. Add 2. Subtract 3. Multiply 4: XOR 5. AND 6. OR 7. NAND
operand1	Opereand1 is 32 bits
operand2	Operand 2 is 32 bits
result	32 bit result of the operation performed on operand1 and operand2
overflow	Overflow of Add and Multiply
done	Goes high when the outputs are ready

Table 1: Execute block Signal Description

2 TESTBENCH

A simple testbench has been provided. The test bench generates inputs, sends them into the DUT, and computes the correct output in the golden reference model and a checker to check for correctness. The different features have been split into separate tasks to make the code more readable and modular.

3 LAB EXERCISE

1. Create a transaction class and send the inputs to the DUT.
2. Write a new() function inside the class to randomize the inputs to the DUT the opcode, operand1, operand2.