DIRAM4 SPECIFICS

DiRAM4 Addressing

DiRAM4 Burst of 2		
DiRAM4 Density	68,719,476,736	bits
Ports	64	Ports
Port Density	1,073,741,824	bits
Channels per Port	2	Channels
Bits per Channel	536,870,912	bits
RAMs per Channel	2	RAMs
Bits per RAM	268,435,456	bits
Banks Per RAM	16	Banks
Bank Density	16,777,216	bits
Pages Per Bank	4,096	Pages
Page Density	4,096	bits
Lines per Page	**64**	**Lines**
Line Size	**64**	**bits**

DiRAM4 Burst of 8		
DiRAM4 Density	68,719,476,736	bits
Ports	64	Ports
Port Density	1,073,741,824	bits
Channels per Port	2	Channels
Bits per Channel	536,870,912	bits
RAMs per Channel	2	RAMs
Bits per RAM	268,435,456	bits
Banks Per RAM	16	Banks
Bank Density	16,777,216	bits
Pages Per Bank	4,096	Pages
Page Density	4,096	bits
Lines per Page	**16**	**Lines**
Line Size	**256**	**bits**

Channels	RAM	Banks	bits/Bank	bits/port	Banks/Port	pages/Bank	bits/Page	bits/open pages	words/open pages
2	2	16	16777216	1073741824	64	4096	4096	262144	8192

Bank addre ts for

Truth Table

CK	CK#	Bank	CMD1	CMD0	Address	PS#	Command
↓	↑	BAxx[5:0]	0	1	Internal Counter	0	(PR) Page Refresh
↓	↑	BAxx[5:0]	1	0	X	0	(PC) Page Close
↓	↑	BAxx[5:0]	1	1	PAxx[11:0]	0	(PO) Page Open
↑	↓	BAxx[5:0]	1	0	CAxx[5:0]	0	(CR) Cache Read
↑	↓	BAxx[5:0]	1	1	CAxx[5:0]	0	(CW) Cache Write
↓	↑	X	0	0	X	0	(NOP) No Operation
↑	↓	X	0	0	X	0	(NOP) No Operation
↑	↓	X	X	X	X	1	(DES) Deselect
↓	↑	X	X	X	X	1	(DES) Deselect

Note: All other states are reserved; xx denotes the port number; X denotes a valid signal level but any state.

Port Array Layout

	L3	L2	L1	L0	R0	R1	R2	R3
M	.....							
P7	P7L3	P7L2	P7L1	P7L0	P7R0	P7R1	P7R2	P7R3
P6	P6L3	P6L2	P6L1	P6L0	P6R0	P6R1	P6R2	P6R3
P5	P5L3	P5L2	P5L1	P5L0	P5R0	P5R1	P5R2	P5R3
P4	P4L3	P4L2	P4L1	P4L0	P4R0	P4R1	P4R2	P4R3
P3	P3L3	P3L2	P3L1	P3L0	P3R0	P3R1	P3R2	P3R3
P2	P2L3	P2L2	P2L1	P2L0	P2R0	P2R1	P2R2	P2R3
P1	P1L3	P1L2	P1L1	P1L0	P1R0	P1R1	P1R2	P1R3
P0	P0L3	P0L2	P0L1	P0L0	P0R0	P0R1	P0R2	P0R3

Port Interface Electricals

- Single-ended CMOS
  - VDDIO: 0.70 V nominal
  - VIH ≤ VDDIO/2 + 0.070 V
  - VIL ≥ VDDIO/2 - 0.070 V
  - 350 Ohms ≥ ZOUT (nominal) ≥ 10 ohms (configurable)
  - Cin ≈ 200 fF
- Diff Input Clock Receivers
  - VREF: 0.35 V nominal

Core Power

- **Page Open Operation**
  - 100 pJ
- **Refresh and Page Close Operation**
  - 320 pJ
- **Cache Read or Write Operation**
  - 64 pJ

- **Page Open @ 1GHz**
  - 100e-12 J / 1e-9 Sec
  - 100 mW @ 1.2 V
  - **83.33 mA**
- **Ref & PC @ 1GHz**
  - 320e-12 J / 1e-9 Sec
  - 320 mW @ 1.2 V
  - **320 mA**
- **Cache Read or Write Cycle**
  - 64e-12 J / 1e-9 Sec
  - 64 mW @ 1.2 V
  - **53.33 mA**

Refresh Rates

Temperature	Refresh Rate
85-0°C	64 ms
85-95°C	32 ms
95-115°C	8 ms