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# DiRAM™ Architecture Overview


**David Chapman**

**VP Marketing**


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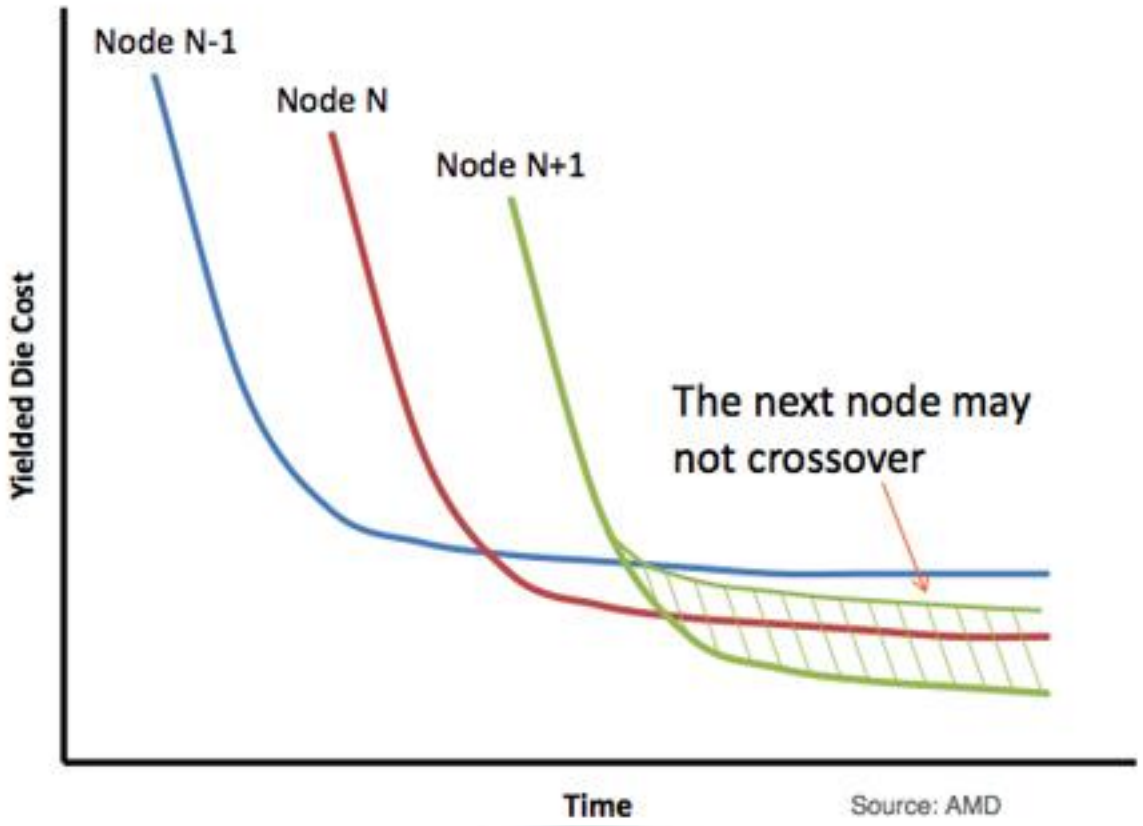
# Why 3D? – Expiring Economics




AMD 2014 3D-ASIP

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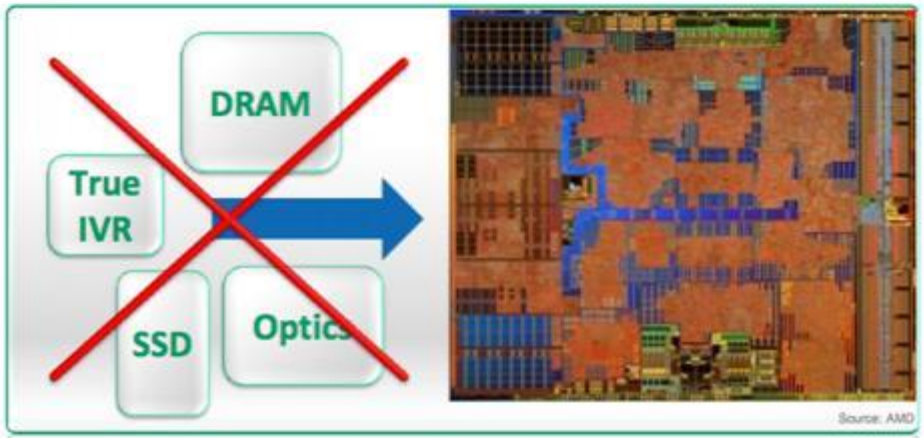
# Why 3D? – Apples & Oranges




AMD 2014 3D-ASIP

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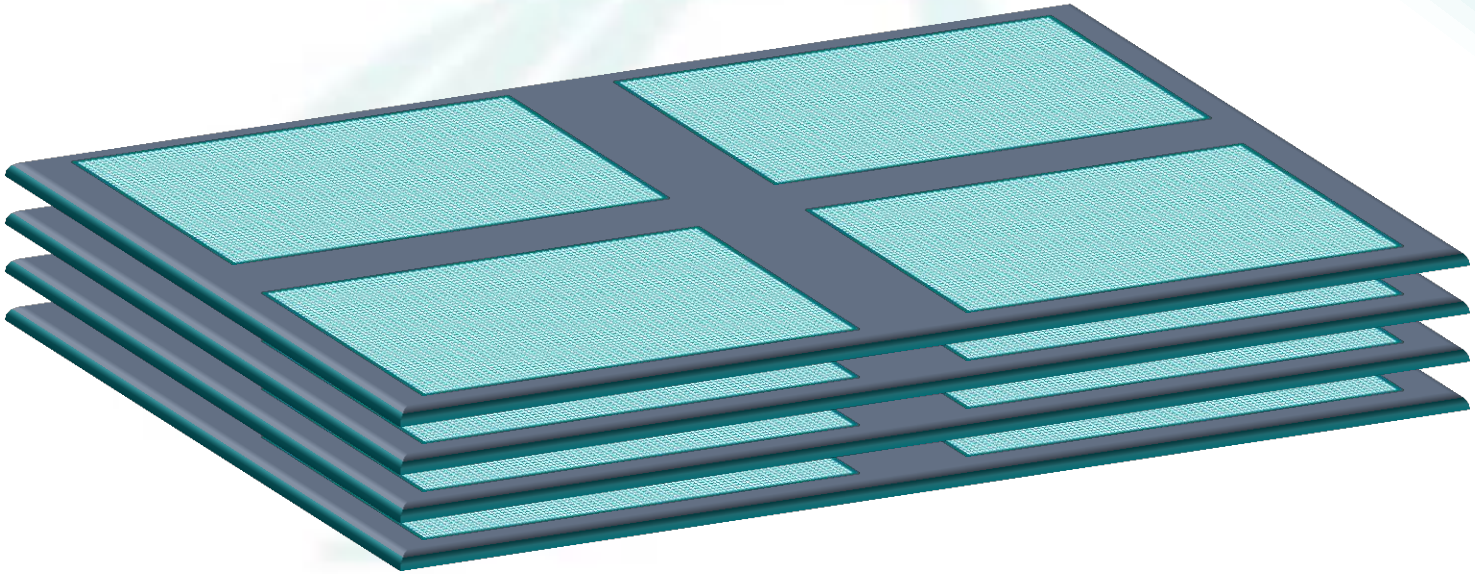
# Conventional 3D *Packaging*

- Preserves traditional RAM problems
- Adds stacking costs



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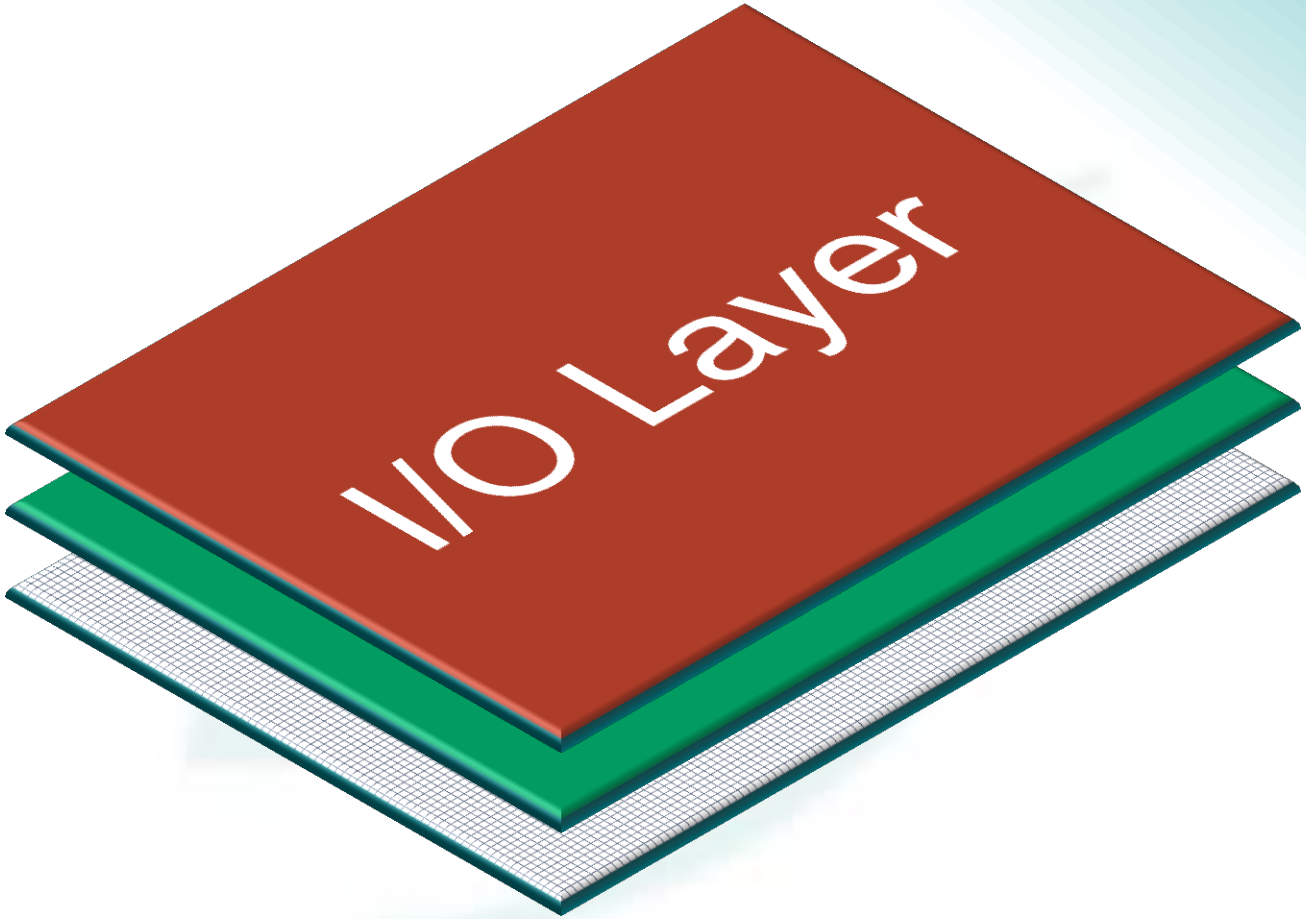
# DiRAM™ True 3D RAM Architecture

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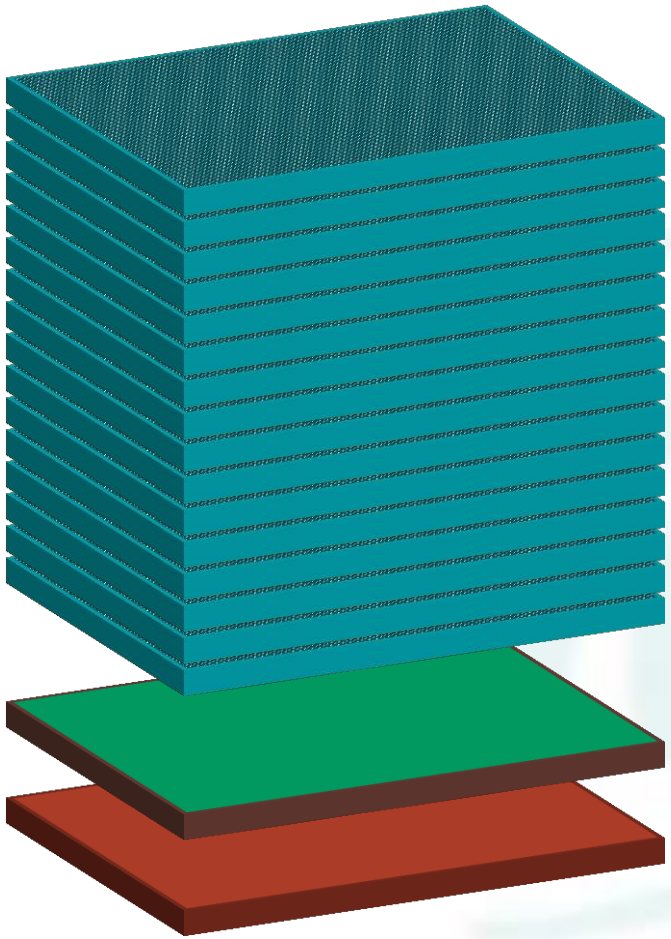
# Dis-Integrated 3D RAM Architecture



**DiRAM™ Architecture**

**Memory Cells and Access Transistors**

**Sense Amps, etc.**

**I/O Layer**

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# DiRAM4 Stack Internal Architecture

- **64 Gb** of Memory in 175 $mm^2$
- **256** fully independent RAMs
- **16 Banks** per RAM
- **64 bit** Sep I/O Data per RAM
- **22ns tRC** (Page Open to Page Open in a Bank)
- **16 Tb/s Data Bandwidth @ Controller Layer**
- Competitive Manufacturing Cost

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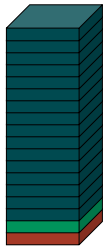
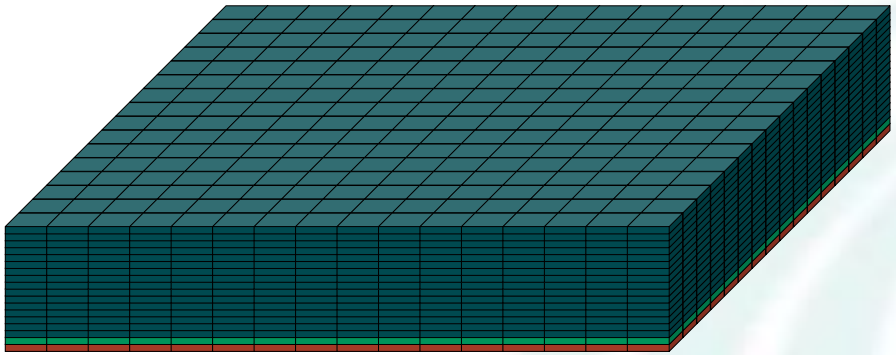
# 256 Independent RAMs



## Each RAM

- 256 Mb Storage
- 64 Gb/s Bandwidth
- 9ns Latency
- 15ns tRC
- 16 Banks

# DiRAM4 64C64 Performance



**256 Independent RAMs**

- **64 Gb** Storage
- 64 Ports
- 128 Channels
- **4096** Banks
- **> 4** Terabit/s Data Bandwidth
- 9 ns Latency
- **64** Billion Transactions Per Second (Minimum)

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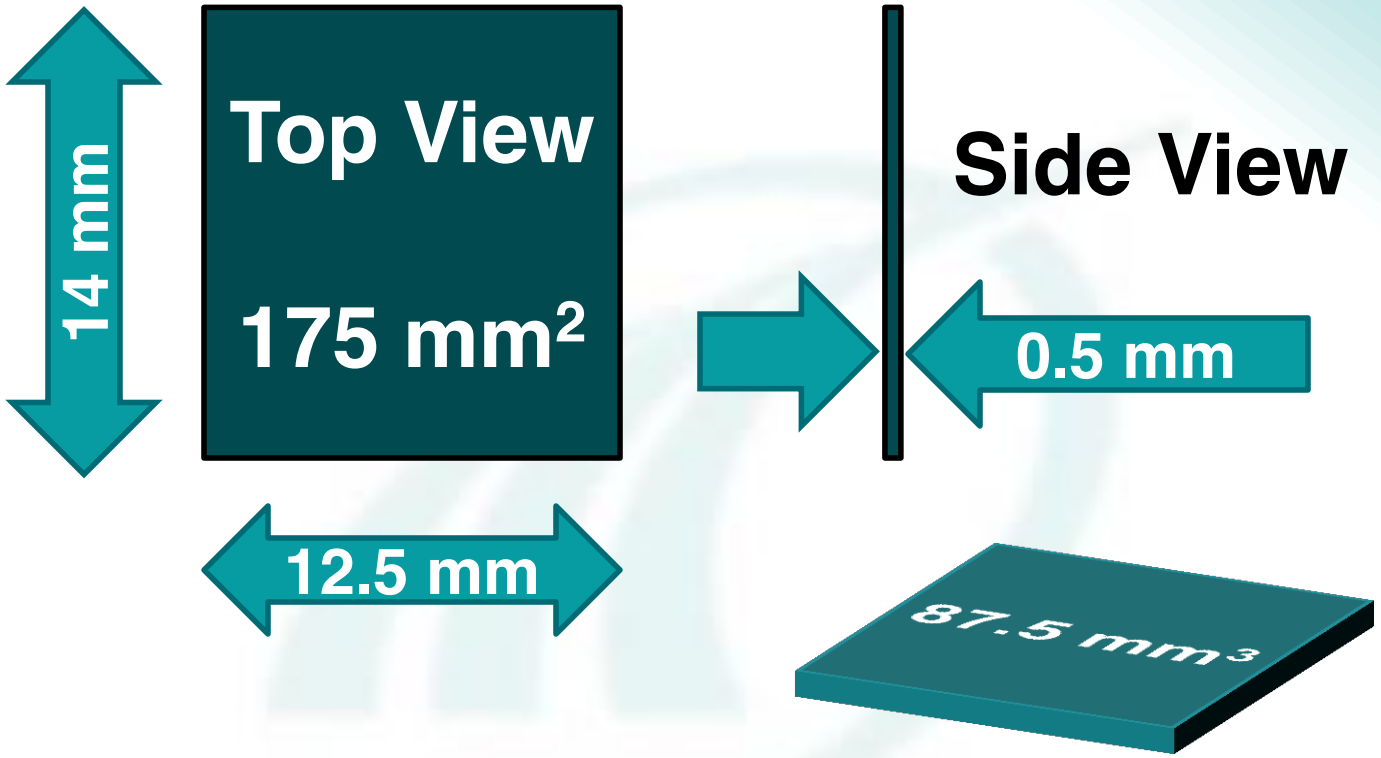
# DiRAM4 Scale* Drawing




* Almost to scale

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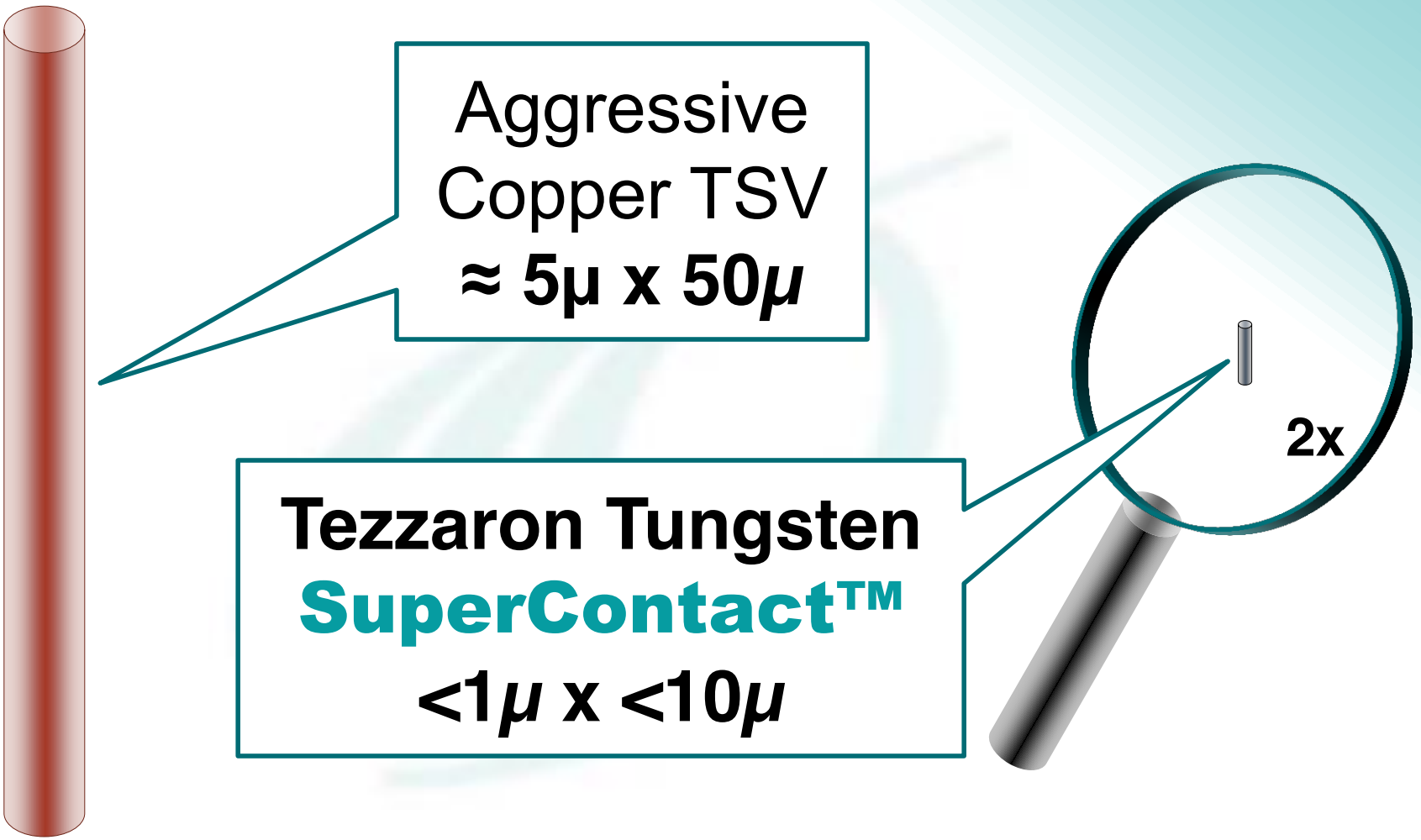
# Via-Free Wafer Stacking

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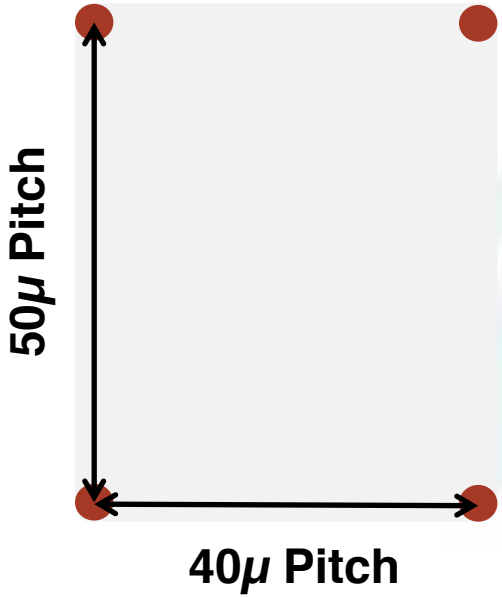
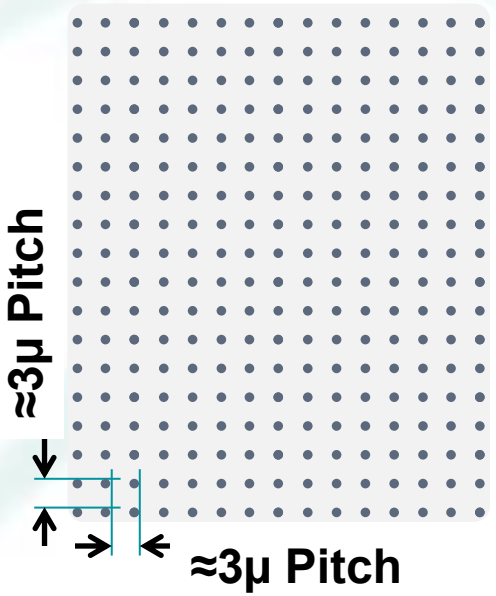
# Common, Cheap, Fast and…Dense

**5μ Diameter**
**Copper TSVs**
**(Stress driven Pitch)**




**<1μ Diameter**
**Tungsten SuperContacts**
**(Alignment driven Pitch)**




**Tezzaron wins: *>66 to 1***

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# Radically Different Manufacturing

**Conventional Flow**

- Fabricate Wafer
- Probe Test Die
- Thin Wafer
- Singulate Die
- Stack Good Die
- Package Stack
- Burn-In & Test Stack

**Tezzaron Flow**

- Fabricate Wafer
- **Stack Wafers**
- **Thin Top Wafer**
- ***Repeat***
- **Probe Test Stacks**
- **Singulate Stacks**
- Package Stacks
- Burn-In & Test Stack

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# Never Handle A Thin Wafer

## The Tezzaron Mantra

Bond Two…Grind One

…to make the world's thinnest RAM wafers

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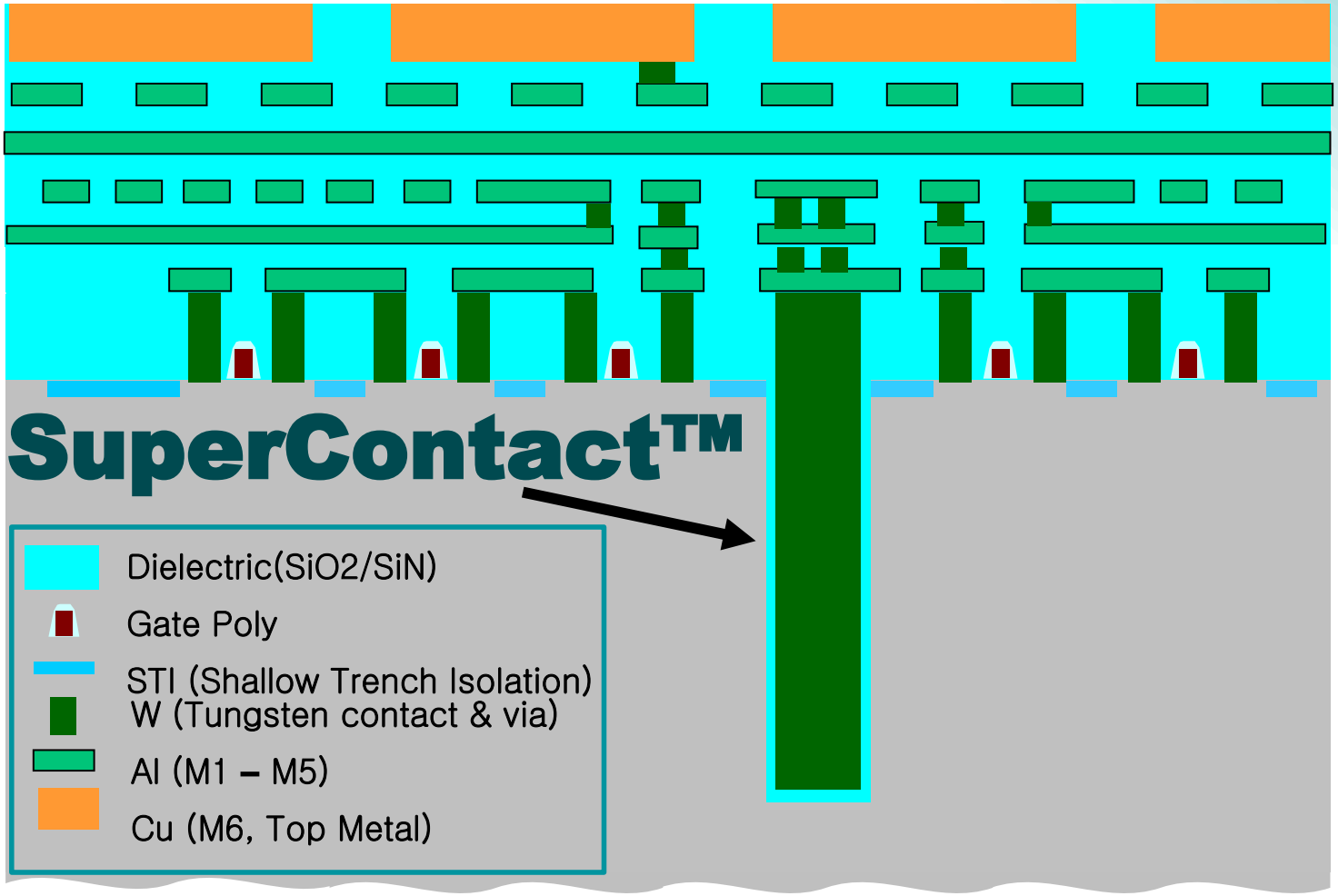
# Step 1 – Build, Drill, Fill & Metalize

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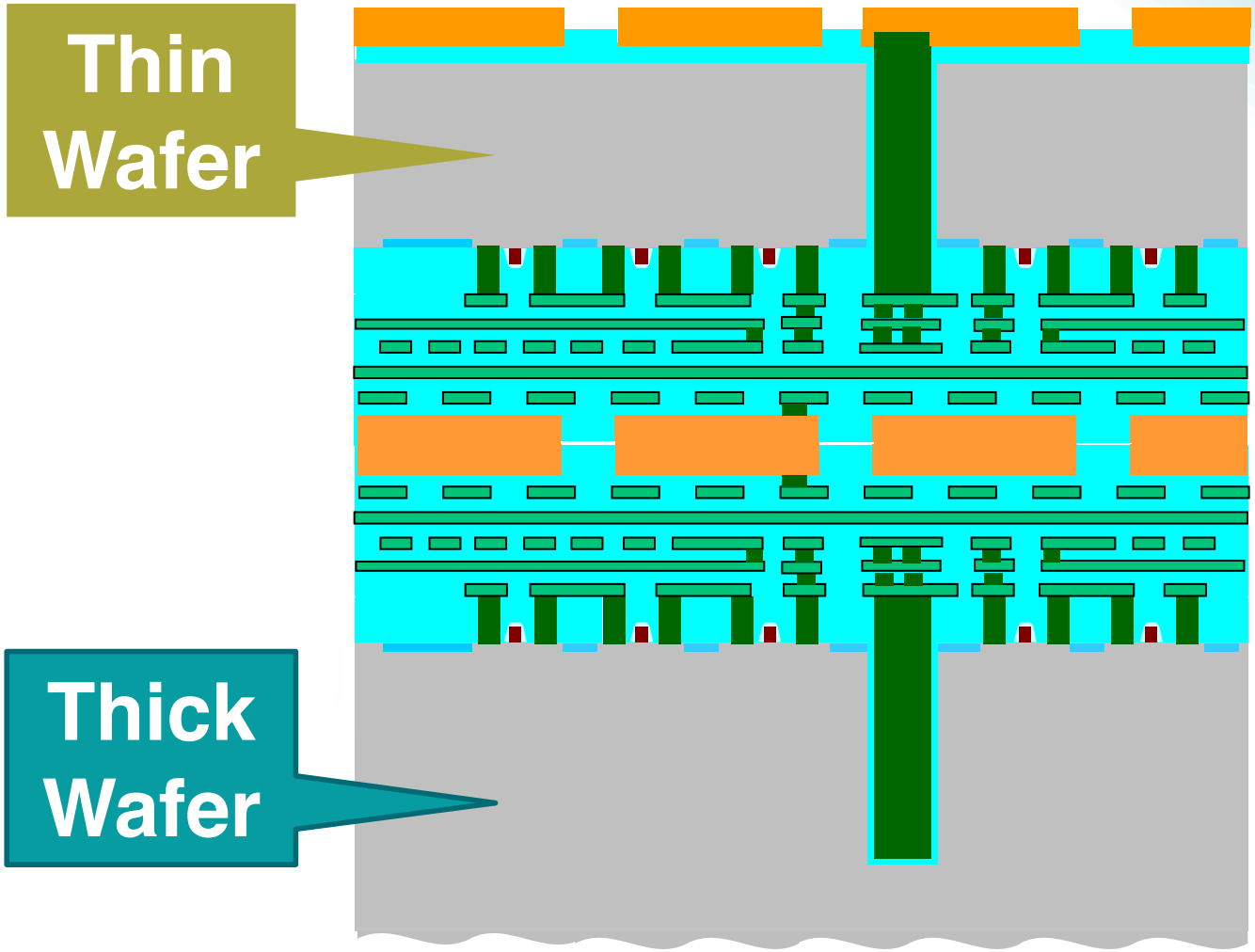
# Step 2 – Bond, Thin & Re-metal

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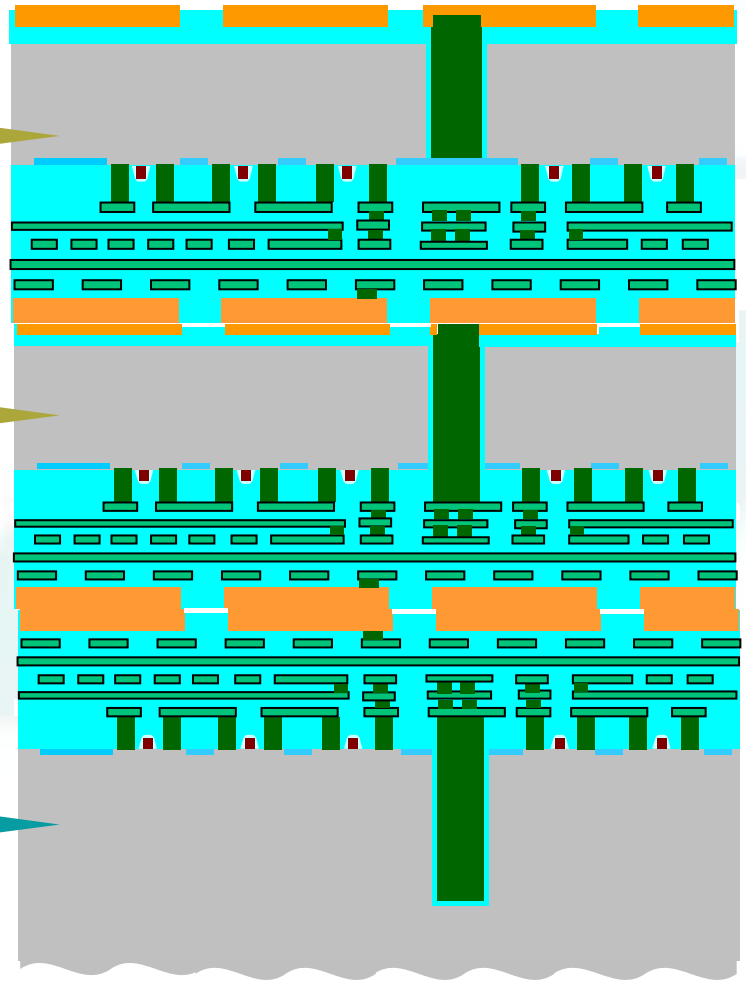
# Step ($n$-1) – Rinse and Repeat

Thin Wafer

Thin Wafer

Thick Wafer



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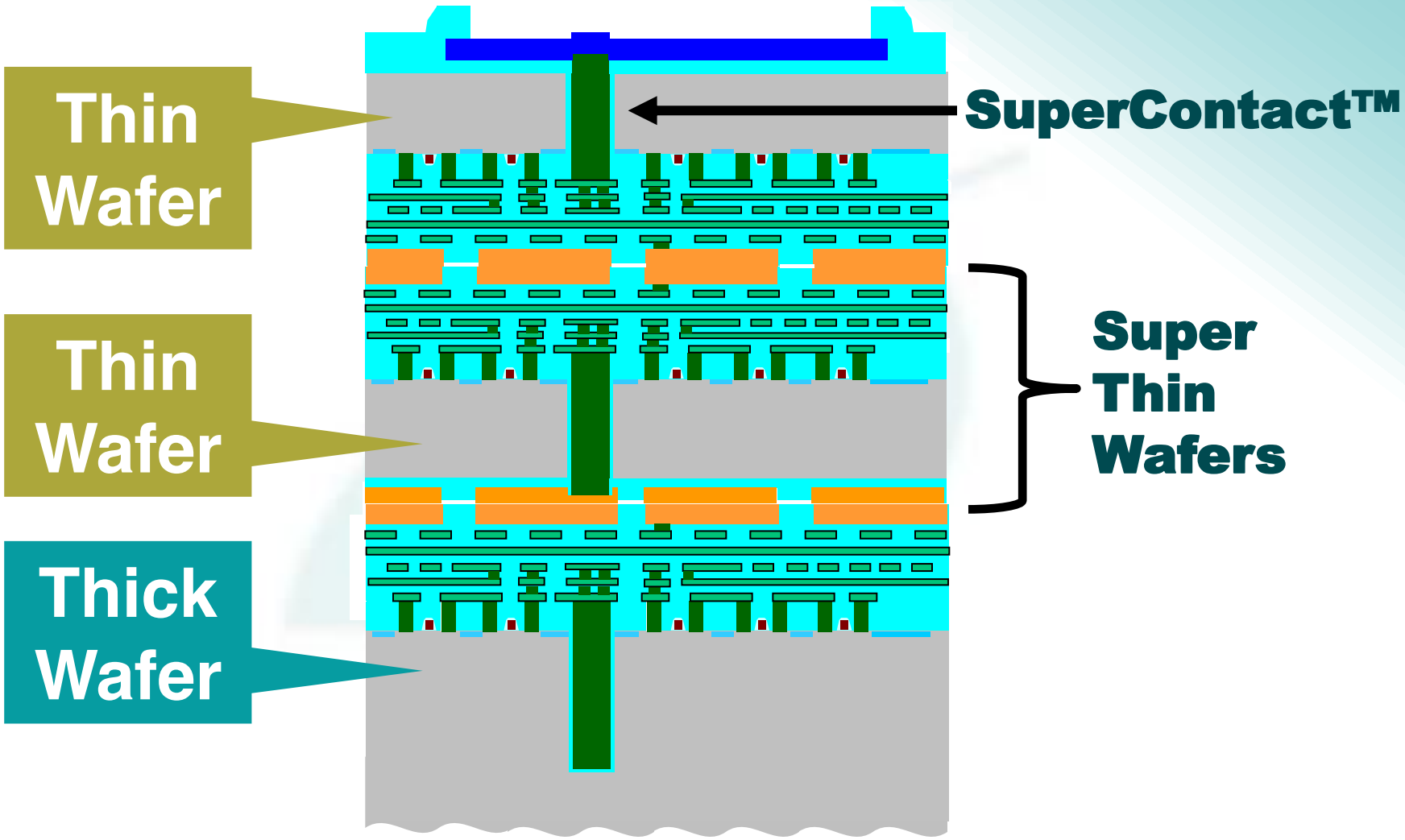
# Step $n$ – Build I/O Pads

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# “That can’t work…”

“…bonding un-tested die will produce **near zero yields**, **poor reliability** and **high costs**.”

## Translation

*You Tezzaron people are crazy!*

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# Super dense interconnect allows…

## Bi-STAR®

**B**uilt-**i**n **S**elf **T**est **A**nd **R**epair

- Controlled by **embedded ARM processor**
- Enabled by **per-cell** control interconnect
- Super-fine grained test and repair
- Continuous, in-the-system hard and soft error repair

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# Bi-STAR™ Does More, Works Better

## Bi-STAR Repairs

- Bad memory cells
- Bad line drivers
- Bad sense amps
- Shorted word lines
- Shorted bit-lines
- Leaky bits
- Bad secondary bus drivers

## Bi-STAR Tests

- Tests > 300,000 nodes per clock cycle
- Tests > 1,000x faster than external memory tester
- Via SPI port, works with Host to allow continuous scrub / repair

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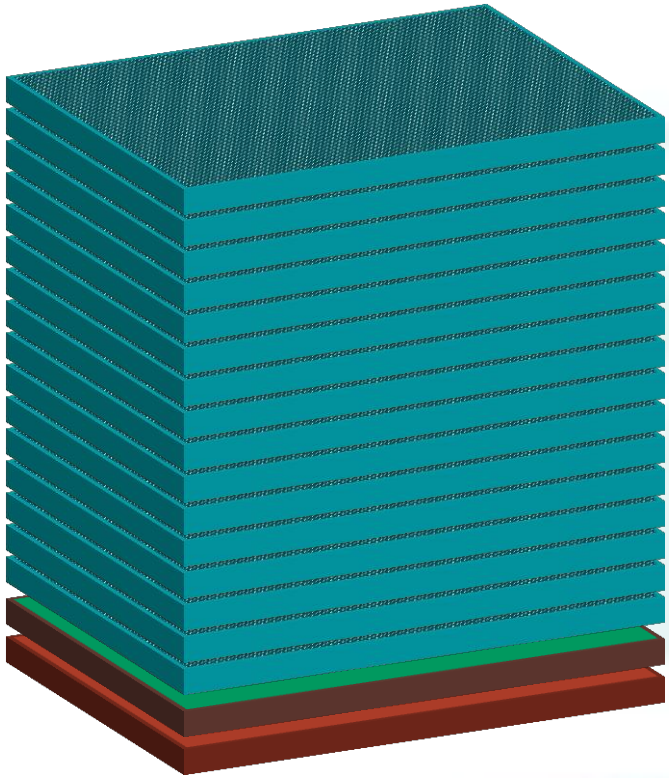
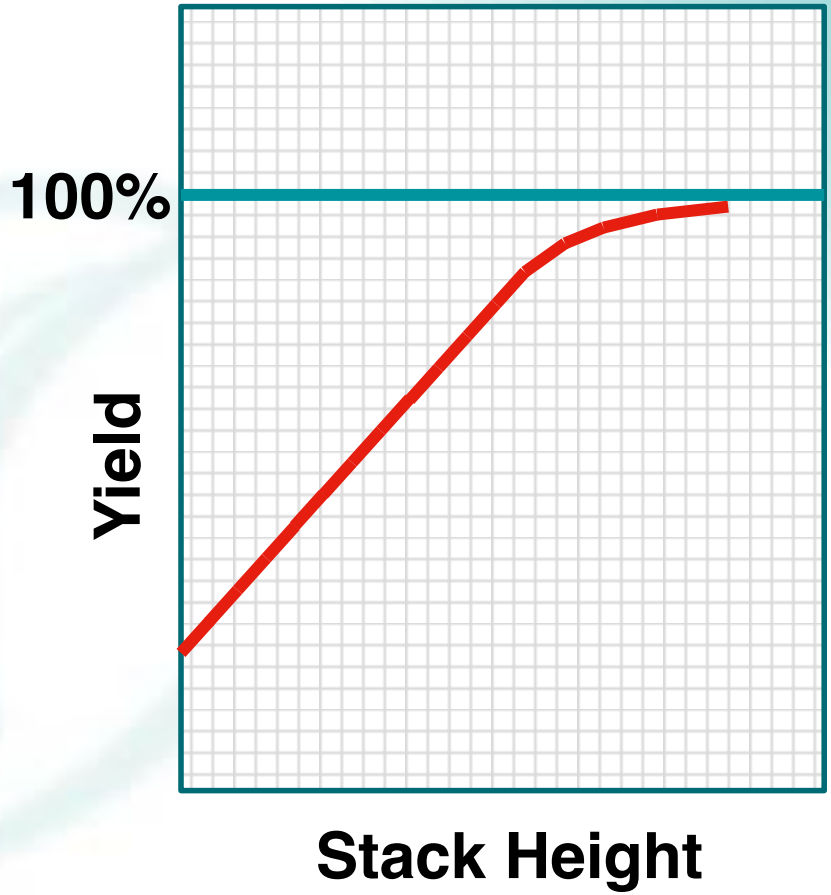
# Bi-STAR Repair Improves Yield



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# Solve 3D Problems with 3D

**Bonding Untested Wafers**

**Enables Super Thin Wafers**

**Enables Effective Repair**

**Enables Tiny Vias**

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# DiRAM: Efficiency for the Future

- Less aggressive wafers
- Higher array efficiency
- Much lower test cost
- Higher yield
- Longer product life cycles

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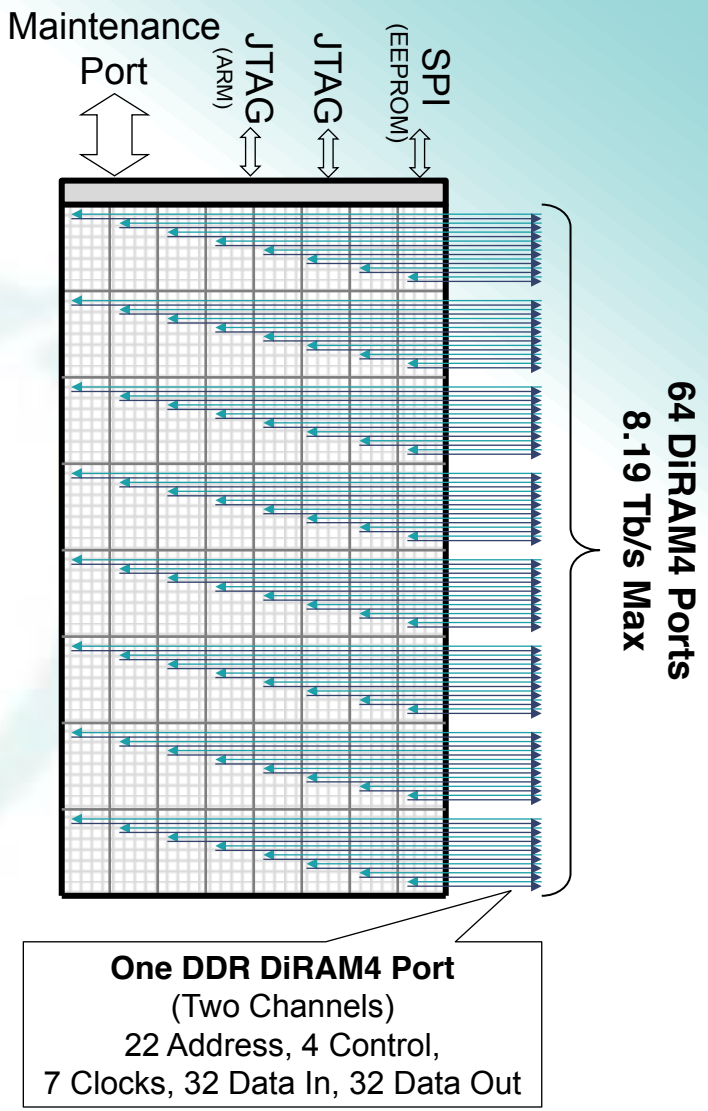
# 64C64 Density and Performance

- **64 Gb** in 175 $mm^2$ footprint
- **64 Ports**
- **128 Channels**
- **32 Banks** per Channel
- **32 bit** Sep I/O per Port
- **14 ns** Worst Case Latency
- **22 ns** tRC

  (Page Open to Page Open in same Bank)
- **4 Tb/s** Min Data Bandwidth

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# RAM is now Singular

## DiRAM4™ Changes the Language of System Design…

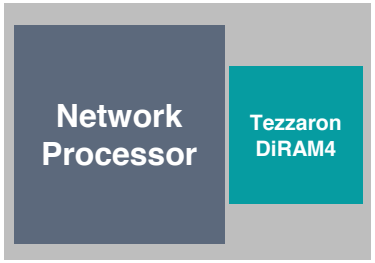
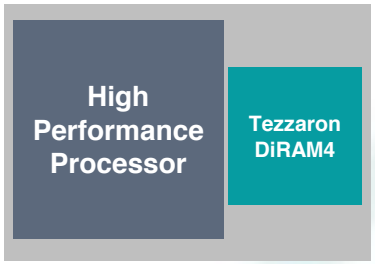



Table Memory + Packet Buffer

### DiRAM4™ in Networking

- High Transaction Rate
- High Bandwidth
- High Density




Local Memory and/or Cache

### DiRAM4™ in Computing

- High Bandwidth
- High Density
- Small References


Fast Local Memory

### DiRAM4™ in Everything

- Multiple Independent Channels
- High Bandwidth
- High Transaction Rate

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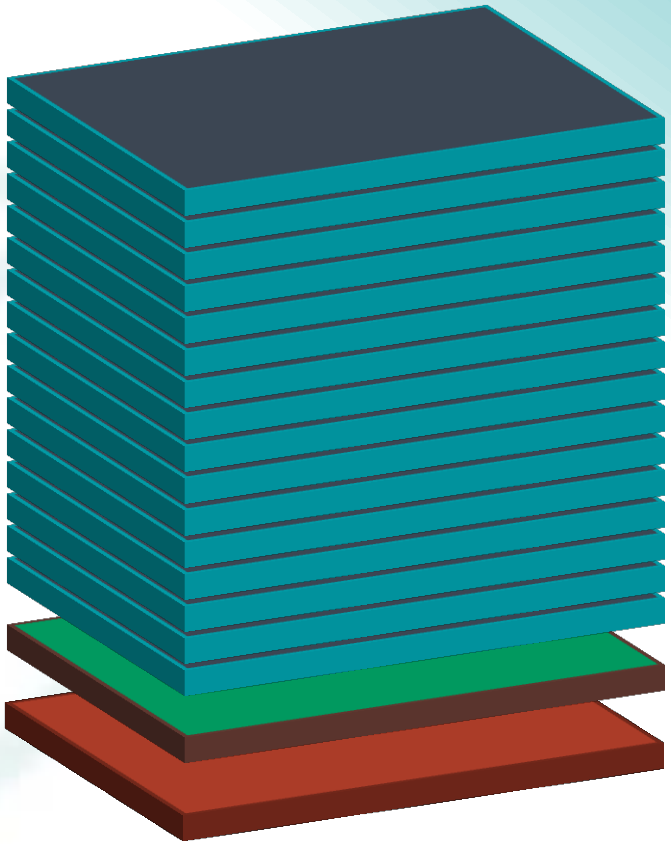
# The Right I/O for Each Market

**DiRAM4**
**Launches**
**with**

**0.7 V CMOS I/O**

**2.5D Si or Organic**

- Low Power
- High Performance



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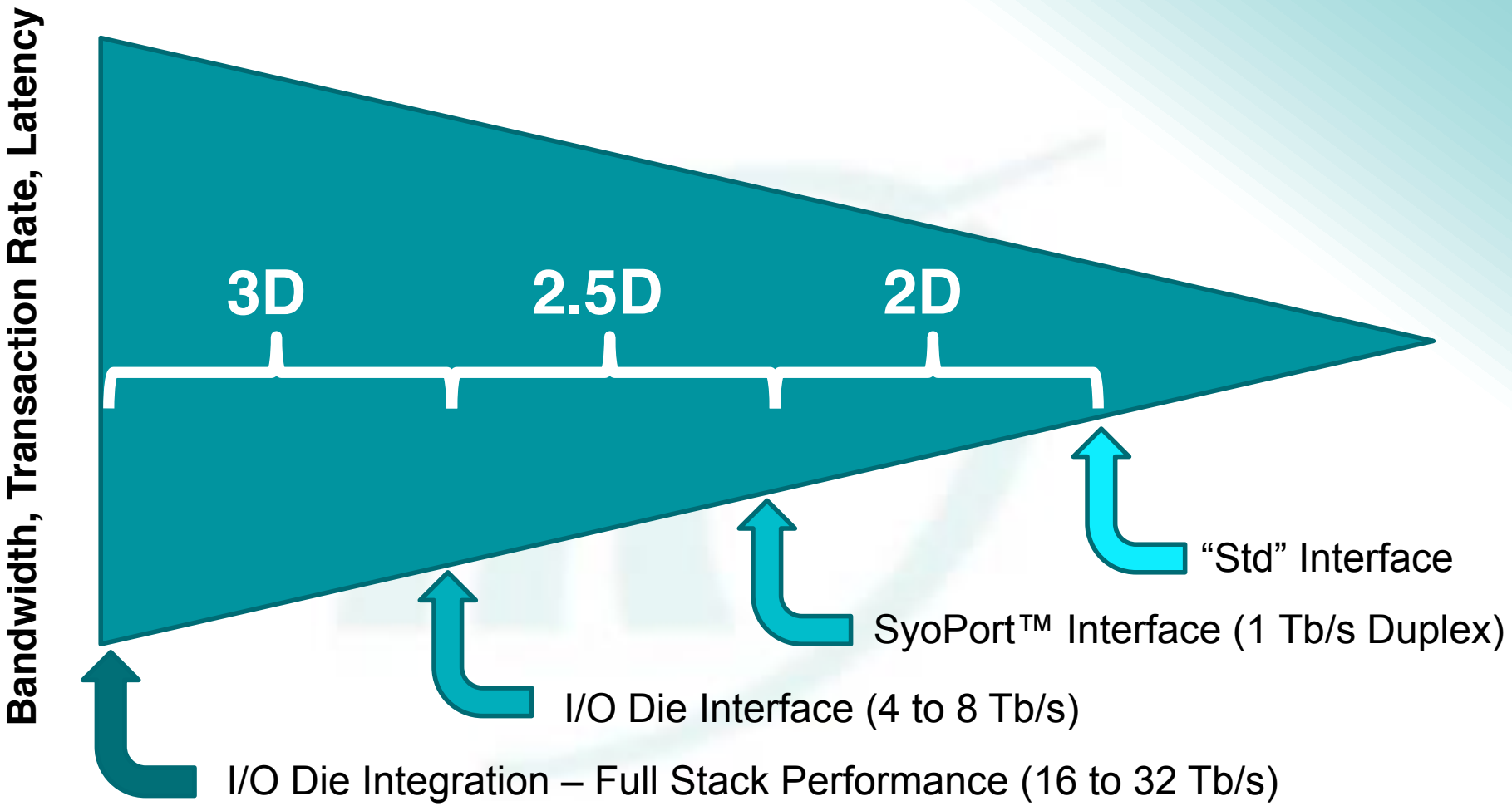
# Performance Choices

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