CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: ___Section 2_4____

Team Members: _____ John Brose _____

_____ Andrew Deick _____

_____ Rolf Anderson _____

Course Goals:

- Obtain an A in the course
- Obtain a deeper understanding of the MIPS architecture
- Learn GitHub and use it effectively
- Learn common hardware components
- Prepare myself for a career in embed systems
- Understand assembly language and how to program with it

Team Expectations:

- **Conduct:** Group members are prfessonal towards one another, diligent in their work, and receptive to communication.
- **Communication:** Best forms of communication are discord and snapchat. Responses should be within the day. At least communicate once a week.
- **Group conventions:** Use do files when applicable. Naming convention for wires will be i_varName, o_varName, s_varName. File naming convention tb_component, when demux or mux type hardware use 32t1, 4t8 etc. Compilation and simulation will be done with modelsim. Version control will be done with GitHub. Comment a lot so other team members can understand.
- **Meetings:**
    - Meeting times can either be in person or online.
    - Monday from noon to 2, Friday from 2 to 4.
    - Andrew will do more of the programming, John and Rolf will be do more of the modelsim.
- **Peer Evaluation Criteria:**
  Effort is defined as the amount of work completed in a given time frame.
  Contribution is defined as the amount of work you do overall.

Role Responsibilities:

Lab Part		Estimated Time	Design		Test	
			Lead	**Deadline**	**Lead**	**Deadline**
Software-Scheduled Pipeline	Control Signals	0.5 hr	Rolf	April 22	John	April 29
	Datapath	3 hr	John	April 22	Rolf	April 29
	Testing	3 hr	Andrew	April 22	John	April 29
	Synthesis (human effort)	0.5 hr	Rolf	May 6	Andrew	May 6
Hardware-Scheduled Pipeline	Pipeline Register Update	1 hr	NA	NA	NA	NA
	Data Hazard Avoidance	4 hr	NA	NA	NA	NA
	Control Hazard Avoidance	2-6 hr based on group size	NA	NA	NA	NA
	Integration (Hardware-Schedule Pipeline)	3 hr	NA	NA	NA	NA
	Testing	3 hr	NA	NA	NA	NA
	Synthesis	0.5 hr	NA	NA	NA	NA

Integrity of Work: We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature  **Date** ____4/1/21_____

Student Signature _____Andrew Deick_____ **Date** ___4/1/21_____

Student Signature _____Rolf Anderson_____ **Date** ___4/1/21_____