CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: _____Section 2_4_____

Team Members: _____John Brose_____

_____Andrew Deick_____

Course Goals: Rolf Anderson

- Obtain an A in the course
- Obtain a deeper understanding of the MIPS architecture
- Learn GitHub and use it effectively
- Learn common hardware components
- Prepare myself for a career in embed systems
- Understand assembly language and how to program with it

Team Expectations:

- **Conduct:** Group members are prfessonal towards one another, diligent in their work, and receptive to communication.
- **Communication:** Best forms of communication are discord and snapchat. Responses should be within the day. At least communicate once a week.
- **Group conventions:** Use do files when applicable. Naming convention for wires will be i_varName, o_varName, s_varName. File naming convention tb_component, when demux or mux type hardware use 32t1, 4t8 etc. Compilation and simulation will be done with modelsim. Version control will be done with GitHub. Comment a lot so other team members can understand.
- **Meetings:**
  - Meeting times can either be in person or online.
  - Monday from noon to 2, Friday from 2 to 4.
  - Andrew will do more of the programming, John will be do more of the modelsim.
- **Peer Evaluation Criteria:**
  Effort is defined as the amount of work completed in a given time frame.
  Contribution is defined as the amount of work you do overall.

Role Responsibilities:

Lab Part	Estimated Time	Design		Test	
		Lead	**Timeline**	**Lead**	**Timeline**
High-level design	1 hr	Andrew	Mar 4	John	NA
Test programs	4 hr	Andrew	Mar 23	John	March 25
Control logic	2 hr	John	Mar 11	Andrew	Mar 16
Fetch logic	3 hr	Andrew	Mar 11	John	Mar 16
Barrel shifter	2 hr	John	Mar 11	Andrew	Mar 16
ALU integration + Misc updates	2 hr	Andrew	Mar 11	John	Mar 16
High-level integration	4 hr	John	Mar 23	Andrew	March 25
Synthesis (human effort)	1.5 hr	John	Mar 28	Andrew	Mar 30

Integrity of Work: We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature _____ **Date** 2/25/21

Student Signature _____Andrew Deick_____ **Date** ___2/25/21_____

03/11/2021