



# **ECE375**

## **Timer/Counter**

**TA:**

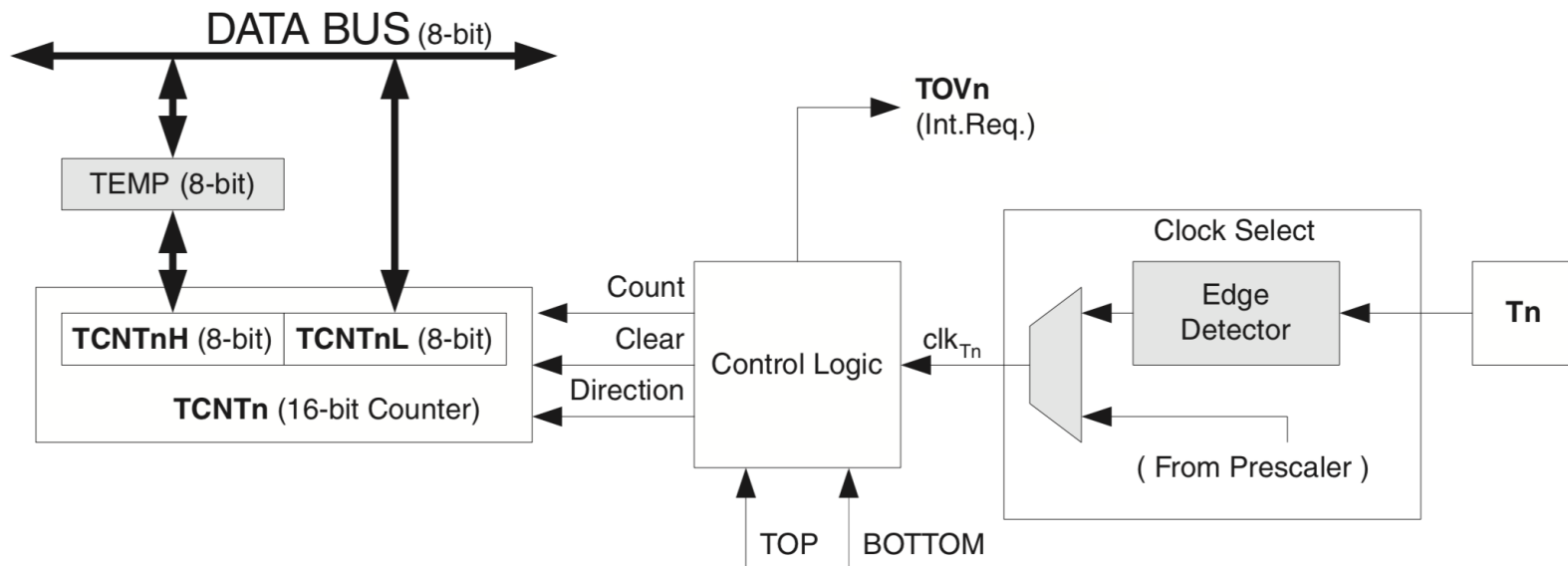
School of Electrical Engineering and Computer Science  
Oregon State University

# Goal of this Lab

- Understand the 16-bit Timer/Counters to generate Pulse-Width Modulation (PWM)
- Correctly configure related registers.
- Control the motor speed of BumpBot using PWM signal

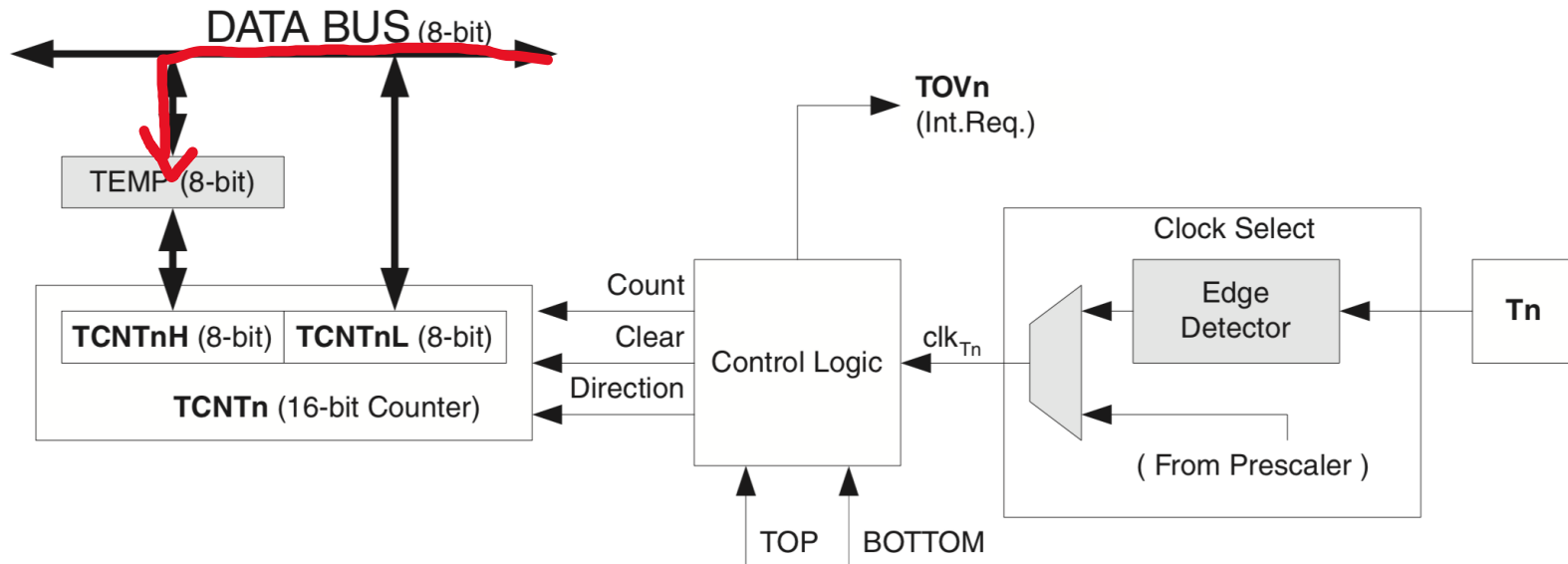
# Why write higher byte first, read lower byte first?

**Figure 47.** Counter Unit Block Diagram



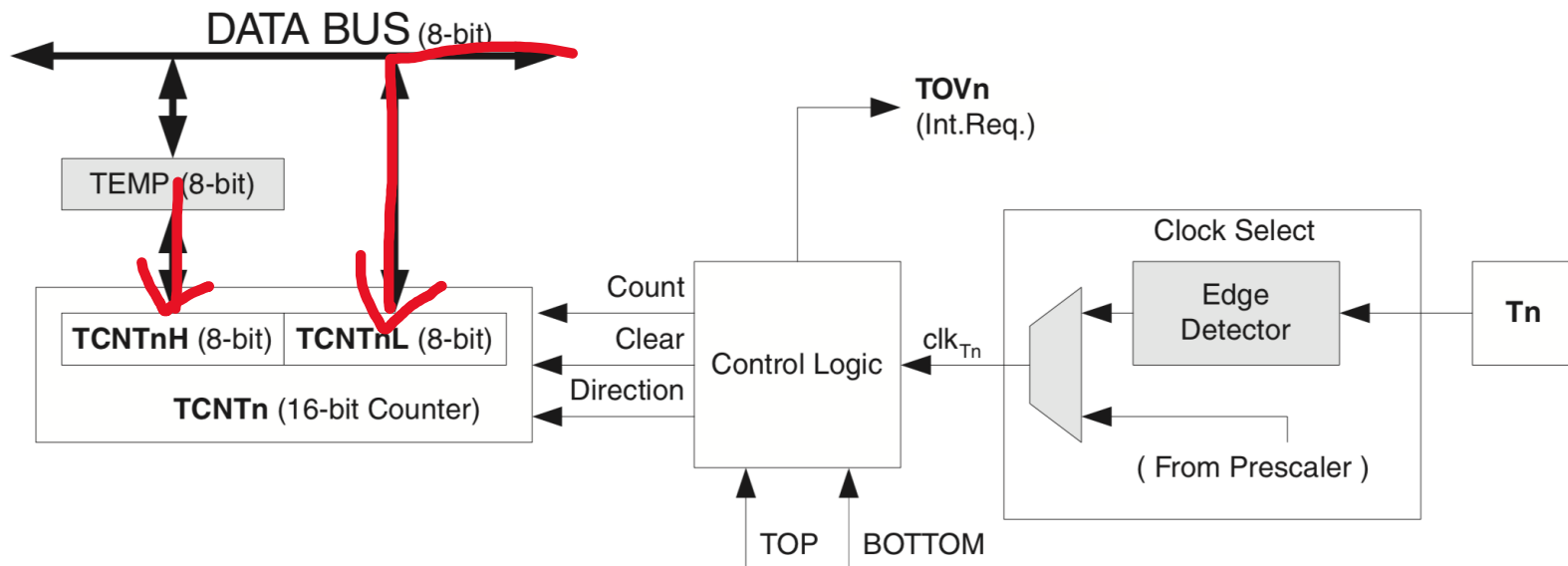
# Why write higher byte first, read lower byte first?

**Figure 47.** Counter Unit Block Diagram



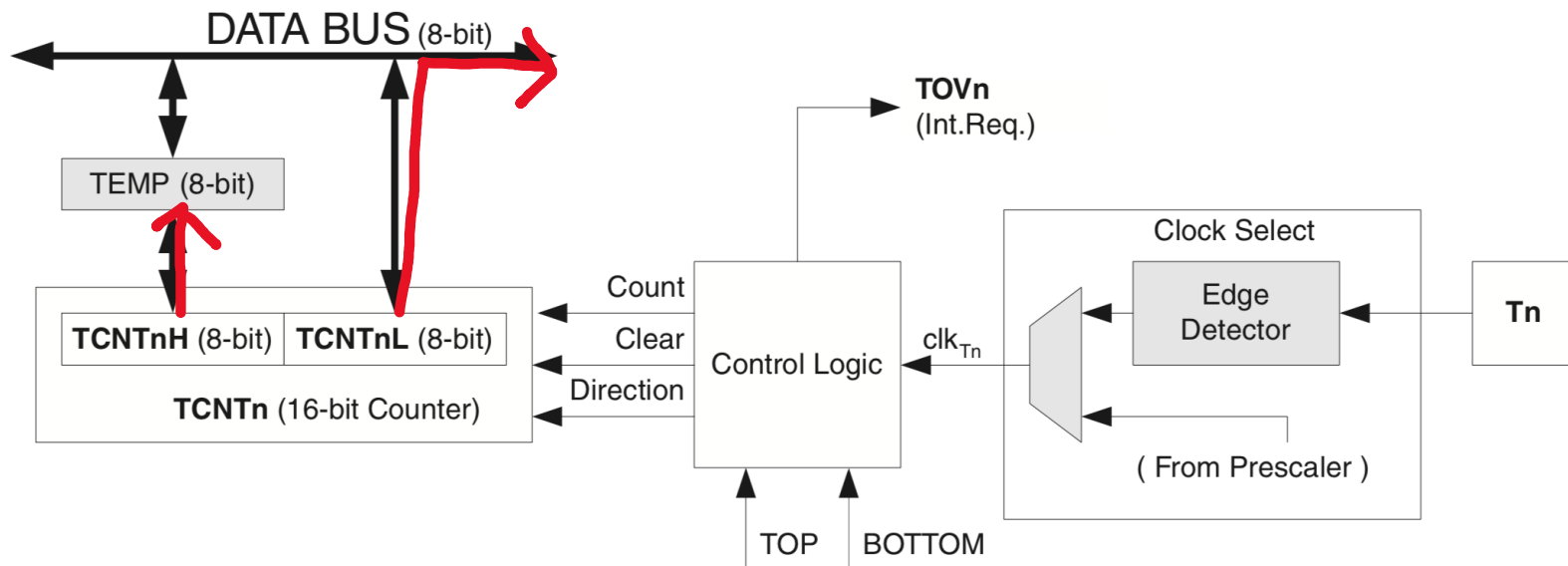
# Why write higher byte first, read lower byte first?

**Figure 47.** Counter Unit Block Diagram



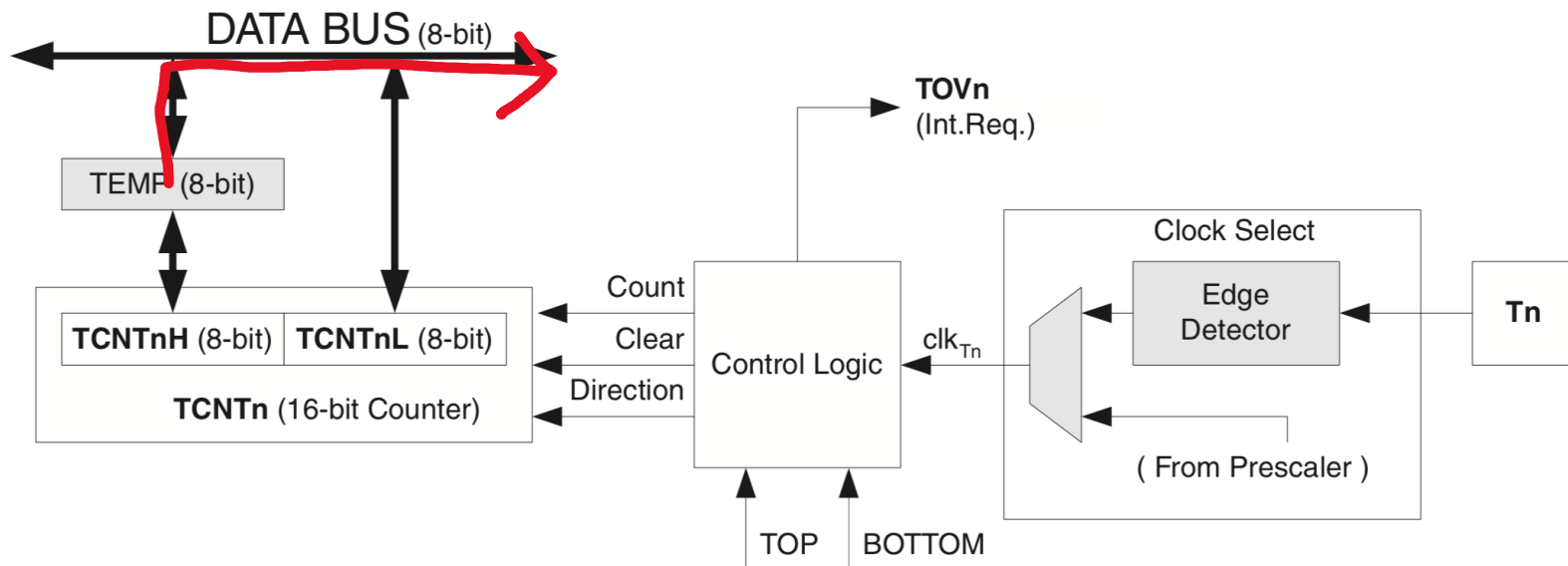
# Why write higher byte first, read lower byte first?

**Figure 47.** Counter Unit Block Diagram



# Why write higher byte first, read lower byte first?

**Figure 47.** Counter Unit Block Diagram





# Read/Write 16bit Register

- Write 16 bit-register
  - `sts TCNTIH, r17` ; write to high byte first
  - `sts TCNTIL, r16` ; write to low byte second
- Read 16 bit-register
  - `lds r16, TCNTIL` ; read from low byte first
  - `lds r17, TCNTIH` ; read from high byte second



# PWM Output

## Alternate Functions of Port B

Port Pin	Alternate Functions
PB7	OC0A/OC1C/PCINT7/ $\overline{\text{RTS}}$ (Output Compare and PWM Output A for Timer/Counter0, Output Compare and PWM Output C for Timer/Counter1 or Pin Change Interrupt 7 or UART flow control RTS signal)
PB6	OC1B/PCINT6/OC.4B/ADC13 (Output Compare and PWM Output B for Timer/Counter1 or Pin Change Interrupt 6 or Timer 4 Output Compare B / PWM output or Analog to Digital Converter channel 13)
PB5	OC1A/PCINT5/ $\overline{\text{OC.4B}}$ /ADC12 (Output Compare and PWM Output A for Timer/Counter1 or Pin Change Interrupt 5 or Timer 4 Complementary Output Compare B / PWM output or Analog to Digital Converter channel 12)
PB4	PCINT4/ADC11 (Pin Change Interrupt 4 or Analog to Digital Converter channel 11)
PB3	PDO/MISO/PCINT3 (Programming Data Output or SPI Bus Master Input/Slave Output or Pin Change Interrupt 3)
PB2	PDI/MOSI/PCINT2 (Programming Data Input or SPI Bus Master Output/Slave Input or Pin Change Interrupt 2)
PB1	SCK/PCINT1 (SPI Bus Serial Clock or Pin Change Interrupt 1)
PB0	$\overline{\text{SS}}$ /PCINT0 (SPI Slave Select input or Pin Change Interrupt 0)



# Duty Cycle

- Change Duty Cycle to control speed

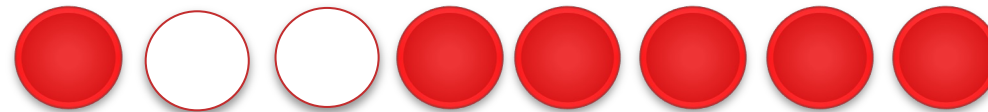
- 100% duty cycle – Halt



- 50% duty cycle - Half Speed



- 0% duty cycle - Full Speed



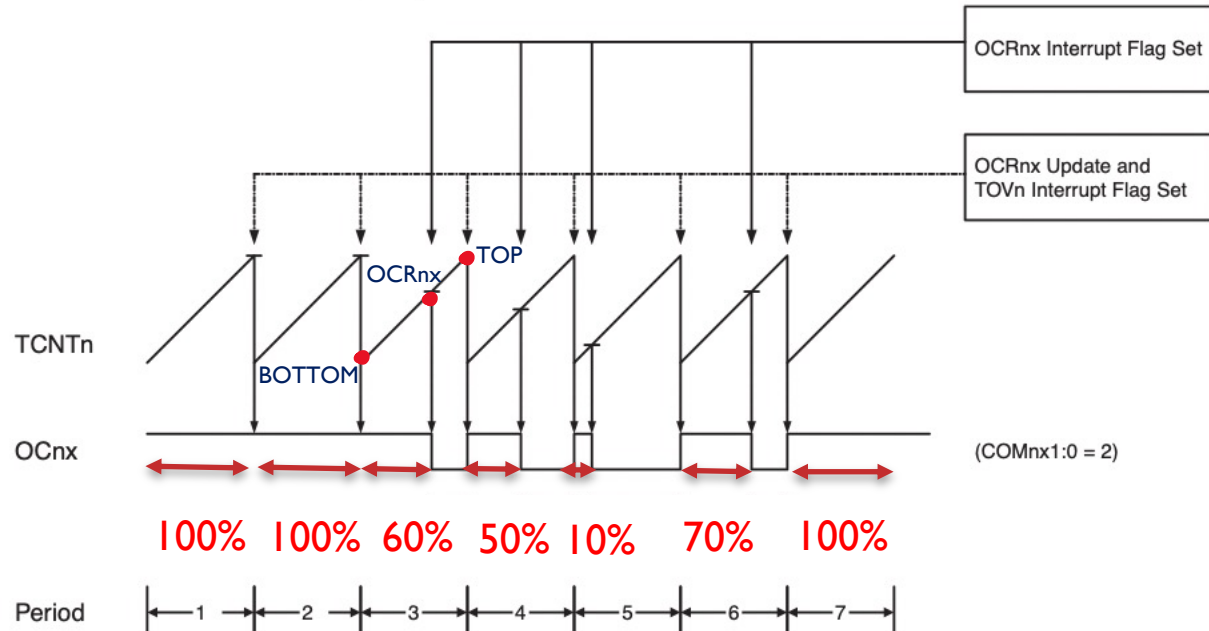
- Use Output Compare Register (OCRnx)

- Timer/Counter 1A: OCR1A

- Timer/Counter 1B: OCR1B

# Fast PWM mode

Figure 13-6. Fast PWM Mode, Timing Diagram



Generate waveform with varying duty cycle and fixed frequency.

The counter counts from BOTTOM to TOP then restarts from BOTTOM.

When OCRnx interrupt flag is set, Ocnx is cleared.

# 16-bit Timer/Counter Control Register

	Timer/Counter 1A		Timer/Counter 1B		Timer/Counter 1C				
Bit	7	6	5	4	3	2	1	0	TCCR1A
	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

**TCCR1A**

Bit	7	6	5	4	3	2	1	0	TCCR1B
	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

**TCCR1B**

**Wave Generation Mode (WGM)**

**Compare Output Mode (COM)**

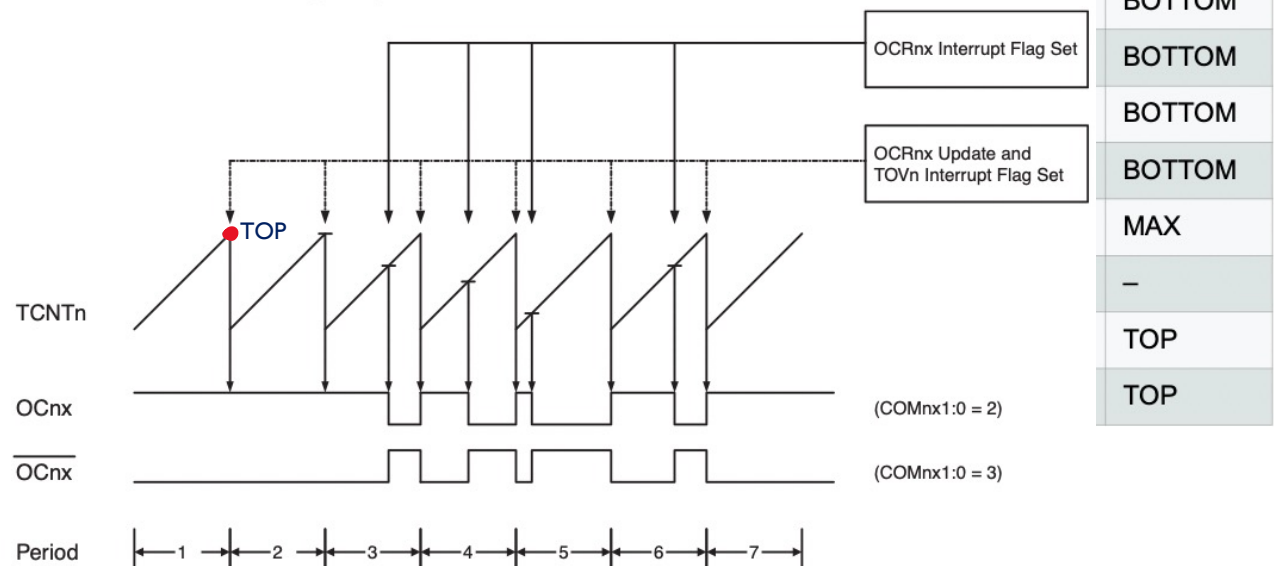
**Clock Selection (CS)**



# Wave Generation Mode (WGM)

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnx at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	TOP	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	TOP	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	TOP	TOP

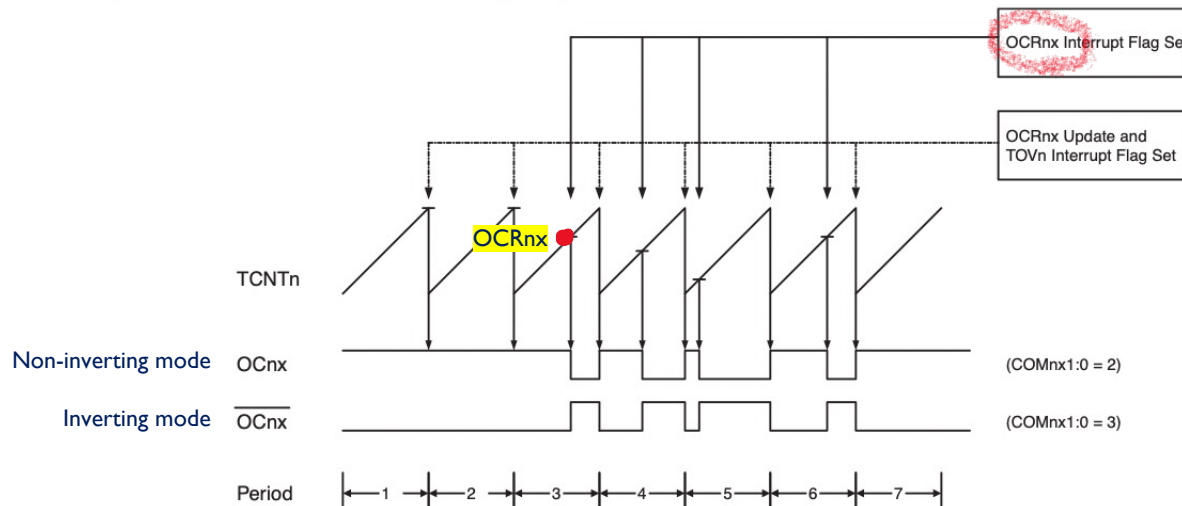
Figure 13-6. Fast PWM Mode, Timing Diagram



# Compare Output Mode (COM)

COMnA1/COMnB1/COMnC1	COMnA0/COMnB0/COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	Toggle OCnA/OCnB/OCnC on compare match
1	0	Clear OCnA/OCnB/OCnC on compare match (set output to low level) <i>Non-inverting mode</i>
1	1	Set OCnA/OCnB/OCnC on compare match (set output to high level) <i>Inverting mode</i>

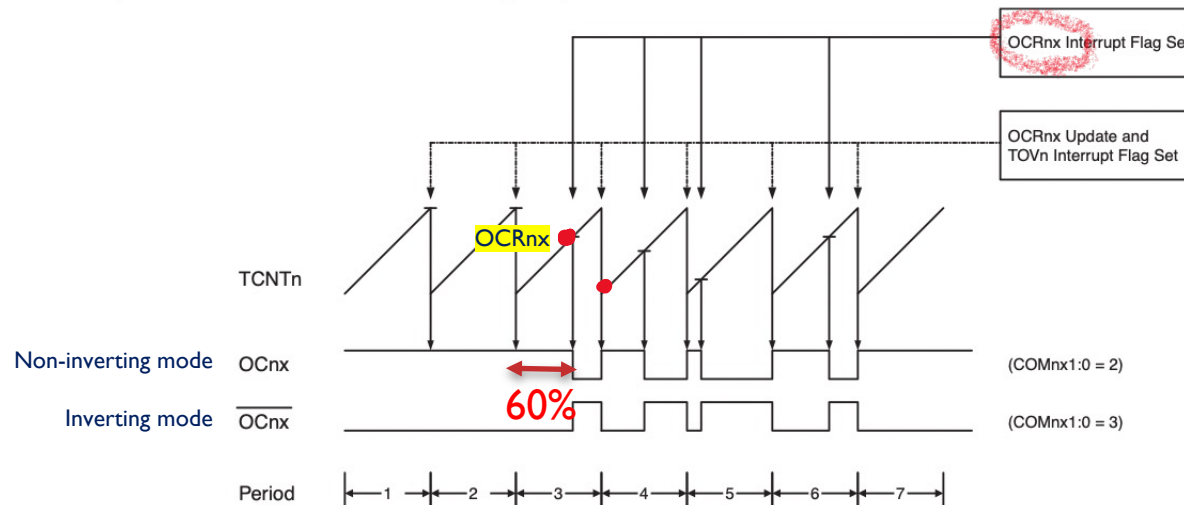
Figure 13-6. Fast PWM Mode, Timing Diagram



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Figure 13-6. Fast PWM Mode, Timing Diagram

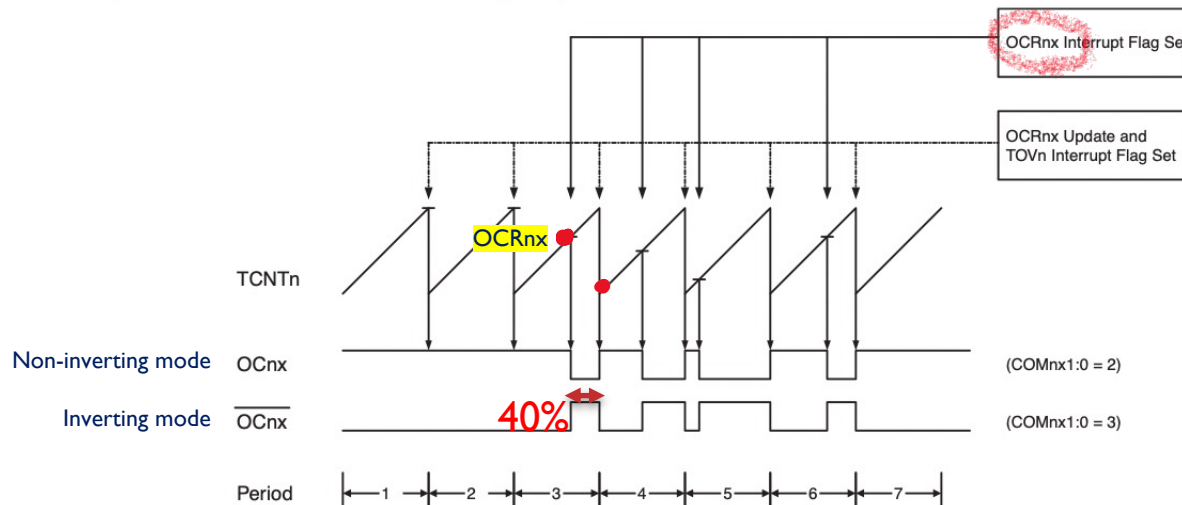




# Compare Output Mode (COM)

COMnA1/COMnB1/COMnC1	COMnA0/COMnB0/COMnC0	Description
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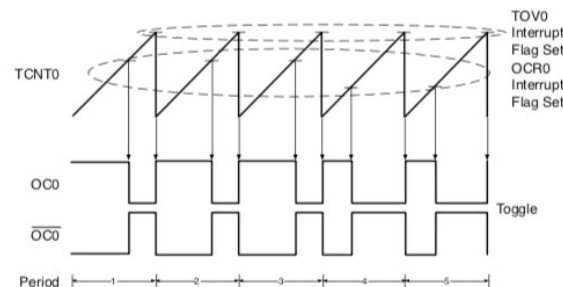
Figure 13-6. Fast PWM Mode, Timing Diagram



# Clock Selection (CS)

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	clk <sub>I/O</sub> /1 (No prescaling)
0	1	0	clk <sub>I/O</sub> /8 (From prescaler)
0	1	1	clk <sub>I/O</sub> /64 (From prescaler)
1	0	0	clk <sub>I/O</sub> /256 (From prescaler)
1	0	1	clk <sub>I/O</sub> /1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

## Fast PWM Mode



- Uses both OCF0 and TOV0
  - Clear OC0 on output compare match, set OC0 at TOP
- Can generate waveform with varying duty cycle and fixed frequency

$$f_{PWM} = \frac{clk_{I/O}}{prescale \cdot 256}$$

# Demo Check

- 16 speed levels
- PORTB 0-3 indicate current speed level
- PORTB 5,6 brightness change
- 3 Functions for Control Speed
  - SPEED\_DOWN
  - SPEED\_UP
  - SPEED\_MAX
- Speed levels bound max and min
- Single button press results single action

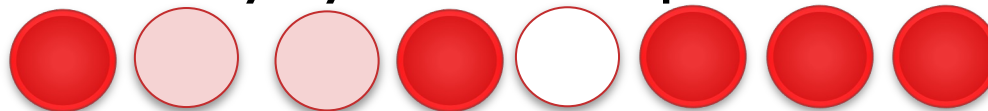
# Speed control

- Change Duty Cycle to control speed

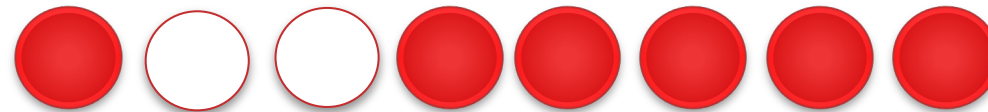
- 100% duty cycle – Halt



- 50% duty cycle - Half Speed



- 0% duty cycle - Full Speed



# Check-off Lists

- Correct settings for PWM-related registers.
- Correct speed changes of each switch buttons.
- Single change from a single press.
- No overflow or underflow for speed-level.

# Announcements

- Read Atmega32u4 Datasheet
  - 74p (Alternate Functions of Port B)
  - 94p - 139p (Timer/Counter)



# Questions?

