INTERNATIONAL UNIVERSITY OF SARAJEVO

JANUARY 2018.

CS303 DIGITAL DESIGN

FINAL EXAM

STUDENT NAME & ID: _____

DATE: _____

Instructions:

• Examination time: **120 min**.

• Write your **name** and **student number** in the space provided above.

• This examination is **closed book**.

• There are 3 questions. The points for each question are given in the square brackets, next to the question title. The overall maximum score is **100**. This final exam **weighs 40%** of your **final grade.**

• Answer each question in the space provided. If you need to continue an answer onto the back of the sheet, clearly indicate that and label the continuation with the question number.

QUESTION	1	2	3
POINTS	/21	/30	/49
		TOTAL	/100

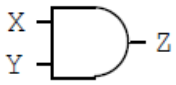
1. Mark the correct statement(s) (21 %)

1.1 Converting the number $154_{(10)}$ to base 8 gives the following result: **[3]**

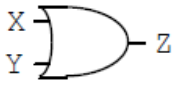
a) 108, b) -232, c) 254, d) 232.

1.2 Which of the following gates is represented by the shown truth-table? **[3]**

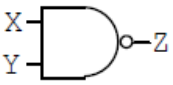
A.



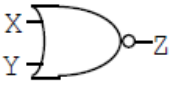
B.



C.



D.



X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

1.3 The minimum number of **NAND** gates (only!) with which it is possible to implement a three-input **OR** gate is (hint: use DeMorgan's theorem): **[3]**

a) 3, b) 5, c) 6, d) It is not possible to do.

1.4 What is the minimum number of flip-flops needed to build a counter that counts uninterrupted sequence from 0 to 12? **[3]**

a) 2, b) 3, c) 4, d) It is not possible to do.

1.5 Which of the following is a valid rule of Boolean algebra: **[3]**

a) $x \cdot 0 = x$, b) $x \cdot x' = 1$, c) $x \cdot x = x$,
d) $x \cdot 1 = 1$, e) $1 + 0 = 0$, f) None of these

1.6 Which of the following equations is the un-simplified Sum-Of-Products equation for the truth table shown? **[3]**

A	B	C	F_{13}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

a) $AB'C + AB'C' + A'B'C + A'B'C'$,

b) $A'B'C' + A'B'C + A'BC + AB'C$,

c) $(A + B' + C)(A' + B + C)(A' + B' + C)(A' + B' + C')$,

d) $(A' + B + C')(A + B' + C')(A + B' + C')(A + B + C)$

1.7 What is the decimal equivalent to the binary number expressed in 2's complement notion 010110_2: **[3]**

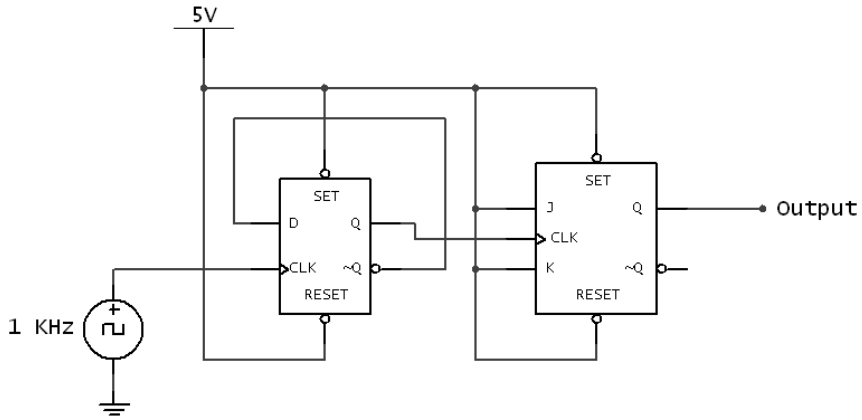
a) 22, b) -22, c) -42, d) 42.

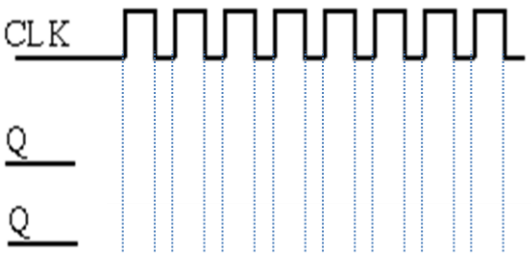
2. Logic gates and components (30%)

2.1 Sketch a negative-edge triggered JK type flip flop as a single block! Write down its excitation table and truth table. What asynchronous inputs could it have? **[8]**

2.2 Implement the functions of a full adder (SUM and Carry Out) using 4x1 multiplexers and external gates. Use back of the sheet. **[8]**

2.3 Determine the output frequency for the circuit shown below. You can sketch the time diagram of the clock and output to argument for your answer. Note that 5V is logical "1" and the clock is a 1kHz square wave signal. **[8]**





2.4 Your RAM consists of four 32Mx16 RAM chips. A decoder enables only one of the four chips at a time. What is the total capacity of the memory**?** What are the width and depth of the memory**?** How many address bits are connected to each memory chip, and how many are connected to the decoder**?** **[6]**

3. VHDL + Finite State Machine Design exercise (49%)

3.1 How do the following two code fragments differ? Be specific and answer the questions below:

```
PROCESS
BEGIN
WAIT UNTIL (CLock'EVENT AND Clock='1');
IF reset='1' THEN
  Q2<='0';
        ELSE
        Q2<=D;
        END IF;
        END PROCESS;
```

```
PROCESS (Reset,Clock)
BEGIN
IF reset='1' THEN
  Q3<='0';
        ELSEIF (Clock'EVENT AND Clock='1')
THEN
        Q3<=D;
        END IF;
        END PROCESS;
```

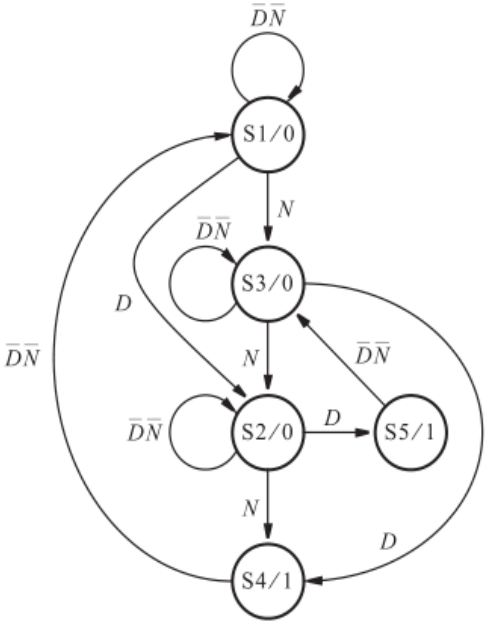
a) When PROCESS begins in both fragments? What is the difference? [4]

b) What are the output conditions in each? [4]

c) Which flip-flop is specified by each fragment? [4]

d) Are those flip-flops rising or falling edge, with synchronous or asynchronous reset? [4]

3.2 Figure to the right shows state diagram of vending machine. The vending machine accepts nickels and dimes. All electronic signals in the vending machine are synchronized to the **positive edge** of a Clock signal. The vending machine's coin-receptor mechanism generates two signals, **senseD** and **senseN**, which are asserted when a dime or a nickel is detected. Assume that the coin receptor also generates two other signals, **D** and **N**. The D signal is set to 1 for one clock cycle after senseD becomes 1, and N is set to 1 for one clock cycle after senseN becomes 1. Note that it is not possible to have both D and N set to 1 at once.



a) How many flip-flops would be necessary to implement this state machine? Would state machine be Mealy or Moore type, if implemented according to the given state diagram? [4]

b) With two inputs D and N and five states the FSM can attain, how big is the state table, not counting the impossible inputs (D=1 and N=1) and unused states? Explain! [4]

c) Now complete the VHDL code for vending machine control. [25]

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY vending_machine IS
PORT (_____________________________
      _____________________________
      _____________________________
      _____________________________);
END vending_machine;

ARCHITECTURE behavior OF vending_machine IS

TYPE State_type IS (S1,S2,S3,S4,S5);
SIGNAL y:_____________________________;

BEGIN
PROCESS (Reset1,Clock)
BEGIN
IF Reset1='0' THEN
_____________________________________
ELSIF (Clock'EVENT AND _____________) THEN
CASE y IS

WHEN S1=>
IF N='1' THEN _____________________________;
ELSIF  D='1'  THEN _____________________;
ELSE _____________________________________;
END IF;

WHEN S2=>
      _____________________________________;
      _____________________________________;
      _____________________________________;
END IF;

WHEN S3=>
      _____________________________________;
      _____________________________________;
      _____________________________________;
END IF;

WHEN S4=>
      _____________________________________;

WHEN S5=>
      _____________________________________;

END CASE;
END IF;
END PROCESS;


_____________________________________________;
END behavior;
```