260 HW 7 pipelining

1) Assume No read and write same time, no bypass, 1 mem unit no r/w same time

$$CPI = \frac{\text{cycles}}{\text{instruction}} = \frac{(17 \text{ cycles per loop}) 100 \text{ loop executions} + 2 \text{ cycles}}{(5 \text{ loop instructions}) 100 \text{ loops} + 2 \text{ instructions}} = 3.39 \text{ CPI avg}$$

2) Assume R/W register, no bypass, 1 mem unit no r/w same time

$$CPI = C/I = \frac{16 \cdot 100 + 2}{5 \cdot 100 + 2} = 3.19 \text{ avg CPI}$$

3) Assume R/W, no bypass, Mem can r/w same time

$$CPI = C/I = \frac{14(100)+2}{5(100)+2} = 2.79 \text{ avg CPI}$$

4) Asume R/W regs bypass, mem r/w same time

$$CPI = C/I = \frac{12(100)+2}{502} = 2.39 \text{ avg CPI}$$

5) Assume code executed on 2GHz processor. What is execution time? Can code be changed to be faster?

$$\text{time} = \frac{\text{Avg CPI} \cdot \text{IC}}{\text{freq}} = \frac{(2.39 \text{ AvgCPI}) \cdot 502}{2 \cdot 10^9} = 599.9 \text{ ps} = .6 \text{ ns}$$

time = avg CPI · IC · cycle-time $(1/2 \cdot 10^9) = 599.89$

Code can be faster by switching add and addi to avoid a memory problem (addi and sw use $s1)