Computer Organization HW2

Verilog files and explanations:

* Mux3x2\_64
  + Basically two 2x1 64 bit multiplexers under the hood.
* Mux3x2\_32
  + Basically two 2x1 32 bit multiplexers under the hood.
* Mux2x1\_32
  + 32 lines of 2x1 multiplexer.
* Mux2x1
  + Simplest form of a multiplexer where 2 one bit input and 1 one bit output with one bit selector.
* Datapath
  + Datapath of mult32, it has 3x2 64 bit multiplexer to select what to write to the output product, there’s also two lines of 2x1 32 bit multiplexers to reset the product to its initial value where its lesser half is multiplier. It also has adder where greater half of product and multiplicand is added always and is written when write is 1. To assign product0 a simple or gate is used.
* Control
  + Control has two main always blocks one for updating the state and one for updating outputs both depend on current state but state update block also depends on the input product0
* Add32
  + Uses 32 full adders to add corresponding digits of given inputs.
* Mux3x8
  + Takes an 8 bit input and returns one of its digits depending on the given selector. Implemented with “and” and “not“ gates and doesn’t uses smaller multiplexers inside.
* Alu32
  + The main module of the project, performs all 8 operations always, and puts the corresponding result to the output by using mux3x8 for every digit of all operations.
* Full\_adder
  + The full adder we all know.
* Sub32
  + Takes two’s complement of second input and performs addition on them.
* Xor32
  + Performs one bit xor on all 32 bits of given inputs.
* And32
  + Performs one bit and on all 32 bits of given inputs.
* Or32
  + Performs one bit or on all 32 bits of given inputs.
* Nor32
  + Performs one bit nor on all 32 bits of given inputs.
* Slt32
  + Performs subtraction of given inputs and returns the leftmost digit of the result.