

Assignment9 - Due: Friday, October 30th, 5pm

CSE/EEE230 Assignment9

Friday, October 30th, 5pm

***Important: This is an individual assignment. Please do not collaborate.
Do not share your solution with anyone.***

Make sure to follow the academic integrity policies.

It must be submitted on-line (course website)

The document needs to be 100% typed (no hand written answers) If it is not typed, it will be zero on the assignment.

Upload your file containing your solution to the course website by the assignment deadline. PDF, word (.doc, docx), and power point (.ppt, pptx) files are accepted.

20 points total (This assignment will be counted towards your grade).

No late assignment will be accepted

Objectives:

- understand and compute clock cycles, clock rates, CPI, CPU time, and instructions per second.
- understand what signals the control unit sends to the datapath in order to control the execution of instructions.
- extend the MIPS single-cycle design to implement additional instructions.

Assignment Description:

1. (1 pt) Suppose you wish to run a program P with 41.5×10^9 instructions on a 20 GHz machine with a CPI of 0.85. What is the expected CPU time to execute this program on this machine?

2. (6 pts) Consider two different implementations, I1 and I2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. I1 has a clock rate of 4 GHz, and I2 has a clock rate of 5 GHz. The average number of cycles for each instruction class on I1 and I2 is given in the following table:

Class	CPI on I1	CPI on I2	C1 Usage	C2 Usage	C3 Usage
A	4	2	35%	25%	15%
B	3	4	40%	30%	50%
C	1	2	25%	45%	35%

The table also contains a summary of average proportion of instruction classes generated by three different compilers, C1, C2, and C3. Assume that each compiler uses the same number of instructions for a given program but that the instruction mix is as described in the table.

- Using C1, compute the average CPI for each of I1 and I2. Then compute the speed, that is the average number of instructions per second for each of I1 and I2. Then decide which one is faster than the other? and in what ratio?
- Using C2, compute the average CPI for each of I1 and I2. Then compute the speed, that is the average number of instructions per second for each of I1 and I2. Then decide which one is faster than the other? and in what ratio?
- Using C3, compute the average CPI for each of I1 and I2. Then compute the speed, that is the average number of instructions per second for each of I1 and I2. Then decide which one is faster than the other? and in what ratio?
- If you purchased I1, which compiler has a better performance than others?

e). If you purchased I2, which compiler has a better performance than others?

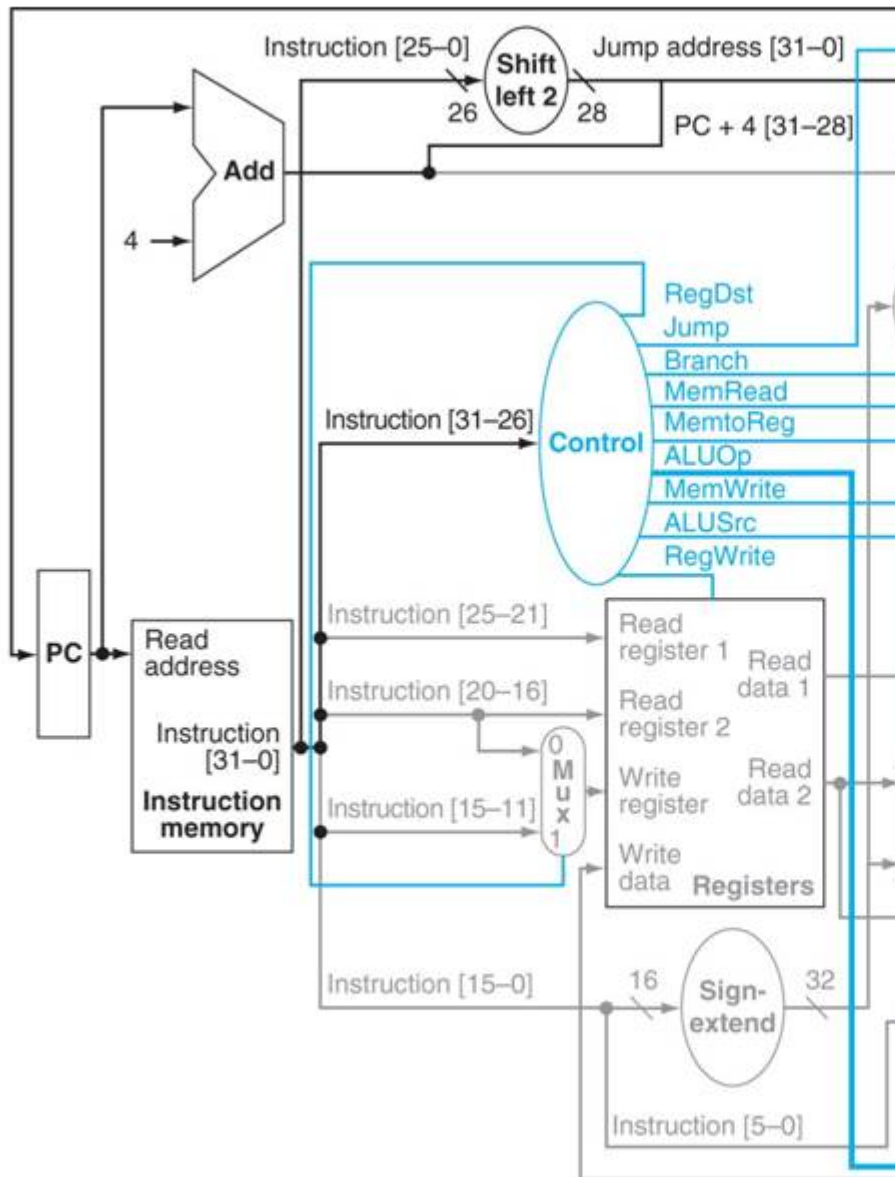
f). Which combination of computer and compiler has the best performance if all other criteria were identical, including cost?

3. (3 pts) Determine which MIPS assembly instruction(s) if any, that we discussed in class (R-format (including add, sub, or, and, nor, slt), lw, sw, beq, j) will not work correctly and explain what will happen instead, if each of the following control signals in the single-cycle datapath that we saw in class (shown below) is always stuck at one value specified below:

a). ALUSrc = 1 (always stuck at 1)

b). Branch = 1 (always stuck at 1)

c). ALUOp0 = 1 (always stuck at 1)



4. (5 pts) We would like to add the “srl” (shift right logical) instruction to the single cycle datapath discussed in class. You will need to feed the shamt field to the ALU so that it can shift using the shift amount. (You can assume that the ALU has an implementation of shift right logical if a shift amount and an integer to be shifted are inserted and its ALUOp is 11.) Trace which datapaths in the following picture are used to perform the “srl” instruction by marking the paths, and add datapath(s) and control signal(s) to the single-

cycle datapath for the “srl” instruction, if it is necessary. (You should also make sure that previously existing instructions such as R-format (add,sub,and,or,slt), lw, sw, and beq still work with this additional instruction.) Download the following PDF/JPG file, use some software (for instance, Microsoft Paint) to draw any new datapath(s) and signal(s) using red color.

(You can copy & paste your image back into your document such as MS Word.) Explain when the new signal(s) that you chose is set to 0, and also 1, if any. Also specify the value of other existing control signals RegDst, ALUSrc, MemtoReg, RegWrite, MemRead, MemWrite, Branch, ALUOp0, and ALUOp1.

Download the figure from here.

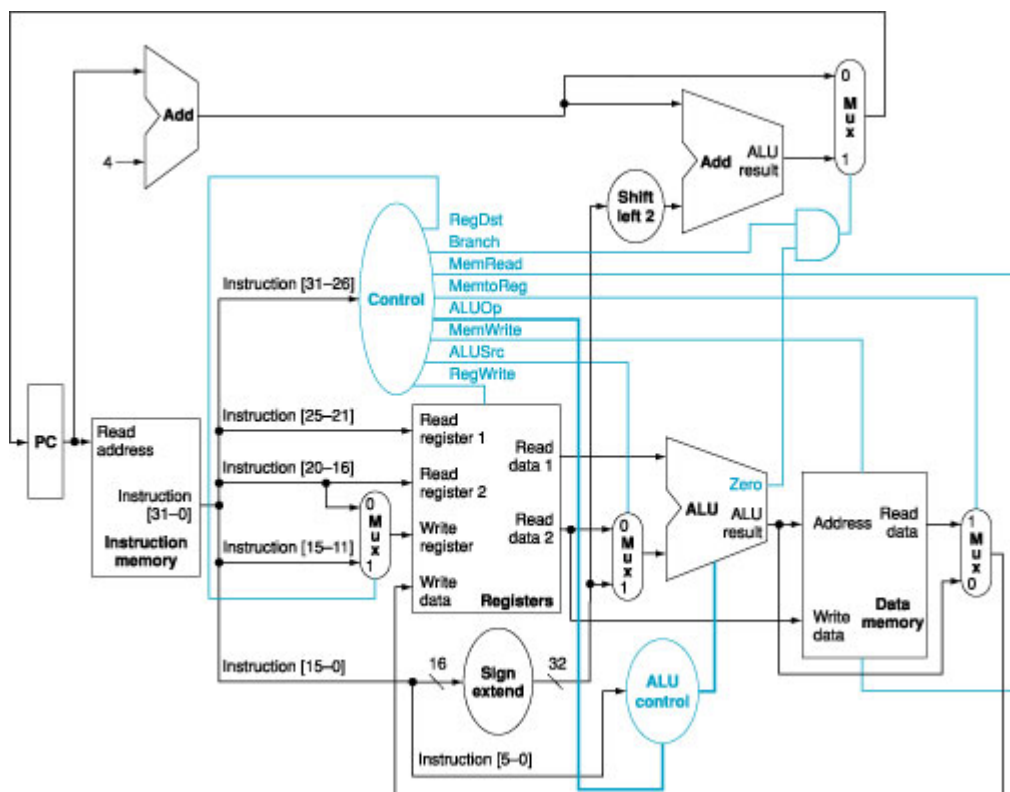
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hw9_Figure_SingleCycle.pdf

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5. (5 pts) We would like to add the “jr” (jump register) instruction to the single cycle datapath discussed in class. Trace which datapaths in the following picture are used to perform the “jr” instruction by marking the paths, and add datapath(s) and control signal(s) to the single-cycle datapath for the “jr” instruction, if it is necessary. (You should also make sure that previously existing instructions such as R-format (add,sub,and,or,slt), lw, sw, and beq still work with this additional instruction.) Download the following PDF/JPG file, and use some software (for instance, Microsoft Paint) to draw any new datapath(s) and signal(s) using red color.

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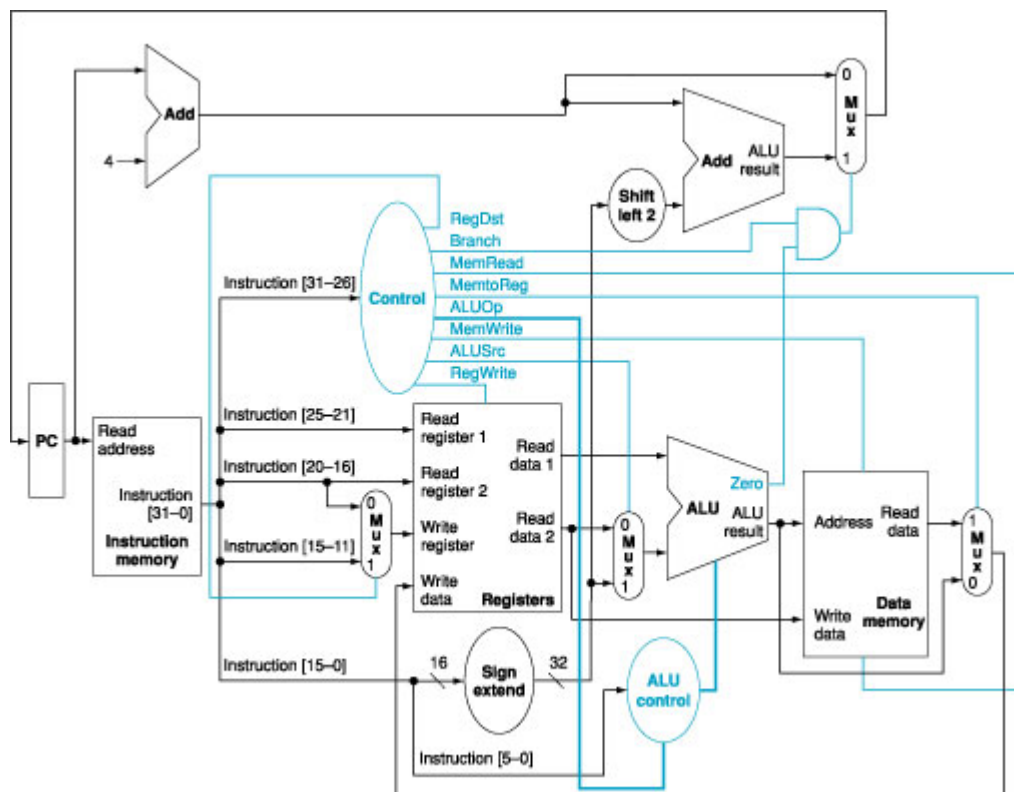
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