# Synchronization Performance Evaluation of Reference Clock Connection Methods for IEEE 1588 Master Clocks

Tamás Kovácsházy
Department of Measurement and Information Systems
Budapest University of Technology and Economics
Budapest, Hungary
khazy@mit.bme.hu

***Abstract*—Clock and/or frequency synchronization is a common requirement in modern distributed measurement and control systems, such as Internet of Things (IoT). The required precision is application dependent; however, the possibility of sub 1 microsecond precision provided by low-cost advanced IEEE 1588 implementations sets the industry standard today. The performance and price of IEEE 1588 implementations are primarily defined by the master clocks and their actual installation and configuration. The paper investigate how master clock architectures, i.e., how the master clock is connected to the reference clock, influence price and performance; and in addition, it also details how the architecture effects installation and configuration requirements. The primary factors of investigation are ambient temperature and delay compensation required due to signal transmission time. The paper also introduces the architecture and performance of a Linux based open source/hardware prototype master clock developed by the authors.**

***Keywords—Distributed Measurement and Control, Precision Clock Synchronization, IEEE 1588, Reference Clock Connection***

## I. INTRODUCTION

Clock and/or frequency synchronization are fundamental requirements in most of the distributed measurement and control systems, only the required precision is an opened question. The concept of Internet of Things (IoT) also increases the need for such solutions as globally synchronized sampling and actuation are common requirements in this type of specialized distributed applications. However, providing the required precision is shown to be theoretically impossible using a software only solution such as NTP [1], the main reason for this is that IoT is foreseen as a TCP/IP based none real-time distributed network embedded system. The IEEE 1588 Precision Time Protocol (PTP) [2] has been developed by IEEE to solve this issue, i.e., it is primarily designed for Ethernet and/or TCP/IP networks, and therefore, also applicable for IoT. IEEE 1588 aims to provide sub 1 microsecond precision, and with proper components and system architecture even sub 100 ns precision is readily achievable. The typical GPS reference clock based architecture of IEEE 1588 is depicted in Fig. 1.

The precision of an IEEE 1588 solution primarily depends on the components, especially the master clock that provides the timing information to the system. The master clock is a network node acting as timing master for all network connected slaves synchronizing to the master.

The master clock synchronizes itself to a reference clock providing global time information, most cases using Coordinated Universal Time (UTC) time format. An estimation of the reference clock's actual global time is provided by a Global Positioning System (GPS) receiver for the master clock nearly exceptionally. When the GPS time information is not available due to malfunctions, weather effects, or GPS jamming, the master clock keep time based on a precision local clock. This situation is called holdover, and the master clocks timing performance during this situation is called holdover

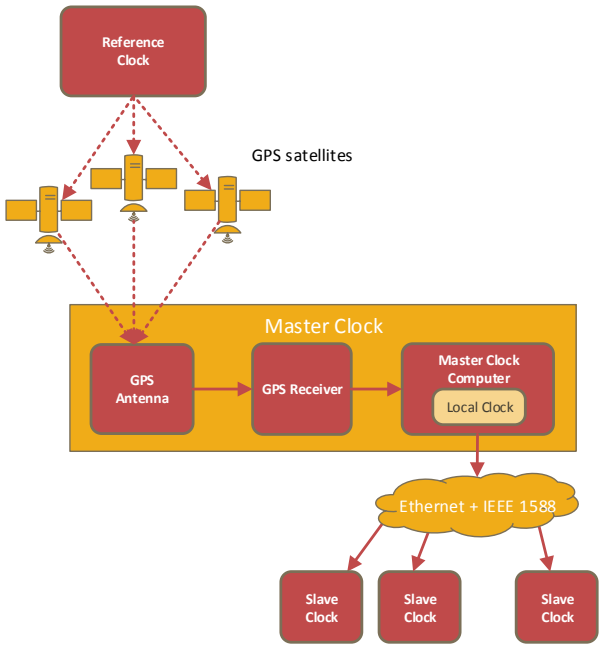


Fig. 1. Architecture of IEEE 1588 solutions with the high level internal architecture of the master clock

performance. The master clock communicates the local time information based on the GPS and/or the local clock to the slaves using IEEE 1588 standard messages using the International Atomic Time (TAI) format. TAI is currently (early 2015) ahead of UTC by 35 seconds, the actual difference changes when Leap Seconds are introduced to UTC.

### *A. Components of a Master Clock*

The master clock has the following main components as shown in Fig. 1.:

- GPS antenna,
- GPS antenna to GPS receiver connection,
- GPS receiver,
- GPS receiver to Master Clock Computer connection,
- Precision Local Clock,
- Master Clock Computer.

Various bands of the GPS signal are in between 1.1 GHz and 1.6 GHz, and they are very weak on ground level. In building reception of GPS signal is practically impossible due to the high frequency and the weakness of the signals, but even if it would be possible, not line of sight signal transmission would render timing (and also localization) unacceptably imprecise. Therefore, GPS antennas must be located outside of buildings in timing applications, primarily on rooftops, to provide a clear and unobscured view of at least 4 satellites in any time during operation.

The GPS signal is transmitted from the antenna to the GPS receiver using coaxial cable except if we use an antenna integrated GPS receiver, which are currently rare in timing applications (antenna integrated GSP receivers are designed for the portable equipment market, so they tend to be less precise in timing applications). Coaxial cables have a specific attenuation limiting the usable cable length, and they delays the signals causing timing error also. In addition, this cable must be pulled in and terminated with connectors increasing installation time and expenses. Furthermore, as most cases the coaxial cable leads from the outside of the building inside, EM protection must be also installed on it on the building boundary to reduce the effects of external EM events, such as lightning strikes, to the internal equipment.

The GPS receiver works out a local estimation of the reference clock. The precision (worst-case difference of the local estimation of time and the reference time) of specialized timing GPS receiver can be in the range of or under 10-20 ns if the GPS antenna is deployed to a proper location with good signal reception, and antenna cable delay is properly taken into account during the estimation. All timing GPS receivers assumes stationary location, i.e., the GPS receiver does not move during operation. The GPS receiver communicate time information with a Time of Day and Pulse per Second (PPS) outputs to the Master Clock Computer. The Time of Day output is typically a logic level asynchronous serial port (UART) conveying time in a specified format. Most cases the Time of Day output is also used to configure the GPS receiver and get additional information from it (both transmit and receive functions of the UART are used). The PPS signal is also a logic signal whose rising edge is generated by the GPS receiver when the local estimation of the reference clock advances seconds. Therefore, the timing precision of the GPS receiver is measured comparing the PPS output to GPS receiver to the PPS output of a locally available reference clock (calibration).

The Time of Day and PPS signals must be received by the Master Clock Computer. The connection between the GPS receiver and the Master Clock Computer strongly depends on the architecture of the master clock. For short, internal connection logic signals can be used. In this case the GPS receiver must be in the same equipment chasses than the Master Clock Computer. In other architectures, the distance in between these two components can be in the range of tens or even hundreds of meters; and therefore, the connection must be implemented using a solution capable to provide long range communication over some cabling infrastructure. This approach introduces additional problems, as long range communication requires special transceivers (to convert logic signals to long range signaling solutions such as RS422 or RS485), galvanic isolation to reduce problems due to ground loops and to fulfill safety requirements, and EM protection. All of these solutions increase delay and jitter also, reducing timing precision.

The Master Clock Computer is an embedded computer or a regular server computer capable of receiving Time of Day and PPS information are received from the GPS receiver to synchronize the local clock to the reference clock. An Ethernet interface is used to send IEEE 1588 messages to allow slave clock to be synchronized to the local clock. Both PPS signals and IEEE 1588 messages must be timestamped with high precision using the local clock in hardware for providing high precision. Software timestamping is not sufficient for sub 1 microsecond precision as software execution time jitter is well over 1 microsecond.

### *B. Factors Influencing precision*

The primarily factors influencing master clock precision are the delay and jitter caused by these components on signals relevant to timing, and the dependence of the delay and jitter on other factors, such as temperature, electromagnetic noise, power supply voltage fluctuations, etc. Out of these secondary factors temperature is the most influential one; especially, as some components are located outside of the building on a rooftop, where temperature can change tens of degree centigrade in minutes due to weather effects such as summer thunderstorms, etc. Therefore, in this paper delay and jitter of components are investigated only as the function of temperature, no other secondary factors are taken into account.

## II. MASTER CLOCK ARCHITECTURES AND THEIR EVALUATION

As it was detailed in the introduction, the master clock can be a distributed system itself, there are three typical architecture common in implementations. These architectures are the following:

- External GPS antenna with integrated internal master clock computer and GPS receiver with (External Antenna based architecture from now),
- External device integrating all components into a GPS antenna like device (Antenna-integrated architecture from now),
- External GPS antenna and receiver connecting to the master clock computer inside using digital domain connections (External Integrated GPS architecture from now).

The architecture can be investigated from the point of view of:

- Maximum cable distance and required cable types used in the architecture,
- Delay and jitter dependence on installation and temperature,
- Delay and jitter compensation for precise timing.

### *A. Evaluation of the External Antenna based Architecture*

The installation of this architecture is limited by the applicable coaxial cable length primarily, which is defined by cable quality (attenuation on the used frequencies) and Antenna and receiver sensitivity. Available quality high frequency coaxial cables limit the distance in between the GPS antenna to the integrated master clock to 20-40 meters even in case of active GPS antennas (active antennas consist an antenna amplifier and they receive power also through the coaxial cable). In addition, the selected cable must be pulled in between the rooftop antenna mounting and the integrated master clock which is located in cable cabinets or server rooms somewhere in the building.

The delay caused by cable length must be compensated as every meter of coaxial cable delays the signal with approximately 5 ns. As an example, an uncompensated 10 m long cable reduces the error budget of the whole system (1 µs worst case) with approximately 50 ns (5% of worst case error). Therefore, the delay caused by the installed cable must be measured using time domain reflectometry to determine the cable delay, and the measured cable delay must be configured in the integrated master clock through its configuration interface. Compensation is done by the integrated master clock based on this static setting. Therefore, if the cable connecting the GPS antenna and the integrated master clock changes, delay compensation must be done again manually, resulting in system downtime. Cable delay is constant and does not depend on temperature significantly, so manual cable compensation is sufficient to achieve the required precision.

The widely used RG-58 coaxial cable has too high attenuation for GPS signals (approximately 60 dB/100m at 1.6 GHz), so it can be used for relatively short distances, under 10 meters only. To increase the potential distance between the GPS antenna and the GPS receiver using lower quality cables such as RG-58, some master clock use down-converting GPS antennas. These GPS antennas not only amplify GPS signals, but also down-convert them to lower frequencies (for example, in the range of 10-100 MHz). In this case a special GPS receiver must be used in the integrated master clock capable of receiving these down-converted GPS signals. For example the GPS antennas and receivers in master clocks manufactured by MEINBERG RADIO CLOCKS GmbH apply this down-converting scheme making possible to use even 200 meters of RG-58 cables.

Fig. 2. Antenna-integrated OTMC 100 IEEE 1588 master clocks (yellow-black and red-black devices) and its management interface on a rugged portable device.

The holdover performance of these solutions are quite good, as the local clock of the device operates in an internal environment, most cases in a temperature controlled server room. In addition, as there is no device size or power consumption limit introduced due to the internal location of the master clock, oven controlled oscillators (OCXO) or Rubidium clocks can be used as local clock frequency sources providing high accuracy and stability even if the GPS signal unavailable.

### *B. Evaluation of the Antenna-integrated Architecture*

The Antenna Integrated Architecture houses all components into a GPS antenna like case and locates it on the rooftop of the building. Therefore, an antenna integrated master clock is connected to the network using a standard Ethernet interface electronically, and cable length is measured and compensated by the IEEE 1588 implementation running on the master clock without external intervention or human interaction. Antenna integrated master clocks are powered over the Ethernet cable using the Power over Ethernet (IEEE 802.3af-2003 or IEEE 802.3at-2009) standard. For example, in Fig. 2. OMICRON Lab OTMC 100 master clocks are shown with their WEB based management interface on a rugged portable device. This architecture provides easy installation and maintenance, simple operation, low cost, and sufficient performance in most applications.

However, this architecture has some drawbacks also. First of all, special external weather tolerant Ethernet connectors and cables must be used, as standard Ethernet connectors and cables are designed for office and home environment only. Secondly, Ethernet compliant EM protection devices only start to appear in the market. Thirdly, the whole device is located outside, and therefore, it is subject to the wide temperature fluctuations due to weather changes, which require special

construction and causes reduced holdover performance. Holdover performance is hard to be enhanced using better quality oscillators as size and power limits apply here also due to the compact, antenna integrated solution.

### C. External Integrated GPS architecture

The External Integrated GPS architecture positions the GPS antenna and the GPS receiver close to each other, typically outside of the building, or installing the GPS receiver to the antenna cable entry into the building. However, the GPS receiver's UART and PPS logic levels must be translated to RS422 signals to transmit them on the standard Category 5/6/7 cabling infrastructure of the building to the Master Clock Computer. The use of the standard Category 5/6/7 cabling infrastructure provides great flexibility of installation and RS422 signals can be transmitted over CAT5/6/7 cables for longer distances (hundreds of meters).

This approach; however, requires the use of RS422 transmitters and receivers (transceivers) on both sides, and in addition, also galvanic isolation must be provided. Therefore, an interface hardware must be built, which has two parts. The first part interfaces the GPS receiver to the RS422 signaling on the GPS receiver side (external side), while the second part interfaces the RS422 signals to the Master Clock Computer (internal side). Unfortunately, delay cannot be considered constant in this case due to the flexibility of cabling, temperature dependent delay of transceivers, and devices used for galvanic isolation, etc., so some form of continuous delay measurement and an on-line delay compensation must be devised. Of course, the on-line delay measurement and compensation increases system complexity and component count.

TABLE I. PERFORMANCE SUMMARY OF THE INVESTIGATED ARCHITECTURES

| Property | External Antenna based architecture | Antenna-integrated architecture | External Integrated architecture |
|---|---|---|---|
| Cable length | Depends on the cable and signaling 40 m (200 m) | 100 m (CAT5 Ethernet) | Several hundred meters |
| Delay | Constant | Constant | Varying, primarily temperature dependent |
| Delay compensation | Manual, static | Automatic due to IEEE 1588 | On-line measurement and compensation |
| Holdover performance | Good | Limited | Good |
| Installation | Complex | Simple | Simple |
| Application | Industrial and laboratory | Industrial | Research and development |

EM protection for RS422 is also available as various field buses also use this signaling solution with identical EM protection requirements.

Holdover performance of this solution is similar to the External Antenna based architecture as the master clock is located inside the building in a controlled environment, and size and power consumption constraints are relaxed so better internal clocks can be used.

Due to the complexity and flexibility of this architecture, the primary application area of this architecture is research and development.

### D. Performance Summary of the Architectures

Table I. summarizes the performance of the three architectures.

## III. ARCHITECTURAL EXAMPLE

The External Integrated GPS architecture provides the best approach for research and development master clock prototype as it is easy to build with limited resources and it is compatible with the rapid development cycles of research laboratory environments. The prototype's primary aim is to experiment with IEEE 1588 master clocks and full IEEE 1588 system. For example, a fully configurable and accessible, open source software based master clock built using commercial off-the-shelf (COTS) HW components allows as to experiment with complex IEEE 1588 based system in a drastically more flexible way than using commercial master clocks, for example:

- We can test new clock management and synchronization algorithms and their influence on the performance of the system,
- We can inject any type of master clock errors into the system including practically all Byzantine failures, and test the behavior of the system in these cases also,
- We can implement and test totally new fault tolerance and redundancy algorithms.

Reliability related research of IEEE 1588 is in the center of interest [4,5] today as some applications can be considered essential.

### A. Components of the prototype master clock

The block diagram of the prototype is shown in Fig. 3. The prototype uses the following components:

- Trimble Bullet GG timing multi-GNSS (GPS, GLONASS, QZSS) antenna,
- Trimble Resolution SMT GG timing multi-GNSS (GPS, GLONASS, QZSS) receiver,
- RS422 based interface electronics for the external side and the internal side developed by the author (see Fig. 4. for details),
- Standard PC as master clock computer, running Linux, gpsd and linuxptp in a configuration detailed in [3],

- INTEL i210 network interface card with hardware IEEE 1588 support and appropriate driver detailed in [3].

The functional block diagram of the interface electronics is shown in Fig. 4. The interface must translate local logic levels to RS422 levels for transmission over the available CAT5/6/7 cables available in the building. The used RS422 transceivers are AM26LS31/32 high speed devices.

In addition, galvanic isolation and EM protection (primarily TVSs, Transient Voltage Suppressors) are also needed for safety and reliability purposes as the GPS unit is outside of the building where various high energy disturbances (lightning strikes, for example) may be present. However, EM protection is not shown on the functional block diagram for the sake of simplicity. Galvanic isolation is implemented by 6N137 fast logic optocouplers. Both side uses galvanically isolated DC/DC power supplies to power the RS232 transceivers and the optocouplers. On the external side an external power supply is used, while on the internal side USB power and communication is utilized for easy setup and operation.

There are 4 twisted pair cables in a CAT5a cable and 2 out of it are needed for the UART transmit and receive line, and 1 for transmitting the PPS signal to the master clock. One pair has no functionality. However, RS422 line drivers and receivers, and devices used for galvanic isolation and EM protection have a temperature dependent delay. In addition, due to the flexibility of the CAT5 cabling, cable length also may change even during operation (with some missing PPS events, though) due to some cable reconfiguration. As the delayed PPS signal causes inaccuracy in the whole systems, it needs to be compensated. The remaining 1 pair of cable can be used to reduce this accuracy problem.

- This pair of cable can be used to return the PPS information from the internal side (far end loopback) to the external side making possible to measure round trip delay.
- Assuming that the GPS to master clock delay is equal to the master clock to GPS delay, by measuring the round trip delay we can continuously compensate for the delays caused by the GPS extender, i.e, we assume that the delays are symmetric.
- Compensation is done in the master clock as half of the measured round trip delay (external part to internal part delay) is sent through the UART transmit line in a custom message to the master clock computer, which then perturbs the local clock with the specified ammount.

This on-line delay measurement is implemented in the current prototype using a Texas Instrument Connected Launchpad development board utilizing a Tiva C Series TM4C1294 microcontroller. The microcontroller runs with 100 MHz clock, so one way delay measurement using the built in counters has 5 ns resolution as round trip delay is measured using the system clock (10 ns resolution) and the result of measurement is divided by 2 to compute the one way delay.

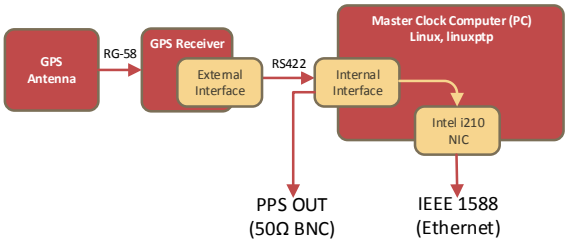


Fig. 3. Functioinal block diagramm of the prototyp master clock using the External Intergrated architecture

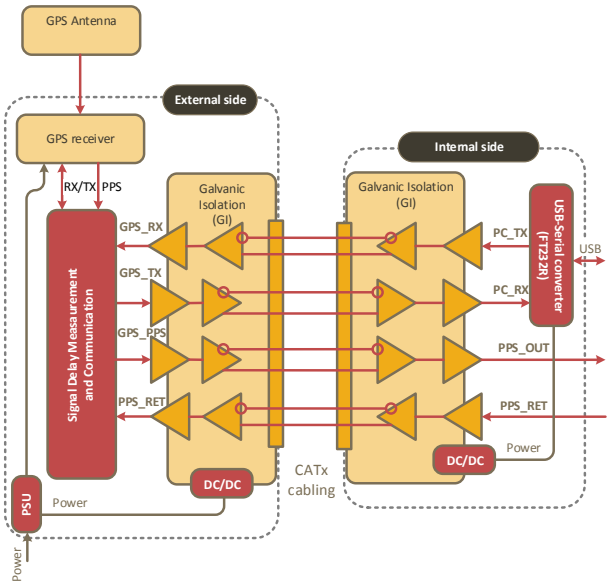


Fig. 4. Functional block diagramm of the interface eletronics developed for the prototype GPS and master clock interface.

For validation purposes the round trip delay of the interface electronics can be measured using an oscilloscope.

## *B. Mechanical construction*

The GPS receiver and the external side interface electronics are built into a standard plastic case for evaluation purposes. Currently, this device is for internal use only, so only the GPS antenna is located outside, the GPS receiver and the external interface electronics are located in an internal location near to the antenna cable entry into the building.

The internal side interface electronics is specially developed for use in a PC computer. The size and the shape of the PCB is manufactured according to the low-profile PCI Express (PCIE) card mechanical specification. However, no electronic connections are implemented on the PCIE connector, the connector is only used for mechanical fastening purposes. The card is connected to and powered from the PC through a motherboard USB connector (pin header).

## *C. Initial Evaluation Results*

Both the oscilloscope and the implemented microcontroller based one way delay measurement systems show that the current external and internal interface electronics causes 210 ns

one way delay (estimated measurement accuracy is +/- 10 ns) if they are connected a minimal length (50 cm) CAT5 cable. The jitter of the connection is minimal in this case, there was no visible "movement" of the signal on the oscilloscope during the measurements using a Rohde-Schwarz RTO1014 oscilloscope.

The interface electronics was also tested using the standard CAT5 cable plant of the building. Both the external and the internal interfaces were connected to wall outlets, then on the other side of those cable runs were connected using a patch cable forming a single approximately 50 meter long cable between the two outlets electronically. The cables in the walls were running in parallel with large number of other CAT5 cables serving various Ethernet devices with 100 Mbps and 1000 Mbps speeds, probably causing some EM interference. This test is similar to the situation in which the interface electronics are to be used. The oscilloscope based jitter evaluation has shown minimal increase in the jitter performance, based on the measurement the one way delay was 340 ns in this case, and the jitter was well-under the 5 ns, which is the resolution of the one way delay measurement solution.

Initial measurement results of the prototype master clock was shown in [3], the results published there were collected without on-line delay compensation and they were based on an early interface electronics prototype using no galvanic isolation (just RS422 transceivers). The development and measurement environment used during evaluation is published in [6].

## IV. Conclusions and Future Work

The paper lists the possible master clock architectures and compares their performance. This presented results allow designers of IEEE 1588 based systems to select the proper master clock for their application. However, here we must note that in industrial and laboratory application it us advised to use multiple master clocks from different manufacturers as the master clock is a single point of failure in current IEEE 1588 systems.

The interface electronics fulfill all the requirements set but it must be redesigned for wide scale use as the current system implements the on-line delay measurement system applying a development board with custom cabling. We consider it to be released in its current form as open hardware for interested research groups, i.e., files required for PCB manufacturing and Bill of Materials are planned to be published. The developed master clock prototype is ready to be used in various research tasks.

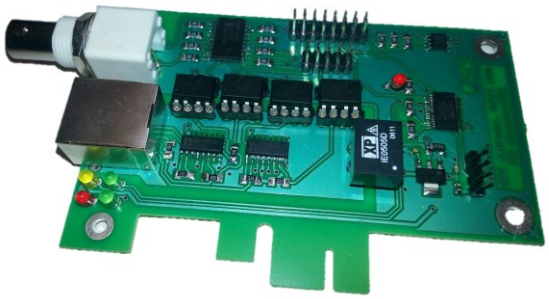

Fig. 5. The prototype hardware (PCB populated with components) of the internal side interface in the form of a low profiel PCI Express card.


## Acknowledgment

Intel Hungary Ltd. Representation Office, OMICRON Lab, and Texas Instrument Inc. have donated equipment for the research this paper is based on.


## References


[1] D. L. Mills, Computer Network Time Synchronization: the Network Time Protocol on Earth and in Space, Second Edition, New York: CRC Press, 2011.

[2] P1588 Working Group, IEEE 1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, Piscataway, NJ, USA: IEEE Standards Association, 2008.

[3] B. Ferencz and T. Kovacshazy, “Hardware assisted COTS IEEE 1588 solution for x86 Linux and its performance evaluation,” in the Proceedings of 2013 International IEEE Symposium on Precision Clock Synchronization for Measurement Control and Communication (ISPCS), 2013, pp. 47–52.

[4] Estrela, Pedro V., and Lodewijk Bonebakker. "Challenges deploying PTPv2 in a global financial company." in the Proceedings of 2013 International IEEE Symposium on Precision Clock Synchronization for Measurement Control and Communication (ISPCS), 2013., pp. 1-6.

[5] Estrela, Pedro V., et al. "Using a multi-source NTP watchdog to increase the robustness of PTPv2 in Financial Industry networks." ." in the Proceedings of 2014 International IEEE Symposium on Precision Clock Synchronization for Measurement Control and Communication (ISPCS), 2014, pp. 87-92.

[6] T. Kovacshazy and B. Ferencz, “Test environment for the evaluation of IEEE 1588 solutions including high precission pps output performance measurements,” in the Proceedings of 14th International Carpathian Control Conference (ICCC), 2013, pp. 175–180.