The component PROGRAMMABLE_SAMPLER is a simple digital component, implemented as a Moore machine, whose top-level view is in Fig. 1. It gets in input:

- a clock signal CLK, characterized by a frequency of 1 MHz
- an asynchronous master reset signal RST
- A stream of bits via a serial 1-bit transmission line DIN, on which bits are transmitted synchronously with respect to the clock signal CLK, one bit per clock cycle. Let's identify by in(t) the value present on DIN at a given clock cycle t
- A positive number N, provided via an 8-bit parallel input bus CNTRL[7:0]

The component provides in output, on its 1-bit output SMPL, the value in(t−N), i.e., the value got by the input signal DIN at the clock cycle t−N, N being the value available at instant t on the 8-bit parallel input bus CNTRL.
In addition, the PROGRAMMABLE_SAMPLER is automatically reset every minute.

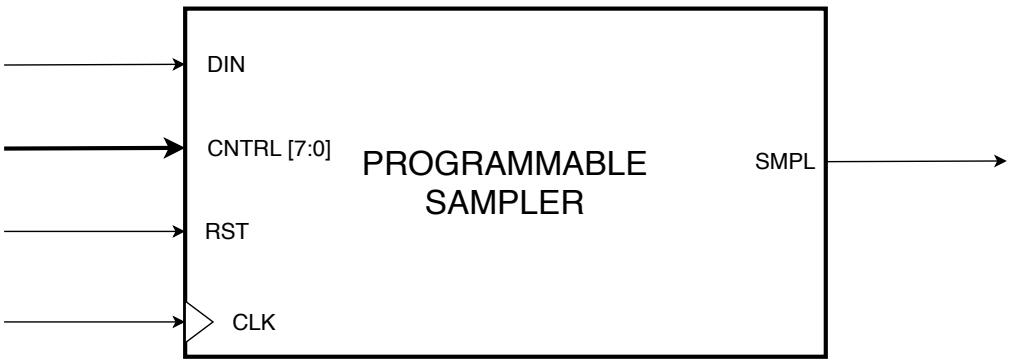

Figure 1 - PROGRAMMABLE SAMPLER top-level view