MCU−LINK Power and USB

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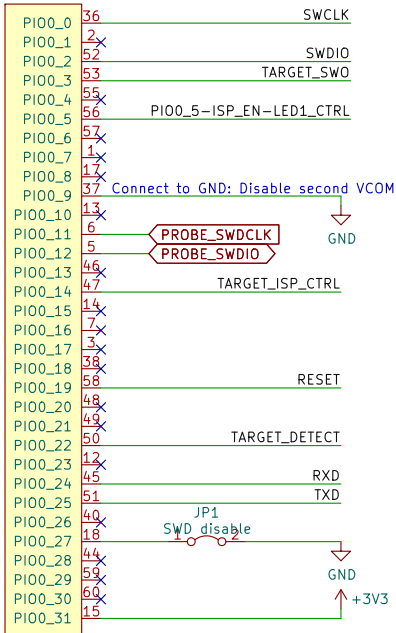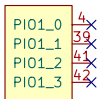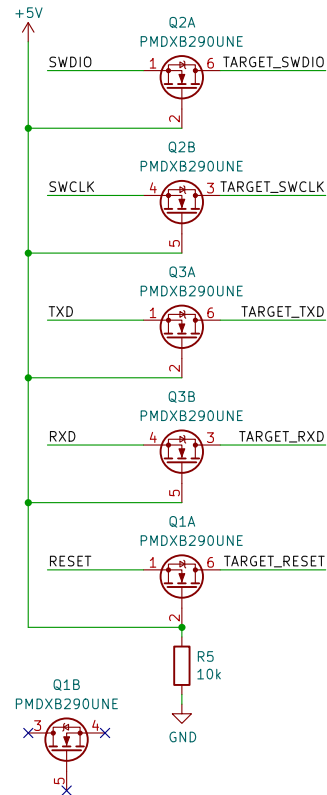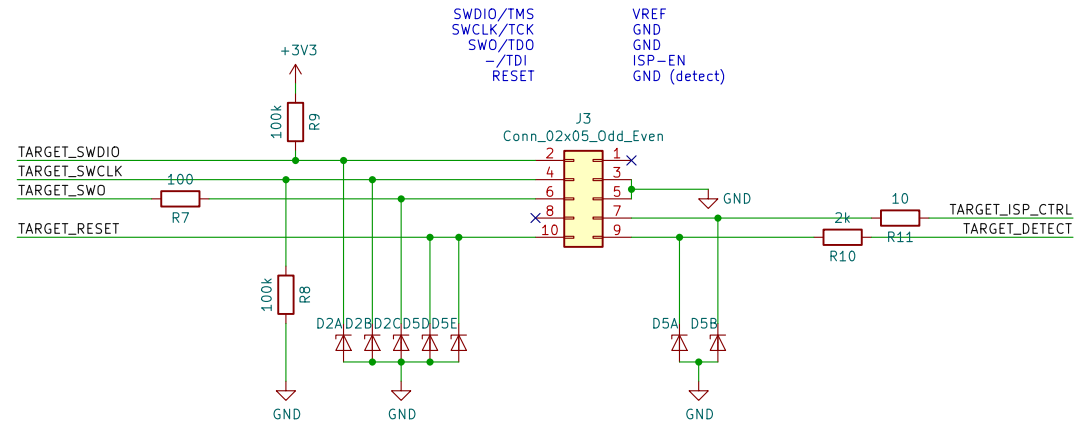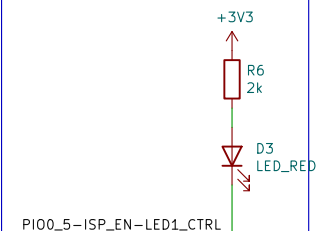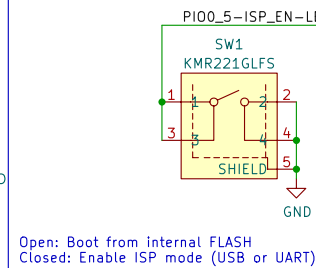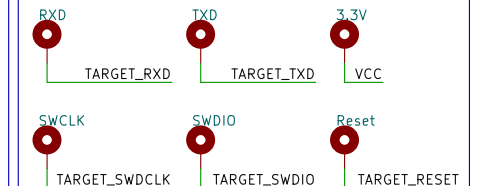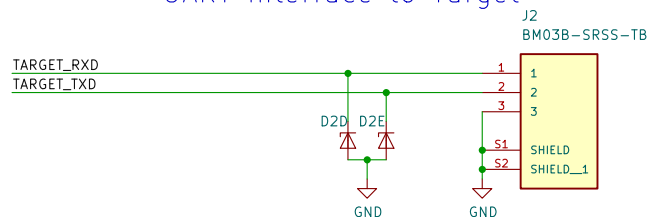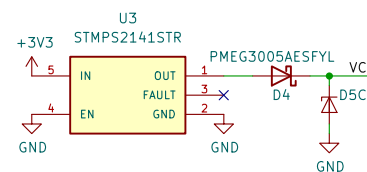
Debug and UART Interface

File: mculink_standalone_debug_uart.kicad_sch

L1
Logo HSLU

H1
MountingHole_Pad

H2
MountingHole_Pad

H3
MountingHole_Pad

H4
MountingHole_Pad

GND

GND

GND

GND

Todo for final v2.2 version:
− move ESD protection diodes closer to the pins
− check/swap UART header pins to match RPi debug probe cable
− Fix DRC errors and warnings

Sheet: /
File: MCU−Link−Standalone.kicad_sch

Title: mini MCU−LINK Standalone

Size: A4 | Date: 2023−12−12 | Rev: v2.2
KiCad E.D.A. 9.0.0 | Id: 1/3

LPC55S69 MCU Powering and USB

LPC55S69 MCU Powering and USB schematic diagram (Sheet 2 of 3)

Key components:
- **L2** MI0603J601R-10
- **C3** 4u7, **C4** 100n, **C5** 100n, **C7** 100n, **C9** 100n, **C11** 100n, **C12** 10n, **C13** 10n, **C14** 10n, **C16** 10n
- **MCU_VDDIO**
- **U2A** LPC55S69JBD64 — VDD (8, 16, 54, 43), VDDA (9), VREFP (10), VBAT_DCDC (32), VBAT_PMU (33), RESETN (21), XTAL32M_P (20), XTAL32M_N (19), XTAL32K_P (34), XTAL32K_N (35), VDD_PMU (28), FB (29), LX (31), VSSA (11), VSS_DCDC (30), EP (65)
- **Y1** 16.000MHz, **C21** 8p, **C24** 8p
- **C17** 100n, **C19** 47p
- **U1** XC6227C331PR-G — VIN (4), CE (1), VOUT (5), VSS (2), NC (3)
- **+5V**, **5V**, **C1** 10u, **C2** 100n
- **+3V3**, **3V3**, **C8** 100n, **C10** 10u
- **L4** MI0603J601R-10
- **C15** 22u, **C18** 100n, **C20** 47p
- **L5** 4u7, **C22** 22u, **C23** 47p, **C25** 100n, **C26** 22u
- **R3** 10k, **R4** 20k
- **J1** USB4110-GF-A_REVB — VBUS (A4/B9, B4/A9), D+ (A6, B6), D- (A7, B7), SBUS1 (A8), SBUS2 (B8), CC1 (A5), CC2 (B5), SHIELD (S1), GND (A1/B12, B1/A12)
- **PROBE_SWDCLK**, **PROBE_SWDIO**
- **R1** 5k1, **R2** 5k1
- **L3** MI0603J601R-10
- **USB_VBUS**, **USB_D+**, **USB_D-**
- **D1** PRTR5V0U2X — I/O1 (2), I/O2 (3), VCC (4), GND (1)
- **C6** 10n
- **U2B** LPC55S69JBD64 — USB0_3V3 (61), USB0_DM (63), USB0_DP (62), USB0_VSS (64), USB1_3V3 (27), USB1_VBUS (25), USB1_DM (24), USB1_DP (23), USB1_VSS (22), USB1_VSS (26)

Signal isolation when switched off

U2C
LPC55S69JBD64

PIO0_0	36 SWCLK
PIO0_1	2 SWDIO
PIO0_2	52
PIO0_3	53 TARGET_SWO
PIO0_4	55
PIO0_5	56 PIO0_5-ISP_EN-LED1_CTRL
PIO0_6	57
PIO0_7	1
PIO0_8	17
PIO0_9	37
PIO0_10	13
PIO0_11	6 PROBE_SWDCLK
PIO0_12	5 PROBE_SWDIO
PIO0_13	46
PIO0_14	47 TARGET_ISP_CTRL
PIO0_15	14
PIO0_16	7
PIO0_17	3
PIO0_18	38
PIO0_19	58 RESET
PIO0_20	48
PIO0_21	49
PIO0_22	50 TARGET_DETECT
PIO0_23	12
PIO0_24	45 RXD
PIO0_25	51 TXD
PIO0_26	40
PIO0_27	18
PIO0_28	44
PIO0_29	59
PIO0_30	60
PIO0_31	15

Connect to GND: Disable second VCOM → GND

JP1 SWD disable → GND

→ +3V3

U2D
LPC55S69JBD64

PIO1_0	4
PIO1_1	39
PIO1_2	41
PIO1_3	42

Signal isolation when switched off

+5V

Q2A PMDXB290UNE
SWDIO 1 — 6 TARGET_SWDIO

Q2B PMDXB290UNE
SWCLK 4 — 3 TARGET_SWCLK

Q3A PMDXB290UNE
TXD 1 — 6 TARGET_TXD

Q3B PMDXB290UNE
RXD 4 — 3 TARGET_RXD

Q1A PMDXB290UNE
RESET 1 — 6 TARGET_RESET

R5 10k → GND

Q1B PMDXB290UNE

Cortex Debug (SWD/JTAG) interface

+3V3

R9 100k

SWDIO/TMS   VREF
SWCLK/TCK   GND
SWO/TDO   GND
−/TDI   ISP−EN
RESET   GND (detect)

J3 Conn_02x05_Odd_Even

TARGET_SWDIO
TARGET_SWCLK — 100 R7
TARGET_SWO
TARGET_RESET

R8 100k

D2A D2B D2C D5D D5E

D5A D5B

R10 2k   R11 10

TARGET_ISP_CTRL
TARGET_DETECT

GND

LED: SWD activity

+3V3
R6 2k
D3 LED_RED

PIO0_5-ISP_EN-LED1_CTRL

Enable ISP mode

PIO0_5-ISP_EN-LED1_CTRL

SW1 KMR221GLFS

SHIELD

→ GND

Open: Boot from internal FLASH
Closed: Enable ISP mode (USB or UART)

castellated pins

RXD	TXD	3.3V
TARGET_RXD	TARGET_TXD	VCC
SWCLK	SWDIO	Reset
TARGET_SWDCLK	TARGET_SWDIO	TARGET_RESET

UART Interface to Target

TARGET_RXD
TARGET_TXD

J2 BM03B-SRSS-TB

D2D D2E

1
2
3
S1 SHIELD
S2 SHIELD_1

GND   GND

eFuse and Reverse Current Protection

+3V3

U3 STMPS2141STR

IN	OUT
	FAULT
EN	GND

PMEG3005AESFYL
D4
VCC
D5C

GND   GND   GND