# BK4819 Registers

REG-BK4819-E02 V1.1

2022/5/5

# Contents

# 1. About This Manual

The BK4819 is a high performance walkie-talkie transceiver. The BK4819 Registers reference manual targets application developers. It provides detailed information of the BK4819 registers.

For pin descriptions, electrical characteristics, package, and ordering information, refer to the corresponding datasheet.

BK4819                          BK4819                                              BK4819

# 2. Registers

**Table 2-1 Registers**

| Register | Default | Description |
|---|---|---|
| REG_00<15> | 0 | Soft reset:<br>1: Reset<br>0: Normal |
| REG_02<15> | Read Only | FSK TX |
| REG_02<14> | Read Only | FSK FIFO |
| REG_02<13> | Read Only | FSK RX |
| REG_02<12> | Read Only | FSK FIFO |
| REG_02<11> | Read Only | DTMF/5 TONE |
| REG_02<10> | Read Only | CTCSS/CDCSS Tail Found |
| REG_02<9> | Read Only | CDCSS |
| REG_02<8> | Read Only | CDCSS |
| REG_02<7> | Read Only | CTCSS Found interrupt |
| REG_02<6> | Read Only | CTCSS Lost interrupt |
| REG_02<5> | Read Only | VOX Found interrupt |
| REG_02<4> | Read Only | VOX Lost interrupt |
| REG_02<3> | Read Only | Squelch Found interrupt |
| REG_02<2> | Read Only | Squelch Lost interrupt |
| REG_02<1> | Read Only | FSK RX Sync interrupt |
| REG_07<15:0> | - | <15:13>: 0: CTC1<br><12:0>: CTC1 frequency control word:<br>= freq (Hz)*20.64888 for XTAL 13M/26M or<br>= freq (Hz)*20.97152 for XTAL 12.8M/19.2M/25.6M/38.4M<br><br><15:13>: 1: CTC2 (Tail 55 Hz RX detection)<br><12:0>: CTC2 (should below 100 Hz) frequency control word:<br>= 25391/freq (Hz) for XTAL 13M/26M or<br>= 25000/freq (Hz) for XTAL 12.8M/19.2M/25.6M/38.4M |

| Register | Default | Description |
|---|---|---|
| | | <15:13>: 2: CDCSS 134.4 Hz |
| | | <12:0>: CDCSS baud rate frequency(134.4 Hz) control word: |
| | | = freq (Hz)*20.64888 for XTAL 13M/26M or |
| | | = freq (Hz)*20.97152 for XTAL 12.8M/19.2M/25.6M/38.4M |
| REG_08<15:0> | - | <15>: 1: CDCSS high 12 bits; 0: CDCSS low 12 bits<br><11:0>: CDCSS high/low 12 bit code |
| REG_09<15:0> | - | DTMF/SelCall symbol coefficient for detection:<br><15:12>: Symbol number<br><7:0>: Coefficient |
| REG_0A<6> | Read Only | GPIO6 input indicator:<br>1: High<br>0: Low |
| REG_0A<5> | Read Only | GPIO5 input indicator:<br>1: High<br>0: Low |
| REG_0A<4> | Read Only | GPIO4 input indicator:<br>1: High<br>0: Low |
| REG_0A<3> | Read Only | GPIO3 input indicator:<br>1: High<br>0: Low |
| REG_0A<2> | Read Only | GPIO2 input indicator:<br>1: High<br>0: Low |
| REG_0A<1> | Read Only | GPIO1 Input Indicator:<br>1: High<br>0: Low |
| REG_0A<0> | Read Only | GPIO0 input indicator:<br>1: High<br>0: Low |
| REG_0B<11:8> | Read Only | DTMF/5 Tone code received |
| REG_0B<7> | Read Only | FSK RX Sync Negative has been found. |
| REG_0B<6> | Read Only | FSK RX Sync Positive has been found. |

| Register | Default | Description |
|---|---|---|
| REG_0B<4> | Read Only | FSK RX CRC indicator:<br>1: CRC pass<br>0: CRC fail |
| REG_0C<15:14> | Read Only | <14>: CDCSS positive code received<br><15>: CDCSS negative code received |
| REG_0C<13:12> | Read Only | CTCSS phase shift received:<br>00: No phase shift<br>01: CTCSS0 120 °phase shift<br>10: CTCSS0 180 °phase shift<br>11: CTCSS0 240 °phase shift |
| REG_0C<10:11> | Read Only | <11>: CTC2 (55 Hz) received<br><10>: CTC1 received |
| REG_0C<2> | Read Only | VOX indicator:<br>0: No<br>1: Yes |
| REG_0C<1> | Read Only | Squelch result output:<br>1: Link<br>0: Loss |
| REG_0C<0> | Read Only | Interrupt indicator:<br>1: Interrupt request<br>0: No request |
| REG_0D<15> | Read Only | Frequency scan indicator:<br>1: Busy<br>0: Finished |
| REG_0D<10:0> | Read Only | Frequency scan high 16 bits |
| REG_0E<15:0> | Read Only | Frequency scan low 16 bits:<br>= REG_0D<10:0><<16 + REG_0E<15:0> (unit: 10 Hz) |
| REG_10<15:0> | 0x0038 | RX AGC Gain Table[0] (Index for max. to min.: 3, 2, 1, 0, -1)<br><9:8>: LNA Gain Short<br>11: 0 dB; 10: -11 dB; 01: -16 dB; 00: -19 dB<br><7:5>: LNA Gain<br>111: 0 dB; 110: -2 dB; 101: -4 dB; 100: -6 dB;<br>011: -9 dB; 010: -14 dB; 001: -19 dB; 000: -24 dB |

| Register | Default | Description |
|---|---|---|
| | | <4:3>: MIXER Gain |
| | | 11: 0 dB; 10: -3 dB; 01: -6 dB; 00: -8 dB |
| | | <2:0>: PGA Gain |
| | | 111: 0 dB; 110: -3 dB; 101: -6 dB; 100: -9 dB; |
| | | 011: -15 dB; 010: -21 dB; 001: -27 dB; 000: -33 dB |
| REG_11<15:0> | 0x025a | RX AGC Gain Table[1] (Index for max. to min.: 3, 2, 1, 0, -1) |
| | | The description is the same as REG_10. |
| REG_12<15:0> | 0x037b | RX AGC Gain Table[2] (Index for max. to min.: 3, 2, 1, 0, -1) |
| | | The description is the same as REG_10. |
| REG_13<15:0> | 0x03de | RX AGC Gain Table[3] (Index for max. to min.: 3,2,1,0,-1) |
| | | The description is the same as REG_10. |
| REG_14<15:0> | 0x0000 | RX AGC Gain Table[-1] (Index for max. to min.: 3, 2, 1, 0, -1) |
| | | The description is the same as REG_10. |
| REG_18<15:11> | 0b01000 | - |
| REG_18<10:9> | 0b10 | - |
| REG_18<8:7> | 0b10 | - |
| REG_18<6> | 0b0 | - |
| REG_18<5:4> | 0b10 | - |
| REG_18<3> | 0b0 | - |
| REG_18<2:0> | 0b101 | - |
| REG_19<15> | 1 | Automatic MIC PGA Gain Controller (MIC AGC) disable: |
| | | 1: Disable |
| | | 0: Enable |
| REG_1A<15:12> | 0b0101 | Crystal vReg bit |
| REG_1A<11:8> | 0b1000 | Crystal iBit |
| REG_1A<7:5> | 0b010 | Range_sel |
| REG_1A<4:0> | 0b10000 | Band_sel |
| REG_1F<15:12> | 0b1000 | Rf VCO_regvco_vbit |
| REG_1F<11:8> | 0b1000 | Rf pll_cp_bit_0 |
| REG_1F<7:6> | 0b01 | Rf pll_r_bit_0 |

| Register | Default | Description |
|---|---|---|
| REG_1F<5:4> | 0b01 | Rf pll_r_bit_1 |
| REG_1F<3:0> | 0b1000 | Rf PLL CP bit_1 |
| REG_24<5> | 0 | DTMF/SelCall enable:<br>1: Enable<br>0: Disable |
| REG_24<4> | 1 | DTMF or SelCall detection mode:<br>1: DTMF<br>0: SelCall |
| REG_24<3:0> | 0xe | Max. symbol number for SelCall detection |
| REG_28<15:14> | 0b01 | Expander (AF RX) ratio:<br>00: Disable<br>01: 1:2<br>10: 1:3<br>11: 1:4 |
| REG_28<13:7> | 0x56 | Expander (AF RX) 0 dB point (dB) |
| REG_28<6:0> | 0x38 | Expander (AF RX) noise point (dB) |
| REG_29<15:14> | 0b10 | Compress (AF TX) ratio:<br>00: Disable<br>01: 1.333:1<br>10: 2:1<br>11: 4:1 |
| REG_29<13:7> | 0x56 | Compress (AF TX) 0 dB point (dB) |
| REG_29<6:0> | 0x40 | Compress (AF TX) noise point (dB) |
| REG_2B<15> | 1 | Enable CTCSS/CDCSS DC cancellation after FM Demodulation:<br>1: Enable<br>0: Disable |
| REG_2B<14> | 1 | Enable AF DC cancellation after FM Demodulation:<br>1: Enable<br>0: Disable |
| REG_2B<10> | 0 | Disable AF RX HPF300 filter:<br>0: Enable<br>1: Disable |

| Register | Default | Description |
|---|---|---|
| REG_2B<9> | 0 | Disable AF RX LPF3K filter:<br>0: Enable<br>1: Disable |
| REG_2B<8> | 0 | Disable AF RX de-emphasis filter:<br>0: Enable<br>1: Disable |
| REG_2B<2> | 0 | Disable AF TX HPF300 filter:<br>0: Enable<br>1: Disable |
| REG_2B<1> | 0 | Disable AF TX LPF1 filter:<br>0: Enable<br>1: Disable |
| REG_2B<0> | 0 | Disable AF TX pre-emphasis filter:<br>0: Enable<br>1: Disable |
| REG_2E<9:8> | 0x10 | CTCSS/CDCSS TX Gain2 tuning (after Gain1):<br>00: 12 dB<br>01: 6 dB<br>10: 0 dB<br>11: -6 dB |
| REG_30<15> | 0 | VCO calibration enable:<br>1: Enable<br>0: Disable |
| REG_30<13:10> | 0 | RX link enable (includes LNA/MIXER/PGA/ADC):<br>1111: Enable<br>0000: Disable |
| REG_30<9> | 0 | AF DAC enable:<br>1: Enable<br>0: Disable |
| REG_30<7:4> | 0 | PLL/VCO enable:<br>1111: Enable<br>0000: Disable |
| REG_30<3> | 0 | PA Gain enable: |

| Register | Default | Description |
|---|---|---|
| | | 1: Enable<br>0: Disable |
| REG_30<2> | 0 | MIC ADC enable:<br>1: Enable<br>0: Disable |
| REG_30<1> | 0 | TX DSP enable:<br>1: Enable<br>0: Disable |
| REG_30<0> | 0 | RX DSP enable:<br>1: Enable<br>0: Disable |
| REG_31<3> | 0 | Enable Compander function:<br>1: Enable<br>0: Disable |
| REG_31<2> | 0 | Enable VOX detection:<br>1: Enable<br>0: Disable |
| REG_31<1> | 0 | Enable Scramble function:<br>1: Enable<br>0: Disable |
| REG_32<15:14> | 0b00 | Frequency scan time:<br>00: 0.2 s<br>01: 0.4 s<br>10: 0.8 s<br>11: 1.6 s |
| REG_32<0> | 0 | Frequency scan enable:<br>1: Enable<br>0: Disable |
| REG_33<14> | 1 | GPIO6 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<13> | 1 | GPIO5 output disable:<br>1: Output disable |

| Register | Default | Description |
|---|---|---|
| | | 0: Output enable |
| REG_33<12> | 1 | GPIO4 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<11> | 1 | GPIO3 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<10> | 1 | GPIO2 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<9> | 1 | GPIO1 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<8> | 1 | GPIO0 output disable:<br>1: Output disable<br>0: Output enable |
| REG_33<6> | 0 | GPIO6 output value:<br>1: High when output is enabled<br>0: Low when output is enabled |
| REG_33<5> | 0 | GPIO5 output value:<br>1: High when output is enabled<br>0: Low when output is enabled |
| REG_33<4> | 0 | GPIO4 output value:<br>1: High when output is enabled<br>0: Low when output is enabled |
| REG_33<3> | 0 | GPIO3 output value:<br>1: High when output is enabled<br>0: Low when output is enabled |
| REG_33<2> | 0 | GPIO2 output value:<br>1: High when output is enabled<br>0: Low when output is enabled |
| REG_33<1> | 0 | GPIO1 output value:<br>1: High when output is enabled |

| Register | Default | Description |
|---|---|---|
| | | 0: Low when output is enabled |
| REG_33<0> | 0 | GPIO0 output value: |
| | | 1: High when output is enabled |
| | | 0: Low when output is enabled |
| REG_34<15:12> | 0x0 | GPIO3 output type selection: |
| | | 0: High/Low |
| | | 1: Interrupt |
| | | 2: Squelch 3 = VOX |
| | | 4: CTCSS/CDCSS comparison results |
| | | 5: CTCSS comparison results |
| | | 6: CDCSS comparison results |
| | | 7: Tail detection results |
| | | 8: DTMF/5 Tone symbol received flag |
| | | 9: CTCSS/CDCSS digital wave |
| | | Others: Reserved |
| REG_34<11:8> | 0x0 | GPIO2 output type selection. |
| | | The description is the same as REG_34<15:12>. |
| REG_34<7:4> | 0x0 | GPIO1 output type selection. |
| | | The description is the same as REG_34<15:12>. |
| REG_34<3:0> | 0x0 | GPIO0 output type selection |
| | | The description is the same as REG_34<15:12>. |
| REG_35<11:8> | 0x0 | GPIO6 output type selection. |
| | | The description is the same as REG_34<15:12>. |
| REG_35<7:4> | 0x0 | GPIO5 output type selection. |
| | | The description is the same as REG_34<15:12>. |
| REG_35<3:0> | 0x0 | GPIO4 output type selection. |
| | | The description is the same as REG_34<15:12>. |
| REG_36<15:8> | 0 | PA bias output 0 ~ 3.2 V: |
| | | 0x00: 0 V |
| | | … |
| | | 0xFF: 3.2 V |
| REG_36<7> | 0 | 1: Enable PA CTL output |
| | | 0: Disable (0 V output) |

| Register | Default | Description |
|---|---|---|
| REG_36<5:3> | 0b111 | PA Gain1 tuning:<br>111: Max.<br>…<br>000: Min. |
| REG_36<2:0> | 0b111 | PA Gain2 tuning:<br>111: Max.<br>…<br>000: Min. |
| REG_37<14:12> | 0b001 | DSP voltage setting |
| REG_37<11> | 1 | ANA LDO selection:<br>1: 2.7 V<br>0: 2.4 V |
| REG_37<10> | 1 | VCO LDO selection:<br>1: 2.7 V<br>0: 2.4 V |
| REG_37<9> | 1 | RF LDO selection:<br>1: 2.7 V<br>0: 2.4 V |
| REG_37<8> | 1 | PLL LDO selection:<br>1: 2.7 V<br>0: 2.4 V |
| REG_37<7> | 0 | ANA LDO Bypass:<br>1: Bypass<br>0: Enable |
| REG_37<6> | 0 | VCO LDO Bypass:<br>1: Bypass<br>0: Enable |
| REG_37<5> | 0 | RF LDO Bypass:<br>1: Bypass<br>0: Enable |
| REG_37<4> | 0 | PLL LDO Bypass:<br>1: Bypass<br>0: Enable |

| Register | Default | Description |
|---|---|---|
| REG_37<3> | 0 | Reserved |
| REG_37<2> | 0 | DSP enable: <br> 1: Enable <br> 0: Disable |
| REG_37<1> | 0 | XTAL enable: <br> 1: Enable <br> 0: Disable |
| REG_37<0> | 0 | Band Gap enable: <br> 1: Enable <br> 0: Disable |
| REG_38<15:0> | 0x3A98 | Frequency (Hz) = (freq_hi16<<16 + freq_lo16)*10 |
| REG_39<15:0> | 0x0271 | |
| REG_3B<15:0> | 0x5880 | Crystal frequency low 16 bits. 5 Hz/LSB |
| REG_3C<15:8> | 0x4f | Crystal frequency high 8 bits |
| REG_3C<7:6> | 0b10 | Crystal frequency mode selection: <br> 00: 13 MHz <br> 01: 19.2 MHz <br> 10: 26 MHz <br> 11: 38.4 MHz |
| REG_3D<15:0> | 0x2aab | IF selection: <br> 0: Zero IF <br> 0x2aab: 8.46 kHz IF <br> 0x4924: 7.25 kHz IF <br> 0x6800: 6.35 kHz IF <br> 0x871c: 5.64 kHz IF <br> 0xa666: 5.08 kHz IF <br> 0xc5d1: 4.62 kHz IF <br> 0xe555: 4.23 kHz IF <br> If REG_43<5> = 1, IF = IF*2. |
| REG_3E<15:0> | 36458 | Band selection threshold: <br> = VCO max. frequency (Hz)/96/640 |
| REG_3F<15> | 0 | FSK TX Finished interrupt enable: <br> 1: Enable |

| Register | Default | Description |
|----------|---------|-------------|
|  |  | 0: Disable |
| REG_3F<14> | 0 | FSK FIFO Almost Empty interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<13> | 0 | FSK RX Finished interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<12> | 0 | FSK FIFO Almost Full interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<11> | 0 | DTMF/5 TONE Found interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<10> | 0 | CTCSS/CDCSS Tail Found interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<9> | 0 | CDCSS Found interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<8> | 0 | CDCSS Lost interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<7> | 0 | CTCSS Found interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<6> | 0 | CTCSS Lost interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<5> | 0 | VOX Found interrupt enable: <br> 1: Enable <br> 0: Disable |
| REG_3F<4> | 0 | VOX Lost interrupt enable: <br> 1: Enable |

| Register | Default | Description |
|---|---|---|
| | | 0: Disable |
| REG_3F<3> | 0 | Squelch Found interrupt enable:<br>1: Enable<br>0: Disable |
| REG_3F<2> | 0 | Squelch Lost interrupt enable:<br>1: Enable<br>0: Disable |
| REG_3F<1> | 0 | FSK RX Sync interrupt enable:<br>1: Enable<br>0: Disable |
| REG_40<12> | 1 | Enable RF TX deviation:<br>1: Enable<br>0: Disable |
| REG_40<11:0> | 0x4D0 | RF TX deviation tuning (applicable for both in-band signals and sub-audio signals):<br>0: Min.<br>…<br>0xFFF: Max. |
| REG_43<14:12> | 0b100 | RF filter bandwidth (Apass = 0.1 dB):<br>000: 1.7 kHz<br>001: 2 kHz<br>010: 2.5 kHz<br>011: 3 kHz<br>100: 3.75 kHz<br>101: 4 kHz<br>110: 4.25 kHz<br>111: 4.5 kHz<br>If REG_43<5> = 1, RF filter BW = BW*2. |
| REG_43<11:9> | 0b000 | RF filter bandwidth when the signal is weak (Apass = 0.1 dB):<br>000: 1.7 kHz<br>001: 2 kHz<br>010: 2.5 kHz<br>011: 3 kHz<br>100: 3.75 kHz |

| Register | Default | Description |
|---|---|---|
| | | 101: 4 kHz |
| | | 110: 4.25 kHz |
| | | 111: 4.5 kHz |
| | | If REG_43<5> = 1, RF filter BW = BW*2. |
| REG_43<8:6> | 0b001 | AF TX LPF2 filter bandwidth (Apass = 1 dB) selection: |
| | | 100: 4.5 kHz |
| | | 101: 4.25 kHz |
| | | 110: 4 kHz |
| | | 111: 3.75 kHz |
| | | 000: 3 kHz (for 25k channel space) |
| | | 001: 2.5 kHz (for 12.5k channel space) |
| | | 010: 2.75 kHz |
| | | 011: 3.5 kHz |
| REG_43<5:4> | 0b00 | Bandwidth mode selection: |
| | | 00: 12.5k |
| | | 01: 6.25k |
| | | 10: 25k/20k |
| REG_43<2> | 0 | Gain after FM demodulation: |
| | | 1: 6 dB |
| | | 0: 0 dB |
| REG_44<15:0> | 0x9009 | 300 Hz AF response coefficient for TX |
| REG_45<15:0> | 0x31a9 | 300 Hz AF response coefficient for TX |
| REG_46<10:0> | 0x50 | Voice amplitude threshold for VOX on |
| REG_47<13> | 1 | AF output inverse mode: |
| | | 1: Inverse |
| REG_47<11:8> | 0x1 | AF output selection: |
| | | 0x0: Mute |
| | | 0x1: Normal AF out |
| | | 0x2: Tone out for RX (enable Tone1 first) |
| | | 0x3: Beep out for TX (enable Tone1 first and set REG_03[9] = 1 to enable AF) |
| | | 0x6: CTCSS/CDCSS out for RX test |
| | | 0x8: FSK out for RX test |
| | | Others: Reserved |

| Register | Default | Description |
|---|---|---|
| REG_47<0> | 0 | AF TX filter bypass all:<br>1: Bypass all AF TX filter<br>0: Normal |
| REG_48<11:10> | 0b00 | AF RX Gain1:<br>00: 0 dB<br>01: -6 dB<br>10: -12 dB<br>11: -18 dB |
| REG_48<9:4> | 0x3C | AF RX Gain2 (-26 dB ~ 5.5 dB, 0.5 dB/step):<br>0x00: Mute |
| REG_48<3:0> | 0b1111 | AF DAC Gain (after Gain1 and Gain2), about 2 dB/step:<br>1111: Max.<br>…<br>0000: Min. |
| REG_49<15:14> | 0b00 | High/Low Lo selection:<br>0X: Auto High/Low Lo<br>10: Low Lo<br>11: High Lo |
| REG_49<13:7> | 0x50 | RF AGC high threshold, 1 dB/LSB |
| REG_49<6:0> | 0x30 | RF AGC low threshold, 1 dB/LSB |
| REG_4B<5> | 0 | AF Level Controller (ALC) disable:<br>1: Disable<br>0: Enable |
| REG_4D<7:0> | 0x20 | Glitch threshold for Squelch = 0 |
| REG_4E<13:11> | 0b101 | Squelch = 1 Delay Setting (5 ms) |
| REG_4E<10:9> | 0b111 | Squelch = 0 Delay Setting (5 ms) |
| REG_4E<7:0> | 0x08 | Glitch threshold for Squelch = 1 |
| REG_4F<14:8> | 0x2F | Ex-noise threshold for Squelch = 0 |
| REG_4F<6:0> | 0x2E | Ex-noise threshold for Squelch = 1 |
| REG_50<15> | 0 | Enable AF TX mute (for DTMF TX or other applications):<br>1: Mute<br>0: Normal |

| Register | Default | Description |
|---|---|---|
| REG_51<15> | 0 | 1: Enable TX CTCSS/CDCSS<br>0: Disable |
| REG_51<14> | 0 | 1: GPIO0 Input for CDCSS<br>0: Normal mode |
| REG_51<13> | 0 | 1: Transmit negative CDCSS code<br>0: Transmit positive CDCSS code |
| REG_51<12> | 0 | CTCSS/CDCSS mode selection:<br>1: CTCSS<br>0: CDCSS |
| REG_51<11> | 0 | CDCSS 24 or 23 bit selection:<br>1: 24 bit<br>0: 23 bit |
| REG_51<10> | 0 | 1050 Hz detection mode:<br>1: 1050/4 detection enable (CTC1 should be set to 1050/4 Hz) |
| REG_51<9> | 0 | Auto CDCSS BW mode:<br>1: Disable<br>0: Enable |
| REG_51<8> | 0 | Auto CTCSS BW mode:<br>0: Enable<br>1: Disable |
| REG_51<6:0> | 0 | CTCSS/CDCSS TX Gain1 tuning:<br>0: Min.<br>…<br>0x7F: Max. |
| REG_52<15> | 0 | Enable 120°/180°/240° shift CTCSS or 134.4 Hz Tail when CDCSS mode is enabled:<br>0: Normal<br>1: Enable |
| REG_52<14:13> | 0b00 | CTCSS tail mode selection (only valid when REG_52<15> = 1):<br>00: 134.4 Hz CTCSS Tail when CDCSS mode is enabled<br>01: CTCSS0 120 °phase shift<br>10: CTCSS0 180 °phase shift<br>11: CTCSS0 240 °phase shift |

| Register | Default | Description |
|---|---|---|
| REG_52<12> | 0 | CTCSS detection threshold mode:<br>1: ~ 0.1%<br>0: 0.1 Hz |
| REG_52<11:6> | 0x0A | CTCSS Found detection threshold |
| REG_52<5:0> | 0x0F | CTCSS Lost detection threshold |
| REG_54<15:0> | 0x9009 | 300 Hz AF response coefficient for RX |
| REG_55<15:0> | 0x31a9 | 300 Hz AF response coefficient for RX |
| REG_58<15:13> | 000 | FSK TX mode selection:<br>000: FSK 1.2K and FSK 2.4K TX<br>001: FFSK 1.2K/1.8K TX<br>011: FFSK 1.2K/2.4K TX<br>101: NOAA SAME TX |
| REG_58<12:10> | 000 | FSK RX mode selection:<br>000: FSK1.2K, FSK2.4K RX and NOAA SAME RX<br>111: FFSK 1.2K/1.8K RX<br>100: FFSK 1.2K/2.4K RX |
| REG_58<9:8> | 00 | FSK RX Gain |
| REG_58<7:6> | 00 | 11: FSK enable<br>00: FSK disable |
| REG_58<5:4> | 00 | FSK Preamble type selection:<br>11: 0xAA<br>10: 0x55<br>00: 0xAA or 0x55 due to the MSB of FSK Sync Byte 0 |
| REG_58<3:1> | 000 | FSK RX bandwidth setting:<br>100: FSK 2.4K and FFSK 1.2K/2.4K<br>000: FSK 1.2K<br>001: FFSK 1.2K/1.8K<br>010: NOAA SAME RX |
| REG_58<0> | 0 | FSK enable:<br>1: Enable<br>0: Disable |
| REG_59<15> | 0 | Clear TX FIFO: |

| Register | Default | Description |
|---|---|---|
|  |  | 1: Clear |
| REG_59<14> | 0 | Clear RX FIFO:<br>1: Clear |
| REG_59<13> | 0 | 1: Enable FSK Scramble |
| REG_59<12> | 0 | 1: Enable FSK RX |
| REG_59<11> | 0 | 1: Enable FSK TX |
| REG_59<10> | 0 | 1: Invert FSK data when RX mode is enabled |
| REG_59<9> | 0 | 1: Invert FSK data when TX mode is enabled |
| REG_59<7:4> | 0 | FSK Preamble length selection:<br>0: 1 byte<br>1: 2 bytes<br>2: 3 bytes<br>…<br>15: 16 bytes |
| REG_59<3> | 0 | FSK Sync length selection:<br>1: 4 bytes (FSK Sync Byte 0, 1 ,2, 3)<br>0: 2 bytes (FSK Sync Byte 0, 1) |
| REG_5A<15:8> | 0x85 | FSK Sync Byte 0 (Sync Byte 0 first, then Byte 1, 2, 3) |
| REG_5A<7:0> | 0xCF | FSK Sync Byte 1 |
| REG_5B<15:8> | 0xAB | FSK Sync Byte 2 |
| REG_5B<7:0> | 0x45 | FSK Sync Byte 3 |
| REG_5C<6> | 1 | CRC option enable:<br>1: Enable<br>0: Disable |
| REG_5D<15:8> | 0x0F | FSK data length (byte) low 8 bits. For example, 0xF means 16-byte length. |
| REG_5D<7:5> | 0 | FSK data length (byte) high 3 bits |
| REG_5E<9:3> | 64 | FSK TX FIFO (total 128 words) Almost Empty threshold |
| REG_5E<2:0> | 4 | FSK RX FIFO (total 8 words) Almost Full threshold |
| REG_5F<15:0> | x | FSK word input/output |
| REG_63<7:0> | Read Only | Glitch indicator |

| Register | Default | Description |
|---|---|---|
| REG_64<15:0> | Read Only | Voice amplitude out |
| REG_65<6:0> | Read Only | Ex-noise indicator, dB/step |
| REG_67<8:0> | Read Only | RSSI (dBm) = REG_67<8:0>/2 − 160, 0.5 dB/step |
| REG_68<15> | Read Only | CTCSS scan indicator:<br>1: Busy<br>0: Found |
| REG_68<12:0> | Read Only | CTCSS frequency. Frequency (Hz):<br>= REG_68<12:0>/20.64888 for 13M/26M XTAL or<br>= REG_68<12:0>/20.97152 for 12.8M/19.2M/25.6M/38.4M XTAL |
| REG_69<15> | Read Only | CDCSS scan indicator:<br>1: Busy<br>0: Found |
| REG_69<14> | Read Only | 23 or 24 bit CDCSS indicator:<br>1: 24 bit<br>0: 23 bit |
| REG_69<11:0> | Read Only | CDCSS high 12 bits |
| REG_6A<11:0> | Read Only | CDCSS low 12 bits |
| REG_6F<6:0> | Read Only | AF TX/RX input amplitude (dB) |
| REG_70<15> | 0 | Enable TONE1:<br>1: Enable<br>0: Disable |
| REG_70<14:8> | 0 | TONE1 tuning gain |
| REG_70<7> | 0 | Enable TONE2:<br>1: Enable<br>0: Disable |
| REG_70<6:0> | 0 | TONE2/FSK tuning gain |
| REG_71<15:0> | 0x8517 | TONE1/Scramble frequency control word:<br>= freq (Hz)*10.32444 for XTAL 13M/26M or<br>= freq (Hz)*10.48576 for XTAL 12.8M/19.2M/25.6M/38.4M |
| REG_72<15:0> | 0x2854 | TONE2/FSK frequency control word:<br>= freq (Hz)*10.32444 for XTAL 13M/26M or |

| Register | Default | Description |
|---|---|---|
| | | = freq (Hz)*10.48576 for XTAL 12.8M/19.2M/25.6M/38.4M |
| REG_73<13:11> | 0b000 | Automatic Frequency Correction (AFC) range selection: <br> 000: Max. <br> … <br> 111: Min. |
| REG_73<4> | 0 | Automatic Frequency Correction (AFC) disable: <br> 1: Disable <br> 0: Enable |
| REG_74<15:0> | 0xf50b | 3000 Hz AF response coefficient for TX |
| REG_75<15:0> | 0xf50b | 3000 Hz AF response coefficient for RX |
| REG_77<15:8> | 0xA8 | Squelch mode select: <br> 0x88/0xA8: RSSI + noise + Glitch <br> 0xaa: RSSI + Glitch <br> 0xcc: RSSI + noise <br> 0xFF: RSSI |
| REG_77<7:0> | 0xef | - |
| REG_78<15:8> | 0x48 | RSSI threshold for Squelch = 1, 0.5 dB/step |
| REG_78<7:0> | 0x46 | RSSI threshold for Squelch = 0, 0.5 dB/step |
| REG_79<15:11> | 8 | VOX detection interval time |
| REG_79<10:0> | 0x40 | Voice amplitude threshold for VOX off |
| REG_7A<15:12> | 8 | VOX = 0 detection delay, ~ 128 ms |
| REG_7B<15:0> | 0xae34 | RSSI table |
| REG_7C<15:0> | 0x8000 | RSSI table |
| REG_7D<4:0> | 0x10 | MIC sensitivity tuning, 0.5 dB/step: <br> 0x00: Min. <br> … <br> 0x1F: Max. |
| REG_7E<15> | 0 | AGC fix mode: <br> 1: Fix <br> 0: Auto |
| REG_7E<14:12> | 0b011 | AGC fix index: |

| Register | Default | Description | | |
|---|---|---|---|---|
| | | 011: Max.<br>…<br>100: Min. | | |
| REG_7E<5:3> | 0b101 | DC filter bandwidth for TX (MIC in):<br>000: Bypass DC filter | TX | MIC in |
| REG_7E<2:0> | 0b110 | DC filter bandwidth for RX (IF in):<br>000: Bypass DC filter | RX | IF in |

# 3. Default Value

**Table 3-1 Default Value of Registers**

| Register | Value (HEX) | Register | Value (HEX) | Register | Value (HEX) | Register | Value (HEX) |
|----------|-------------|----------|-------------|----------|-------------|----------|-------------|
| REG_00 | 4819 | REG_20 | 0000 | REG_40 | 34D0 | REG_60 | - |
| REG_01 | - | REG_21 | 06D8 | REG_41 | 81C3 | REG_61 | - |
| REG_02 | - | REG_22 | 4D08 | REG_42 | 6B5C | REG_62 | - |
| REG_03 | - | REG_23 | 8410 | REG_43 | 4048 | REG_63 | - |
| REG_04 | - | REG_24 | 8C5E | REG_44 | 9009 | REG_64 | - |
| REG_05 | 7812 | REG_25 | C1BA | REG_45 | 31A9 | REG_65 | - |
| REG_06 | - | REG_26 | 33B0 | REG_46 | A050 | REG_66 | - |
| REG_07 | - | REG_27 | 1430 | REG_47 | 6140 | REG_67 | - |
| REG_08 | - | REG_28 | 6B38 | REG_48 | 33CF | REG_68 | - |
| REG_09 | - | REG_29 | AB40 | REG_49 | 2830 | REG_69 | - |
| REG_0A | - | REG_2A | 4711 | REG_4A | 5450 | REG_6A | - |
| REG_0B | - | REG_2B | C000 | REG_4B | 7100 | REG_6B | - |
| REG_0C | - | REG_2C | 5B05 | REG_4C | A520 | REG_6C | - |
| REG_0D | - | REG_2D | 1038 | REG_4D | A020 | REG_6D | - |
| REG_0E | - | REG_2E | 0204 | REG_4E | 6F08 | REG_6E | - |
| REG_0F | - | REG_2F | F49B | REG_4F | 2F2E | REG_6F | - |
| REG_10 | 0038 | REG_30 | 0000 | REG_50 | 3B20 | REG_70 | 0000 |
| REG_11 | 025A | REG_31 | 0000 | REG_51 | 0000 | REG_71 | 8517 |
| REG_12 | 037B | REG_32 | 0244 | REG_52 | 028F | REG_72 | 2854 |
| REG_13 | 03DE | REG_33 | FF00 | REG_53 | E66C | REG_73 | 4682 |
| REG_14 | 0000 | REG_34 | 0000 | REG_54 | 9009 | REG_74 | F50B |
| REG_15 | 8005 | REG_35 | 0000 | REG_55 | 31A9 | REG_75 | F50B |
| REG_16 | 0000 | REG_36 | 003F | REG_56 | 1021 | REG_76 | A126 |
| REG_17 | 0000 | REG_37 | 1F00 | REG_57 | 0000 | REG_77 | A8FF |

| Register | Value (HEX) | Register | Value (HEX) | Register | Value (HEX) | Register | Value (HEX) |
|----------|-------------|----------|-------------|----------|-------------|----------|-------------|
| **REG_18** | 4525 | **REG_38** | 3A98 | **REG_58** | 0000 | **REG_78** | 4846 |
| **REG_19** | 9041 | **REG_39** | 0271 | **REG_59** | 0000 | **REG_79** | 4040 |
| **REG_1A** | 5850 | **REG_3A** | 049A | **REG_5A** | 85CF | **REG_7A** | 889A |
| **REG_1B** | 2200 | **REG_3B** | 5880 | **REG_5B** | AB45 | **REG_7B** | AE34 |
| **REG_1C** | 0000 | **REG_3C** | 4F88 | **REG_5C** | 56F9 | **REG_7C** | 8000 |
| **REG_1D** | 0000 | **REG_3D** | 2AAB | **REG_5D** | 0F00 | **REG_7D** | E550 |
| **REG_1E** | 4C58 | **REG_3E** | 8E6A | **REG_5E** | 3204 | **REG_7E** | 302E |
| **REG_1F** | A656 | **REG_3F** | 0000 | **REG_5F** | - | **REG_7F** | - |

# Revision History

| Version | Date | Description |
|---------|------|-------------|
| 1.0 | 2022/1/17 | Initial release. |
| 1.1 | 2022/5/5 | • Added REG_33<8> to Table 2-1 in Section 2 Registers<br>• Corrected the values of registers REG_1E and REG_1F in Table 3-1 in Section 3 Default Value |

**Beken Corporation**

Building 41, 1387 Zhangdong Rd
Shanghai 201203
China

http://www.bekencorp.com