CO MILESTONE 2
REPORT

Team 16

Adham Hesham 52-0693 **adham.elsegeeny@student.guc.edu.eg**

Mostafa Ahmed 52-1727 **mostafa.ebied@student.guc.edu.eg**

Mohamed Ahmed 52-17435 **mohamed.sameh@student.guc.edu.eg**

Youssef Ahmed 52-2295 **youssef.darwiesh@student.guc.edu.eg**

Aly Ahmed 52-2793 **aly.rezk@student.guc.edu.eg**

Memory Instructions and contents :

ORG 0 (Start from address 0 in memory)

Address: 0000 → LDA A (200C)

Address: 0001 → ADD B (100D)

Address: 0002 → SUB C (500E)

Address: 0003 → SZA (7004)

Address: 0004 → BUN N1 (4007)

Address: 0005 → LDA B (200D)

Address: 0006 → BUN N2 (400A)

Address: 0007 → LDA A (200C)

Address: 0008 → INC (7020)

Address: 0009 → BUN N3 (400B)

Address: 0010 → AND A (000C)

Address: 0011 → STA D (300F)

Address: 0012 → DEC 2 (0002)

Address: 0013 → DEC 5

Address: 0014 → DEC 7

Address: 0015 → DEC 0

BUS Control

COMPONENT: SELECTION LINES : CONTROL SIGNALS

M[AR]   (000) $D0T4 + D1T4 + D2T4 + D5T4 + T1$

AR   (001) $D4T4$

TR   (010)   X

DR   (011)   X

AC   (100) $D7I'T3B5 + D3T4 + D5T5$

PC   (101) $T0$

IR   (110) $T2$

XXX   (111)   NOTHING

ALU Signals

FUNCTION: SELECTION LINES : CONTROL SIGNALS

ADD   (001)   D1T5

SUB   (010)   D5T6

Transfer   (011)   D5T5 + D2T5

AND   (100)   D0T5

OR   (101)   X

XOR   (110)   X

INC   (111)   D7I'T4B5

Instructions needed:

LDA :   D2T4 + D2T5

ADD: $\quad$ D1T4 + D1T5

SUB: $\quad$ D5T4 + D5T5 +D5T6

SZA: $\quad$ D7I'T3B2 $\qquad$ if (AC=0)

BUN: $\quad$ D4T4

INC: $\quad$ D7I'T3B5 + D7I'T4B5

AND: $\quad$ D0T4 + D0T5

STA: $\quad$ D3T4

Registers and counters:

SC CLR : D0T5 + D1T5 + D2T5 + D3T4 + D4T4 + D5T6 + D7I'T3B2 + D7I'T4B5

SC INC: (SC CLR)'

PC INC: $D7I'T3B2(AC)' + T1$

DR Load: $D0T4 + D1T4 + D2T4 + D5T5 + D5T4 + D7I'T3B5$

Memory Write: $D3T4 + D5T4$

Memory Read: $D0T4 + D1T4 + D2T4 + D5T4 + T1$

AR Load : $T0 + T2$

AC Load: $D7I'T4B5 + D0T5 + D1T5 + D2T5 + D5T6 + D5T5$

IR Load: $T1$

PC Load: $D4T4$