**GRP-17 Data Path design:**

Operand 2 select

Operand 1 select

Op select

source reg

Dest reg

Memory read

Memory write

Output signal

LMD

ALU OUT

Ins

[25-22], [21-18]

Ins [17-0], [21-0]

Ins [13-13]

Ins [31-26]

Mux

Mux

Shamt[Imm[0]])

Imm1

Mux

4+

zero

Cond

NPC

Mux

Mux

Memory

ALU

Mux

Imm

B

A

Sign Extend

Register Bank

Instruction Memory

PC

Designed as 4:1 MUX

* The blue lines are data lines
* The dotted lines are control signals
* Black lines are instruction bit dividers

**Description of the processor data path:**

The instruction pointed by the PC is fetched from Instruction memory and PC is immediately updated to point to the next instruction

The first six bits of the instruction is sent to the control unit that sends the needed control signals according to the opcode

The instruction fetched is decoded. Decoding is done in parallel with reading the register operands rs, rt and shift amount. Similarly immediate data and address are also decoded and sign extended to 32 bit.

Then according to the control signals, respective outputs are obtained out of MUX’s and the operands are sent into ALU along with the operation to get the output.

This output is sent into memory to fetch the corresponding data in case of this type of instructions. The output from ALU and the data from memory are connected to a MUX and the output is obtained according to the opcode

This output is then written back into SP or to the respective register.

For branch instructions, according to the condition, the PC is updated.