Comparison of all-digital LDO architectures and their implementations in ASAP7 (team: Adhiraj Datar)

Project Proposal

Digital low drop-out (D-LDO) voltage regulators can offer many advantages over their analog counterparts such as low-voltage operation, scalability, and fast transient response. In recent years, many D-DLO architectures have incorporated different techniques including dual loop control, droop detection, TDC integration/time quantization, etc. to improve upon D-LDO metrics such as transient response time, power supply ripple rejection (PSRR), and performance independence from operation clock frequency. Furthermore, many recently proposed D-LDO architectures make claims of “full synthesizability” and compatibility with automatic PnR flows, increasing their ease of implementation and integration in digital designs across processes. This project aims to achieve 2 main goals: First, to comparatively study certain novel D-LDO architectures and compare their performance metric improvements in the ASAP7 process; and second, to generate some usable D-LDO IP that can be directly integrated into other ASAP7 projects and find use in other designs. Lastly, this study will also comment on each author’s claims of “full synthesizability” and “all-digital/automatic PnR” design and qualify the extent to which each proposed D-LDO architecture was successful in meeting this claim.

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