# Comparison of Novel Digital Low-Dropout (D-LDO) Voltage Regulation Techniques in ASAP7

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***Abstract*—This report presents and compares state-of-the-art techniques used to improve the performance of all-digital low-dropout voltage regulators. In recent years, D-LDO circuit implementations have seen a rise in popularity due to key advantages over their analog counterparts such as easier integration into digital systems, better scaling with lower voltages and process nodes, and performance independence from analog gain and large passive requirements. Several teams have recently proposed innovative D-LDO architectures and enhancements to improve performance on key metrics like transient response time, power supply noise rejection, bandwidth, operating clock frequency independence, current efficiency, etc. This report summarizes key findings from many of these studies and presents a head-to-head comparison of their results. In addition, it presents a design methodology for some of the novel D-LDO architectures in the ASAP7 technology with a plan to include a comparative summary of results from the ASAP7 implementation.**

## I. Introduction

Voltage regulators are universally used in electronic systems to isolate different power domains and provide a reliable power supply to functional system cores across operating conditions. In particular, low-dropout (LDO) voltage regulators are extremely popular because of their low voltage drop-off and high efficiency. Therefore, LDOs allow scaling of power systems with decreasing supply voltages. Low-voltage VLSI integrated circuit operation is extremely desirable since it polynomially reduces both dynamic and static power consumed by VLSI electronics.

For low power applications, maximum power efficiency is achieved by scaling supply voltage below 0.5V. However, a conventional analog LDO used in most systems cannot functionally scale beyond this supply voltage level. Furthermore, analog LDOs are more difficult to scale with modern processes and require an iterative AMS implementation that can be inconvenient to incorporate in a digital circuit flow. In recent years, novel D-LDO architectures have been proposed in order to tackle this scaling problem.

The basic D-LDO architecture - first proposed in [1] - consists of a voltage comparator, a serial-in parallel-out bidirectional shift register controlled by the voltage comparison, and a DAC implemented with a bank of pass transistor power FETs. Figure 1 shows the schematic of the first proposed D-LDO architecture. The analog power FET in the analog LDO is replaced by a bank of identical switches the gates of which are digitally controlled using the D-LDO controller.

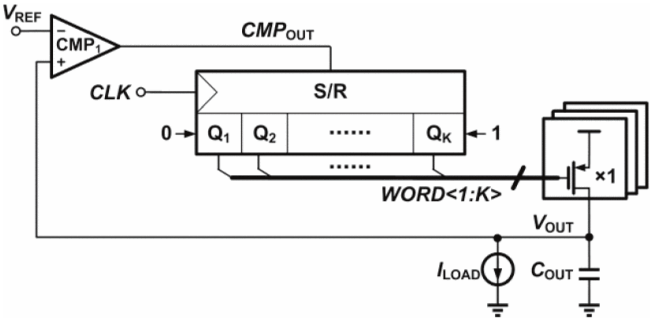


Fig. 1. Initially proposed "basic" D-LDO architecture from [1]. An N-bit digital shift register digitally controls N pass power FET switches to regulate the voltage on $V_{OUT}$

In the original publication, the D-LDO digital controller is implemented as a bidirectional serial-in parallel-out shift register that generates and registers a signal to control the gates of the power FETs. To increase the output voltage, a digital 0 is shifted into the register chain to increase the number of active switches and to reduce the output voltage, a digital 1 is shifted into the register chain to decrease the number of active power FETs. As a result, the proposed D-LDO implements an analog LDO's function using a purely digital control scheme. This meets the key advantage of being able to scale into ultra-low power application regimes as the digital switches (unlike the analog LDO) can be used in near-subthreshold biasing regimes, allowing supply voltage scaling to 0.5V and below as demonstrated in [1].

Nonetheless, this proposed D-LDO implementation suffers from some noticeable drawbacks. These include

- Low power supply noise rejection
- Lower bandwidth
- Limited sampling frequency $f_S$
- Slow reponse time due to 1 control bit update/clock cycle
- Not fully synthesizable/automatically routable design

## II. State-of-the-art D-LDO techniques

Several novel state of the art D-LDO techniques and architectures have been recently proposed to address many of these aforementioned performance drawbacks. These techniques range from dual loop switch bank control to time domain processing, overshoot/droop detection, and asynchronous event-driven D-LDOs. This section summarizes and comparatively analyzes many of these new techniques.

### A. Dual loop control

One major disadvantage of the initial proposed D-LDO design is slow response and settling time. This is in large part because the original D-LDO operates on a sampling and control clock, and the control scheme proposed in [1] is only capable of toggling one power FET switch in a sampling clock cycle. As a result, the D-LDO regulator slowly converges to the appropriate digital control signal one bit at a time across a rather slow sampling clock, which typically operates in the 100Hz-kHz range.

In recent years, many designs have proposed and implemented a dual loop control scheme to greatly increase the digital control speed of D-LDO. The dual loop control works with a coarse loop control and a fine loop control. In general, the coarse loop control activates or deactivates multiple/groups of power FETs in a single cycle whereas the fine control loop can active or deactivate single power FET switches. Figure 2 shows the D-LDO presented in [2]. This implementation reports a 500ns-750ns settling time for D-LDO voltage regulation, which is significantly reduced from the  ms settling timescale reported in [1]. Although the exact speedup attributable to solely to dual loop control schemes is unclear due to most dual loop studies also performing additional speedup techniques, the benefits from the control scheme are readily apparent and help overcome one of the original shortcomings of the D-LDO architecture presented in [1].

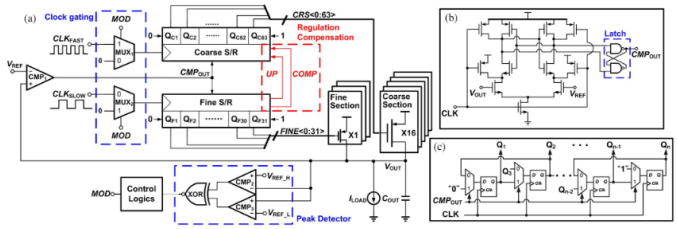


Fig. 2. The D-LDO architecture presented in [2] consists of a dual loop control scheme to improve the response time of the digital control section of the D-LDO and activate more power FETs at a time, leading to faster D-LDO operation

Similarly, Other studies including [3] and [4] also present dual loop based control schemes for D-LDO operation that are qualitatively similar to the scheme presented in [2]. The settling times presented in these studies are also in the $\mu$s range, which is once again a significant improvement over the original D-LDO design's  ms range settling time.

### B. Overshoot/supply droop detection based actuation

The all-digital control scheme of the original D-LDO presented in [1] is purely synchronous. The shift register that controls the power FET bank signals as well as the controller both operate on the same sampling clock $f_S$. In order to sufficiently charge and discharge the capacitors and satisfy the current draw requirements on the output node of the voltage regulator, the sampling clock of the D-LDO operates at a relatively slow frequency, in the kHz range. When there is a ripple, an overshoot or a droop on the output voltage node, the original D-LDO takes several clock cycles to recover the voltage and as a result has a very slow response time to supply voltage overshoots and droops. Trying to increase $f_S$ can undermine the steady state operation of the D-LDO.

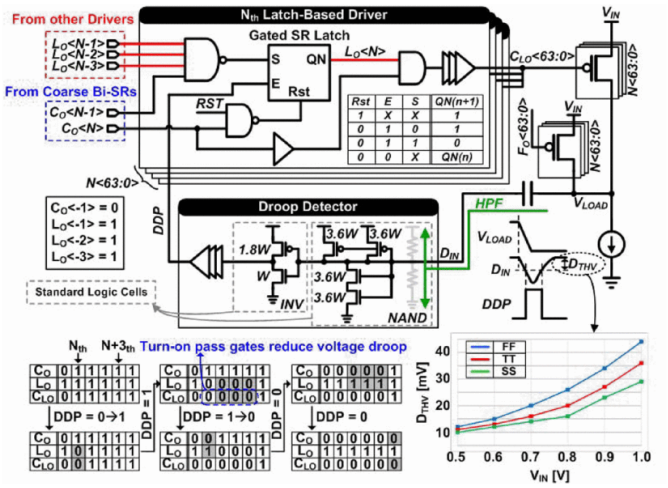


Fig. 3. The architecture presented in [8] includes a synthesizable NAND based supply voltage droop detector to asynchronously trigger a control correction cycle independently of the main D-LDO sampling clock

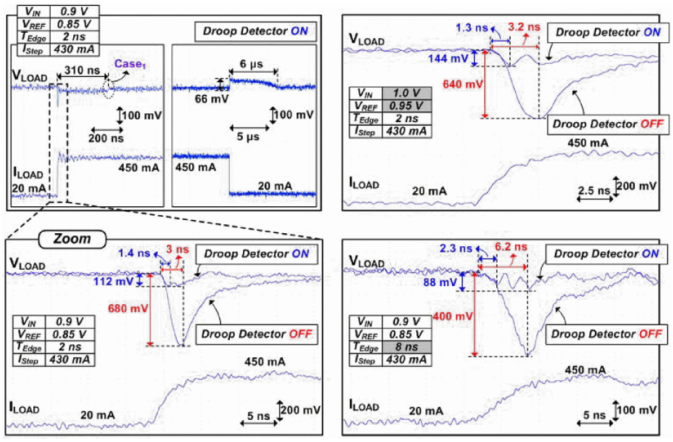


Fig. 4. The measurements for the D-LDO presented [8] show a clear improvement in LDO response time after the insertion of the VDD overshoot/droop detector

Several asynchronous processing D-LDOs have been proposed to try and target this problem. One approach that has gained popularity is an event based correction triggered by an on-chip supply voltage droop detector. The D-LDO presented in [8] is one of the many novel immplementations that integrates a droop/overshoot detector into the D-LDO in this fashion. Figure 3 shows the integration of the droop detector into the D-LDO. The droop detector is implemented using a synthesized NAND gate divider.

Figure 4 shows the waveform under the simulation of

a VDD droop. The graph presented as part of [8] shows the reduction in response time by adding a droop detector, and the study reports a response time of 1.3ns, which is significantly lower than most comparable response times reported for D-LDOs that do not employ overshoot or droop detection techniques. Similarly, [2] also presents a D-LDO with droop detection that presents a large figure of merit speed improvement and a "recovery edge time" of 20ns which is a large speedup over both analog LDOs and the basic D-LDO architecture.

### C. Time domain signal comparison

Digital LDOs can also make use of a time-based approach instead of using the traditional voltage quantizer. One such method uses a time to digital converter (TDC) in order to reduce the settling time within the D-LDO. This design uses the charging time of a capacitor to create a time signal that is then fed through a flip-flop based TDC to output a 64 bit signal into the controller as shown in Figure 5.

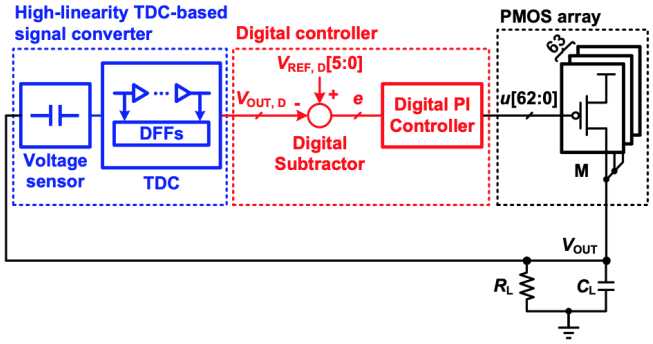


Fig. 5. TDC-based D-LDO architecture from [2]. A capacitor-based voltage sensor converts the analog signal into a time domain one. This signal is fed into a TDC with a 64-bit digital output

In an effort to combine a time domain design with reduced transient droop effects, [6] proposes a design with a beat-frequency time quantizer and a Voltage-Controlled Oscillator (VCO) pair. The beat-frequency time quantizer runs at a high sampling frequency with lower resolution when transient droop is detected and runs at a low sampling frequency with higher resolution in steady-state. This helps to provide the time quantizer with the sampling frequency it needs to handle droop caused by changes in D-LDO behavior rapidly while keeping the detailed steady-state information intact.

In this design, the VCO pair is used to convert the reference and output voltages to a current to be fed to a ring oscillator-based current-controlled oscillator. This behaves similarly to the dual loop control described in section II.A where both fine and coarse-grained control are used for both VCOs, but they are calibrated externally and not as a part of the loop for the LDO.

Much like the previous time domain design, the output of the quantizer is fed into a PI controller for the power FET switches outlined in the base design in Figure 1. Overall, time domain-based designs appear to be useful in reducing the settling time after large deviations via a TDC or a beat-frequency time quantizer.

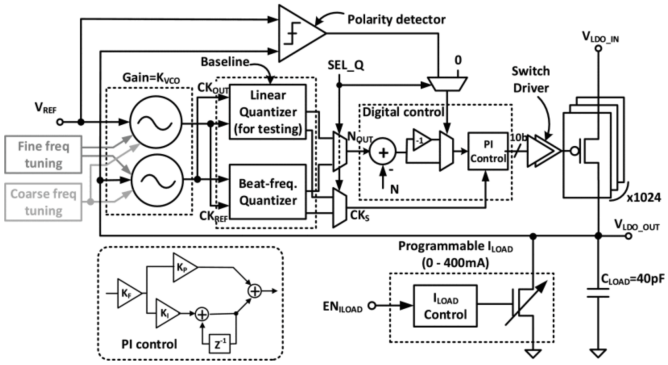


Fig. 6. Time domain design with droop detection from [6]. A VCO pair and a beat-frequency quantizer generate a digital signal for a PI controller. A linear quantizer is included for testing purposes.

### D. Fully synthesizable implementations

One of the primary proposed advantages of D-LDO designs is their ease of integration into digital IC flows and possibly automatic synthesis and PnR tools. However, the initial few D-LDO designs based on the D-LDO proposed in [1] were not compatible with most modern automatic RTL to GDSII flows and processes. In particular, for the D-LDO design proposed in [1], the comparator as well as the power FET switch bank were implemented with full-custom hand layout, and only the digital power FET control logic was capable of being synthesized and auomatically routed.

Since then, many teams have pushed the synthesizability of D-LDO designs and increased their compatibility for integration into automated semi-custom VLSI back-end PnR flows based entirely on digital standard cells. The D-LDO presented in [4] is a design presented in 2016 which achieves a high degree of synthesizability in a 130nm CMOS process by implementing the voltage comparator with a set of cross coupled 3 input NAND gates. This avoids having to implement the latch in a full custom design as was done with the original D-LDO presented in [1] which used a strong-arm latch in a comparator configuration. Furthermore, the D-LDO in [4] synthesizes the power FETs using transmission gate based logic gates which are then laid out manually. Although this implementation is far more suitable for direct integration into a digital circuit flow than the original D-LDO, it can still run into problems with process scaling into modern processes due to its reliance on transmission gate based logic gates, tri-state inverters, and NAND gate based SR style flops, which are often not available in modern process standard cell libraries.

In contrast, the D-LDOs presented in [7] and [8] at ISSCC 2020 have implemented synthesizable D-LDOs in more modern technologies. The D-LDO presented in [7] by a team from Intel is implemented in 10nm CMOS and is synthesized entirely with 10nm CMOS standard cells. The power switch

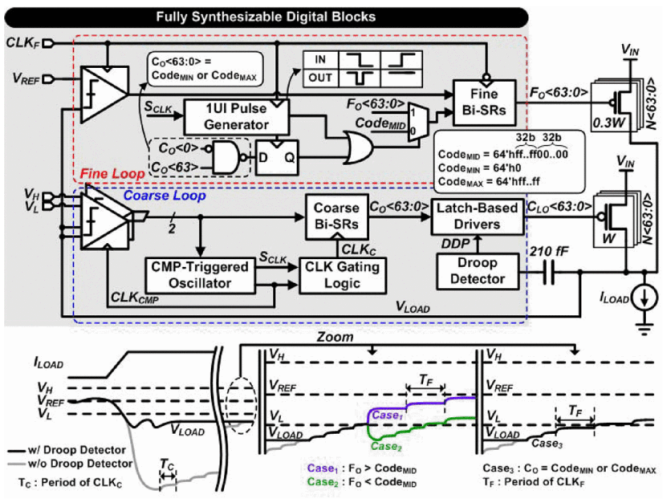


Fig. 7. The architecture of the D-LDO presented in [8] shows each of the fully synthesized blocks in the D-LDO. As with the D-LDO presented in [7], each of the digital blocks in the D-LDO is synthesized using standard cells and an automatic synthesis tool.

array is also automatically placed and routed, although the integration of the switch array appears to have been done in a bottom-up process to achieve greater control over the power FET layout. The D-LDO implementation presented in [8] is done in 28nm CMOS and also uses NAND gate based comparators as well as synthesized droop detectors and logical controls and actuators. The figure below shows the architecture of the D-LDO presented in [8]. Although these D-LDO designs may not yet be fully automated, they are certainly more compatible and convenient to integrate directly into an automatic digital VLSI flow than the first presented D-LDO designs.

## III. Presolved results

This project aims to benchmark the improvements from some of the mentioned novel D-LDO architectures in the ASAP7 technology and compare them against each other. The secondary goal of this study is to release a stable D-LDO IP implemented in ASAP7 that can be directly integrated into other ASAP7 projects.

The initial work on the implementation of this project has consisted of a barebones reproduction of the first proposed "basic" D-LDO architecture in the ASAP7 Virtuoso environment using ideal components. In the coming weeks, we intend to fully implement the basic D-LDO architecture in the ASAP7 technology and then benchmark the effects of proposed state-of-the-art D-LDO improvements like dual loop control, LCO reduction, and evaluate whether a fully synthesizable D-LDO implementation is possible and realistic to achieve in the ASAP7 technology setup.

For the comparison of D-LDO functionality and performance metrics, we expect to be able to reproduce many of the results showed in the D-LDO literature, especially operation at low voltages beyond the domain of analog LDOs and improvements in process independence and integrability into digital ASIC flows.

## IV. Conclusion

The state-of-the-art techniques described in this paper have been integrated into a few different options in the papers referenced below. The references had different measurements of success, but they all provided basic data about the design. Table 1 compares these designs against each other as well as two analog LDOs to see how well they perform when certain optimizations are applied and the effects of the various techniques.

| Reference | [10] | [11] | [1] | [3] | [4] | [5] | [6] | [7] | [8] | [9] |
|---|---|---|---|---|---|---|---|---|---|---|
| Type | Analog | Analog | Digital | Digital | Digital | Digital | Digital | Digital | Digital | Digital |
| Process | 180 nm | 55 nm | 65 nm | 65 nm | 130 nm | 65 nm | 65 nm | 10 nm | 28 nm | 65 nm |
| Active area [mm2] | 0.021 | 0.042 | 0.042 | 0.01 | | 0.017 | 0.0374 | 0.014 | 0.049 | |
| VIN [V] | 1.3–1.8 | 0.8 | 0.5 | 0.6-1.1 | 0.6 | 0.7–1.1 | 0.6-1.2 | 0.7-1.05 | 0.5-1.0 | 0.6-0.8 |
| VOUT [V] | 1.2 | 0.6 | 0.45 | 0.4-1 | 0.4 | 0.65–1.05 | 0.4-1.1 | 0.65-0.95 | 0.45-0.95 | 0.5-0.7 |
| Quiescent IQ [A] | 10 | 0.016 | 2.7 | 82 | 5.1-49.8 | 495 | 0.1-107 | 21-57 | 7.7-241 | 1.5 |
| IMAX [mA] | 25 | 10 | 0.2 | | 25 | 120 | 100 | | 480 | 0.3 |
| Peak current efficiency [%] | 99.9 | 99.8 | 98.7 | 99.92 | 99.9 | 99.6 | 99.5 | 98.6 | 99.99 | 99 |
| Line regulation [mV/V] | 0.5 | 0.5 | 3.1 | 3 | 2.5 | 15 | | | | 12-34 |
| Load regulation [mV/mA] | 0.14 | 1.05 | 0.65 | 0.06 | 2.4 | 0.6 | | | | 7-14 |
| Load capacitor CL [nF] | 4700 | 1000 | 100 | 1 | | 0.5 | | 0.534 | 0.0041 | 0.5 |
| Max voltage droop [mV] @ Load step | 2 @ 25 mA | 70 @ 10 mA | | | | 371 @ 80 mA | 108 @ 50 mA | 200 @ 1.17 A | 112 @ 430 mA | |
| Response time TR * [ns] | 376 | 7000 | 590 | 700 | | 2.1 | | | | |

TABLE I
Performance of D-LDOs referenced in this report against 2 analog LDOs

As a whole, the digital LDO's main uniform advantage over analog ones appear to be their small load capacitance. From the data provided, it would seem that digital LDOs can have a much better response time with the time domain signal comparison method, but not enough data was found outside of [5] to verify that analog LDOs could not get closer to the speed of the digital LDOs. A similar effect appears to occur for the input voltages required by the digital LDOs. The analog LDO in [11] incorporated a variety of techniques and tradeoffs such as a rail-to-rail buffer. The digital LDOs seem to regularly reach 0.5 or 0.6 The rest of the metrics either show a series of trade-offs depending on the state-of-the-art technique used or incomplete information to truly compare. However, this fits as many of the benefits provided by digital LDOs come from unlisted measures such as scalability with modern processes and easy of combination with digital flows. Importantly, the digital LDOs have similar current efficiency to analog LDOs while taking advantage of the benefits of their digital composition.

The secondary goal of the design of a D-LDO in the ASAP7 technology that is stable will help further provide a comparison for the calculated parameters found in other state-of-the-art designs. This will help provide the ability to integrate a digital LDO with other projects in ASAP7 directly in order to provide easier integration into ASAP7 ASIC flows. The ASAP7 D-LDO should compare similarly to many of the other designs as it will incorporate many of the state-of-the-art design components such as dual loop control and a fully synthesizable structure if it is feasible to do so.

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