# Benchmarking and Comparison of Digital Low-Dropout (D-LDO) Voltage Regulation Techniques in ASAP7

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***Abstract*—This report presents and compares state-of-the-art techniques used to implement all-digital low-dropout voltage regulators. In recent years, D-LDO implementations have seen a rise in popularity due to key advantages over their analog counterparts such as easier integration into digital systems, better scaling with lower voltages and process nodes, and performance independence from analog gain and large passive requirements. Several teams have recently proposed innovative D-LDO architectures and enhancements to improve performance on key metrics like transient response time, power supply noise rejection, bandwidth, operating clock frequency independence, current efficiency, etc. This report presents a bi-directional shift register D-LDO and a dual loop feedback enhanced D-LDO implemented in the ASAP7 technology. A head-to-head comparison of these ASAP7 D-LDO implementations with each other as well the D-LDOs presented in recent literature highlights many key characteristics such as very low dropoff voltage (¡ 100mV), high current efficiency (¿ 99%) and transient reponse time on the order of magnitude of $\mu$s. This report also examines the trade offs between transient response, current efficiency and operating clock frequency commonly encountered in D-LDO designs and comments on why "full synthesizability" of D-LDO designs, while desired and claimed by many teams, can be hard to achieve in practice for many processes.**

## I. Introduction

Voltage regulators are universally used in electronic systems to isolate different power domains and provide a reliable power supply to functional system cores across operating conditions. In particular, low-dropout (LDO) voltage regulators are extremely popular because of their low voltage drop-off and high efficiency.

For low power applications, maximum power efficiency is achieved by scaling supply voltage below 0.5V to maximize quadratic and exponential power savings from supply scaling. However, a conventional analog LDO used in most systems cannot functionally scale beyond this supply voltage level. Furthermore, analog LDOs are more difficult to scale with modern processes and require an iterative analog/mixed-signal implementation that can be inconvenient to incorporate in a digital circuit flow. In recent years, novel D-LDO architectures have been proposed in order to tackle this scaling problem.

The basic D-LDO architecture - first proposed in [1] - consists of a voltage comparator, a serial-in parallel-out bidirectional shift register controlled by the voltage comparison, and a DAC implemented with a bank of pass transistor power FETs. Figure 1 shows the schematic of the first proposed D-LDO architecture from [1]. The analog power FET in the analog LDO is replaced by a bank of identical switches the gates of which are digitally controlled using the D-LDO controller.

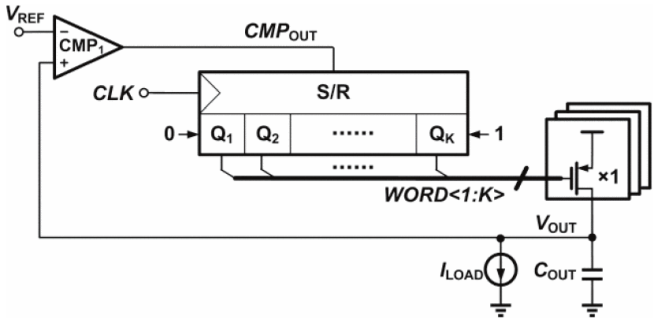


Fig. 1. Initially proposed "basic" D-LDO architecture from [1]. An N-bit digital shift register digitally controls N pass power FET switches to regulate the voltage on $V_{OUT}$

This D-LDO design achieves all-digital control of the DAC regulated voltage. Nonetheless, this proposed D-LDO implementation suffers from some noticeable drawbacks. These include:

- Low power supply noise rejection
- Lower bandwidth
- Limited sampling frequency $f_S$
- Slow reponse time due to 1 control bit update/clock cycle
- Not fully synthesizable/automatically routable design

## II. State-of-the-art D-LDO techniques

Several novel state of the art D-LDO techniques and architectures have been recently proposed to address many of these aforementioned performance drawbacks. These techniques range from dual loop switch bank control to time domain processing, overshoot/droop detection, and asynchronous event-driven D-LDOs. This section summarizes and comparatively analyzes some of these new techniques.

### *A. Dual loop control*

One major disadvantage of the initial proposed D-LDO design is slow response and settling time. This is in large part because the original D-LDO operates on a sampling and control clock, and the control scheme proposed in [1] is only capable of toggling one power FET switch in a sampling clock cycle. As a result, the D-LDO regulator slowly converges to

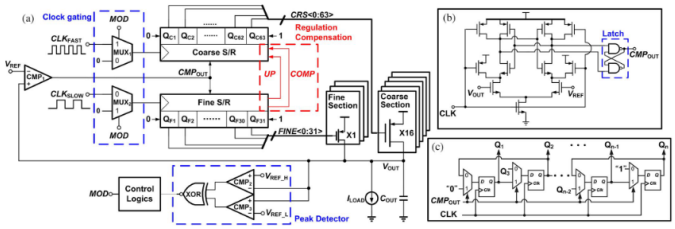


Fig. 2. The D-LDO architecture presented in [2] consists of a dual loop control scheme to improve the response time of the digital control section of the D-LDO and activate more power FETs at a time, leading to faster D-LDO operation

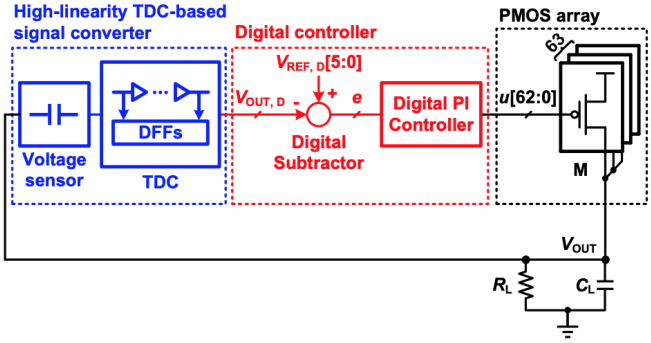


Fig. 3. TDC-based D-LDO architecture from [2]. A capacitor-based voltage sensor converts the analog signal into a time domain one. This signal is fed into a TDC with a 64-bit digital output

the appropriate digital control signal one bit at a time across a rather slow sampling clock, which typically operates in the 100Hz-kHz range.

In recent years, many designs have proposed and implemented a dual loop control scheme to greatly increase the digital control speed of D-LDO. The dual loop control works with a coarse loop control and a fine loop control. In general, the coarse loop control activates or deactivates multiple/groups of power FETs in a single cycle whereas the fine control loop can active or deactivate single power FET switches. Figure 2 shows the D-LDO presented in [2]. This implementation reports a 500ns-750ns settling time for D-LDO voltage regulation, which is significantly reduced from the  ms settling timescale reported in [1]. Although the exact speedup attributable to solely to dual loop control schemes is unclear due to most dual loop studies also performing additional speedup techniques, the benefits from the control scheme are readily apparent and help overcome one of the original shortcomings of the D-LDO architecture presented in [1].

Similarly, Other studies including [3] and [4] also present dual loop based control schemes for D-LDO operation that are qualitatively similar to the scheme presented in [2]. The settling times presented in these studies are also in the $\mu$s range, which is once again a significant improvement over the original D-LDO design's  ms range settling time.

### *B. Time domain signal comparison*

Digital LDOs can also make use of a time-based approach instead of using the traditional voltage quantizer. One such method uses a time to digital converter (TDC) in order to reduce the settling time within the D-LDO. This design uses the charging time of a capacitor to create a time signal that is then fed through a flip-flop based TDC to output a 64 bit signal into the controller as shown in Figure 5.

In an effort to combine a time domain design with reduced transient droop effects, [6] proposes a design with a beat-frequency time quantizer and a Voltage-Controlled Oscillator (VCO) pair. The beat-frequency time quantizer runs at a high sampling frequency with lower resolution when transient droop is detected and runs at a low sampling frequency with higher resolution in steady-state. This helps to provide the time quantizer with the sampling frequency it needs to handle droop caused by changes in D-LDO behavior rapidly while keeping the detailed steady-state information intact.

In this design, the VCO pair is used to convert the reference and output voltages to a current to be fed to a ring oscillator-based current-controlled oscillator. This behaves similarly to the dual loop control described in section II.A where both fine and coarse-grained control are used for both VCOs, but they are calibrated externally and not as a part of the loop for the LDO.

Much like the previous time domain design, the output of the quantizer is fed into a PI controller for the power FET switches outlined in the base design in Figure 1. Overall, time domain-based designs appear to be useful in reducing the settling time after large deviations via a TDC or a beat-frequency time quantizer.

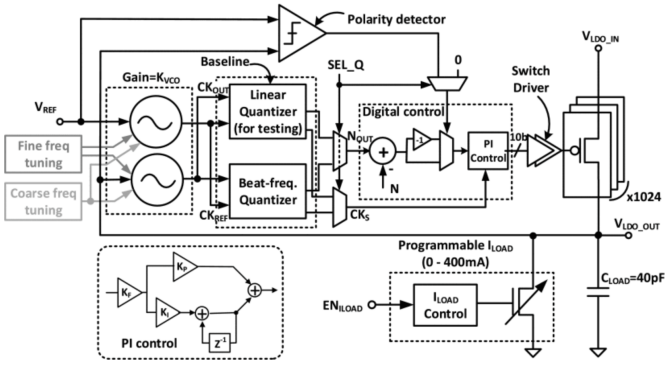


Fig. 4. Time domain design with droop detection from [6]. A VCO pair and a beat-frequency quantizer generate a digital signal for a PI controller. A linear quantizer is included for testing purposes.

### *C. Fully synthesizable implementations*

One of the primary proposed advantages of D-LDO designs is their ease of integration into digital IC flows and possibly automatic synthesis and PnR tools. However, the initial few D-LDO designs based on the D-LDO proposed in [1] were not compatible with most modern automatic RTL to GDSII flows

and processes. In particular, for the D-LDO design proposed in [1], the comparator as well as the power FET switch bank were implemented with full-custom hand layout, and only the digital power FET control logic was capable of being synthesized and auomatically routed.

Since then, many teams have pushed the synthesizability of D-LDO designs and increased their compatibility for integration into automated semi-custom VLSI back-end PnR flows based entirely on digital standard cells. The D-LDO presented in [4] is a design presented in 2016 which achieves a high degree of synthesizability in a 130nm CMOS process by implementing the voltage comparator with a set of cross coupled 3 input NAND gates. This avoids having to implement the latch in a full custom design as was done with the original D-LDO presented in [1] which used a strong-arm latch in a comparator configuration. Furthermore, the D-LDO in [4] synthesizes the power FETs using transmission gate based logic gates which are then laid out manually. Although this implementation is far more suitable for direct integration into a digital circuit flow than the original D-LDO, it can still run into problems with process scaling into modern processes due to its reliance on transmission gate based logic gates, tri-state inverters, and NAND gate based SR style flops, which are often not available in modern process standard cell libraries.

In contrast, the D-LDOs presented in [7] and [8] at ISSCC 2020 have implemented synthesizable D-LDOs in more modern technologies. The D-LDO presented in [7] by a team from Intel is implemented in 10nm CMOS and is synthesized entirely with 10nm CMOS standard cells. The power switch array is also automatically placed and routed, although the integration of the switch array appears to have been done in a bottom-up process to achieve greater control over the power FET layout. The D-LDO implementation presented in [8] is done in 28nm CMOS and also uses NAND gate based comparators as well as synthesized droop detectors and logical controls and actuators. The figure below shows the architecture of the D-LDO presented in [8]. Although these D-LDO designs may not yet be fully automated, they are certainly more compatible and convenient to integrate directly into an automatic digital VLSI flow than the first presented D-LDO designs.

## III. D-LDO Implementations

This project aims to benchmark the improvements from some of the mentioned novel D-LDO architectures in the ASAP7 technology and compare them against each other. The secondary goal of this study is to release a stable D-LDO IP implemented in ASAP7 that can be directly integrated into other ASAP7 projects.

### A. Bi-directional shift register D-LDO

The first D-LDO implemented in the scope of this project is a version of the canonical D-LDO presented in [1]. In this D-LDO scheme, the control logic is a simple bi-directional shift register that enables or disables a switch in the PFET array depending on whether the compared value of the regulated

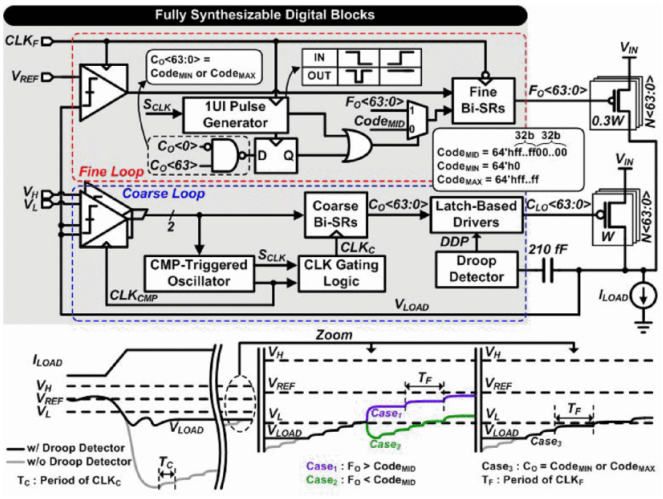


Fig. 5. The architecture of the D-LDO presented in [8] shows each of the fully synthesized blocks in the D-LDO. As with the D-LDO presented in [7], each of the digital blocks in the D-LDO is synthesized using standard cells and an automatic synthesis tool.

voltage is higher or lower than $V_{ref}$. If the value of $V_{out}$ is higher than $V_{ref}$, the bi-directional shift register pushes in a logical 1 to the array of power FET switches, turning a transistor off. Conversely, if the the regulated voltage value is lower than $V_{ref}$, the control logic turns on a power FET in the array. In this way, this scheme achieves all-digital control over the regulated voltage. Figure 6 shows the basic architecture of this digital LDO.

The adaptation of the canonical D-LDO presented in [1] has relatively few design variables to consider and optimize for in its implementation. Specifically, these include the number of transistors in the power FET bank, the selection and design of the comparator used to compare $V_{ref}$ to $V_{out}$ and the selection of an appropriate clock frequency at which to run the design.

The comparator in the design is a clocked comparator which generates the logical signal ($V_{out} > V_{ref}$). This comparator is implemented using a "Strong arm latch" in its clocked comparator application. In order to avoid any possible race condition between the generation of the comparison and its actuation in control logic, the comparison occurs on the negative edge of the D-LDO clock, whereas the control logic triggers on the positive edge.

For this project, the implemented D-LDO was designed to operate at a load current of 200$\mu$A and a 1nF capacitive load to mirror the setup in [1] to allow for direct head-to-head comparison. Values of 16, 64 and 256 were tested for the number of power FETs in the array. Ultimately, a bank of 256 power FETs was used to allow finer control over the regulated voltage/current and to match the setup in [1].

Figure 1 shows an accurate schematic representation of the simple bi-directional shift register implemented in the ASAP7 technology as part of this project. The following section (Section V) describes the simulation testbenches and data analysis performed ont this regulator design.

### B. Dual Loop Control D-LDO

The second D-LDO implemented incorporated a pair of bi-directional shift registers, one for coarse tuning and one for fine tuning the output as demonstrated in [3]. Two different types of tuning allow this D-LDO to approach the desired output quickly, yet provide accurate small adjustements once the D-LDO output voltage is within a very close proximity of the reference voltage. This D-LDO design uses the same comparator as the single loop D-LDO design with a strong-arm latch triggered on the negative edge of the clock.

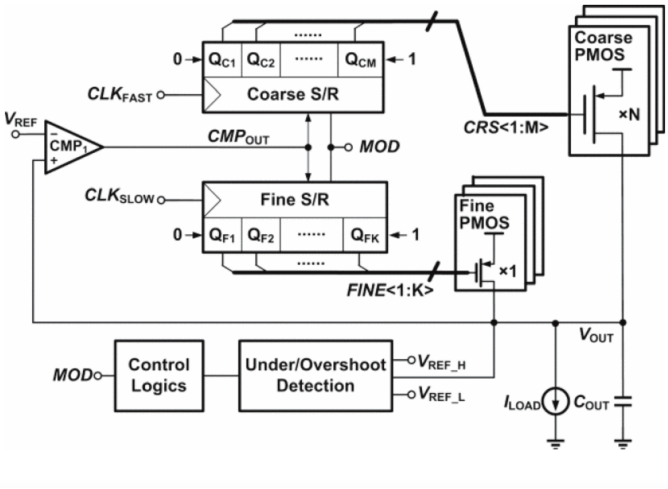


Fig. 6. Diagram referenced in [3] of dual loop control D-LDO design with overshoot/undershoot detection and burst-mode coarse control

This adaptation of the dual loop control D-LDO behaves like an extended version of the single loop D-LDO. The first comparator generates the logical signal ($V_{out} > V_{ref}$) and sets the direction the desired loop should shift the bits in. The shift register then outputs a sequence of bits that control the PFET array depending on the relationship between the current D-LDO regulated output voltage and the D-LDO reference voltage.

In selecting two different loops, the LDO is able to control both the amount that the regulated output voltage is altered by and the speed at which the shift registers alter the control of the PFET array. The coarse control loop is primarily useful immediately after a new reference voltage for the D-LDO is set. This loop divides 1024 power FETs into groups of 16 that can be controlled with a 64-bit output from the associated 64-bit shift register. Since the D-LDO is only briefly in the coarse loop, the reference clock for the coarse loop shift register runs at the relatively fast frequency of the clocked comparator and loop selection control logic.

The fine control loop is primarily useful when settling near the reference voltage or for regulating the output for small adjustments to the reference voltage. The fine loop controls an array of 32 PFET devices individually in order to more accurately tune the regulated output voltage. In an effort to save power consumption during the fine tuning period the D-LDO is primarily in, the reference clock frequency is 10 times slower than that of the coarse control loop.

Furthermore, when choosing which control loop is more desirable for the current state of the D-LDO, an additional pair of reference voltages spaced equidistant from the primary reference voltage are used. These slightly altered reference voltages mark the boundaries of the coarse control and fine control operating regions. In this design, these additional reference voltages, placed 100mV away, tell the D-LDO to operate in fine tuning mode when within their bounds and to operate in coarse tuning mode when outside of them.

In order to make sure the D-LDO isn't stuck in coarse tuning mode oscillating around the edges of the high and low reference voltages wasting unnecessary power, a burst mode was put in place. This burst mode functions to ensure that the D-LDO could only leave fine tuning and use coarse tuning for a brief period of time before being forced to resort to fine tuning for a while, 128 cycles in our design, without being able to transition back into coarse tuning. This helps ensure that the D-LDO settles appropriately when dealing with adjustments that force the D-LDO regulated voltage output outside of the fine tuning region.

Compared to the single loop design previously presented, this dual loop design referenced in [3] provides a regulated voltage output that reaches the desired reference voltage faster and with less power consumed. The ability to alternate between different modes provides the D-LDO with an opportunity to optimize its behavior for specific situations. Finally, a burst mode coarse control loop helps to ensure that power consumption costs are lowered for the design as a whole.

## IV. Results

One of the main goals of this project was to generate a starting point for usable D-LDO IP in the ASAP7 technology. The other main goal was to perform a head-to-head comparison of key D-LDO metrics across different designs in ASAP7 as well as across our designs in ASAP7 to other D-LDO implementations reported in existing literature.

For this project, the key metrics of interest are the dropout voltage of the LDO, the transient reponse time, the current efficiency, and clock frequency independence. The reason we decided to focus on these matrics is because they reflect some of the main advantages and drawbacks of D-LDOs. In particuluar, the main advantage of D-LDOs which led to their increasing adaptation over analog LDOs is their extremely low dropout and ability to operate at very low input voltages. On the other hand a significant drawback of D-LDOs is the potentially long transient response time, dependence on clock frequency and trade off between current efficiency and response time. The simulations in this report explore the impacts of different design choices and technologies on these parameters.

### A. Simulation Setup

Figure 7 shows the basic setup of the D-LDO simulation testbench. Unlike an analog LDO, the D-LDO is a clocked

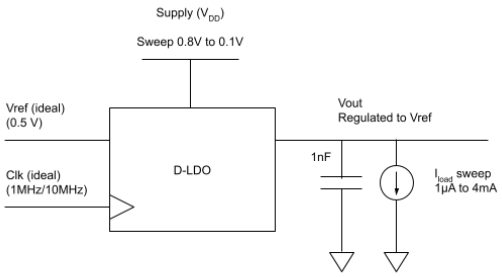


Fig. 7. D-LDO testbench setup with annotations of sweeps performed as well as a list of input and output signals (showing measurements taken and ideal input waveforms where used).

digital circuit and as such is not amenable to a DC or AC frequency/phase analysis. The simulation testbench for the D-LDO presented in [1] consists of an input voltage (the supply), a nominal reference voltage generated by a circuit such as a bandgap-reference, and a load provided by a capacitor and a loading current source which model the active devices being powered by the D-LDO.

In order to achieve highest accuracy measurements of the transient response and the current efficiency of the D-LDO, the testbench is set up to run hspice simulations on an ASAP7 cdl netlist. The analyses performed for each D-LDO design consist of 2 sweeps - one of the load current ($I_{load}$) with supply voltage ($V_{DD}$) held constant, which helps evaluate the current efficiency and line regulation of the design, and another sweep with of the supply voltage ($V_{DD}$) with the loading current held constant ($I_{load}$).

This report presented the following D-LDO designs simulated in the aforementioned setup:

- Design 1: D-LDO with $f_{clk}$ =1 MHz
- Design 2: D-LDO with $f_{clk}$ =10 MHz
- Design 3: dual-loop control D-LDO

### *B. Simulation Results and Discussion*

Figure 8 shows the transient response for designs 1, 2 and 3. The simulation outlined in this figure is performed with a load current of 200$\mu$A and a capacitive load of 1nF. As hypothesized from the discussion, the transient response time of the D-LDOs varies from the $\mu$s range to the 100$\mu$s range, which is typical of the D-LDOs presented in many recent papers such as [1], [4] and [7].

Furthermore, as expected from the aforementioned discussion, the transient response time of design 1 is the slowest with the D-LDO taking close to 100$\mu$s to settle to the eventual output value of $V_{ref}$. The transient response time of the basic D-LDO with a boosted clock frequency of 10MHz (design 2) is much faster, with the output setting to $V_{ref}$ in approximately 40$\mu$s of the start of the simulation. This is expected since the the faster clock rate allows for much faster adjustment of the power FET switches and the faster feedback cycle allowed by the 10MHz clock is substantially faster at correcting

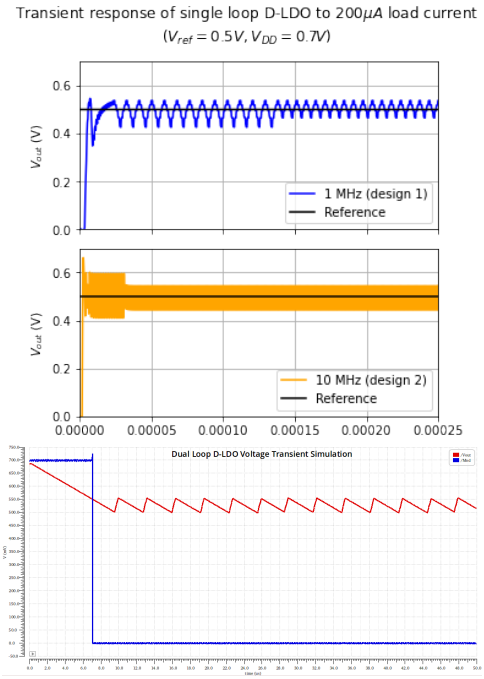


Fig. 8. Transient response characteristics of designs 1, 2 and 3. At the beginning of the simulation, all power switches are turned off and the load current ramps up to a value of 200$\mu$A. Then, the control logic of the D-LDO starts to regulate the output voltage.

overshoots and undershoots. This result is consistent with the result reported in [1], where the 1MHz D-LDO has a transient response time of 590$\mu$s, compared to the 240$\mu$s response time of the 10MHz D-LDO. Similarly, the dual-loop control D-LDO also has a much faster transient response time on the order of magnitude of 1$\mu$s. This corresponds very well with the results of [1] as well as the studies showing a coarse/fine loop control scheme such as [3] and [4] which outline large transient response time performance improvements with the incorporation of a coarse/fine dual loop control scheme.

Figure 10 analyzes the current efficiency of the D-LDO implementations outlined in designs 1 and 2 to study the fundamental trade off experienced by D-LDOs between current efficiency and transient response time, as well as to showcase the operating clock frequency dependence of D-LDOs, which is one of th drawbacks that D-LDO designs face compared to analog LDOs, which oeprate independently of clocked systems and do not face direct current efficiency tradeoffs from such effects.

The current efficiency of the LDO refers to the fraction of the load current sourced by the LDO to the total current consumed by the LDO on the input supply voltage. This ratio gives the % of current that is used by the device being powered by the LDO and is commonly used to measure the power/energy efficiency of an LDO. From this we can expect that a D-LDO with a faster control scheme and associated clock will have a worse current efficiency since there are more operations occuring in a given unit of time which are sourcing

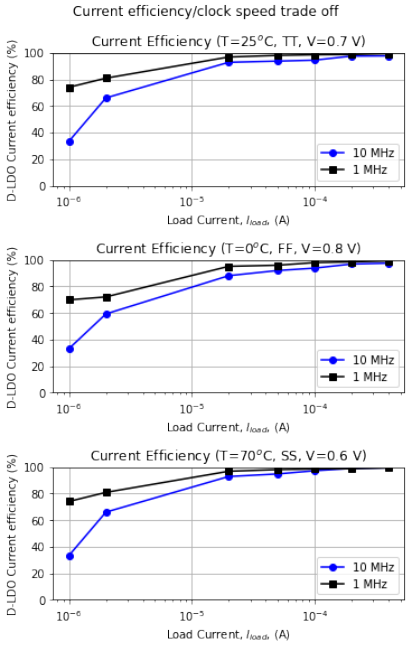


Fig. 9. The performance and efficiency of the DLDO has a strong dependence on operating clock frequency and load current. For a given architecture, there is usually a trade off between current efficiency of the D-LDO and the response time set by the operating clock frequency.

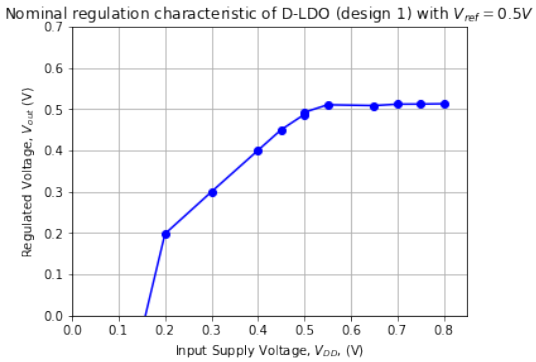


Fig. 10. The D-LDO implemented in ASAP7 has the expected voltage regulation characteristics of low dropout, good scaling with process node and supply reduction, and operability at reduced supply voltages up to 0.55V-0.6V.

and sinking current that is not directly being supplied to the device powered by the D-LDO. From this, we can expect that a D-LDO with a higher clock frequency will have a significantly worse current efficiency. This is seen directly in the analysis presented in [1] and [4], as well as Figure 9, all of which compare the current efficiency of D-LDOs operating at 1MHz and 10MHz across a range of load currents. Since the quiescent current of the D-LDO is relatively independent of the load current, the nominal corenr peak current efficiency of design 1 is achieved at 200$\mu$A with an efficiency of 99.7%. Conversely, the peak current efficiency reached by design 2 is 98.5% at $I_{load} = 200$. From this discussion, it also follows that the current efficiency of design 2 is significantly worse at lower load currents, which is seen clearly in figure 10 as well as the figures reported in [1] and [4].

This analysis clearly reflects the current efficiency-performance trade off faced by D-LDOs. At the time of writing this report, there is no clear single metric used to quantify this trade-off. One metric we propose (efficiency loss$\times$delay product) is to take the product of the "wasted current", denoted by 100%-Current efficiency and the response time normalized to a particular clock frequency. A minimization of this product can help identify which clock frequency to select for the D-LDO. In our study, design 1 has a metric of $13\mu$s whereas design 2 has a metric of $10\mu$s. However, the exact frequency to design for will still likely vary based on application requirements and several other design variables including those related to the device being powered by the D-LDO. Intuitively, the setup corners ($V_{DD} = 0.6V$, ss, $T = 85C$) also have the highest current efficiency for a fixed load current since the quiescent current of the D-LDO is lower).

Although the dual loop control scheme is not reported to help with this trade off [3][4], some other interesting architectured have been proposed to help boost response time without sacrificing current efficiency. The D-LDO in [8] uses a supply voltage droop detector to asynchronously trigger an overshoot/undershoot correction and improve response time. Asynchronous event handling in this way, as reported in [8], can help improve the efficiency loss$\times$delay metric since it provides speedup without using too much excessive switching current per unit time. Unfortunately, due to time constraints we could not implement and test a similar droop detection actuated/asynchronous D-LDO. However, it remains a good idea for further work on this project or a new project as well as an interesting architectural way to handle this trade off.

Figure 11 shows one of the main characteristics of the D-LDO for design 1 - the voltage regulation characteristic with a load of 200$\mu$A at different supply voltages. From the figure we can clearly see that the D-LDO in general has a very low drop-off and can be operated at much lower input voltages than an analog LDO can. This characteristic drop off of around 100mV as well as reliable operation into highly scaled supply voltages has been reported consistently throughout D-LDO literature [1][2][3][4][5][6]. Figure 11 shows that the drop-off characteristic is very similar for all D-LDO designs implemented in the project and clearly depicts one of the major advantages of D-LDOs over analog LDOs which is possibly the primary reason for their growing adoption in power electronics systems.

## V. Conclusion

This project started with the 2 main goals of generating a starting point for D-LDO IP in ASAP7 and a head-to-head benchmarking and comparison of key D-LDO metrics and characteristics in the ASAP7 technology.

The 3 D-LDO designs implemented in this study show the voltage regulation operation and characteristics of digital LDOs, benchmark and examine the transient response of 2

different digital LDO architectures and clock frequencies, and highlight the nature of current efficiency and system clock frequency dependence of digital LDO regulators. In addition to these key metrics whose importance has been discussed in earlier sections, table 1 shows a list of metrics compared between the 3 designs created as part of this project and other D-LDOs demonstrated in studies.

| Reference | design1 | design2 | design3 | [1] | [3] | [4] | [5] | [6] | [7] | [8] |
|---|---|---|---|---|---|---|---|---|---|---|
| Type | Digital | Digital | Digital | Digital | Digital | Digital | Digital | Digital | Digital | Digital |
| Process | ASAP7 | ASAP7 | ASAP7 | 65 nm | 65 nm | 130 nm | 65 nm | 65 nm | 10 nm | 28 nm |
| Active area [mm2] | – | – | – | 0.042 | 0.01 | | 0.017 | 0.0374 | 0.014 | |
| VIN [V] | 0.55-0.8 | 0.55-0.8 | 0.55-0.8 | 0.5 | 0.6-1.1 | 0.6 | 0.7–1.1 | 0.6-1.2 | 0.7-1.05 | 0.5-1.0 |
| VOUT [V] | 0.5 | 0.5 | 0.5 | 0.45 | 0.4-1 | 0.4 | 0.65–1.05 | 0.4-1.1 | 0.65-0.95 | 0.45-0.95 |
| Quiescent IQ [$\mu$ A] | 2.5 | 2.5 | 2.5 | 2.7 | 82 | 5.1-49.8 | 495 | 0.1-107 | 21-57 | 7.7-241 |
| IMAX [mA] | 0.2 | 0.2 | 0.2 | 0.2 | | 25 | 120 | 100 | | 480 |
| Peak current efficiency [%] | 99.7 | 98.5 | 98.4 | 98.7 | 99.92 | 99.9 | 99.6 | 99.5 | 98.6 | 99.99 |
| Line regulation [mV/V] | 9.6 | – | – | 3.1 | 3 | 2.5 | 15 | | | |
| Load regulation [mV/mA] | 0.14 | 1.05 | – | 0.65 | 0.06 | 2.4 | 0.6 | | | |
| Load capacitor CL [nF] | 1 | 1 | 1 | 100 | 1 | | 0.5 | | 0.534 | 0.0041 |
| Max voltage droop [mV] @ Load step | 60 | 60 | 60 | | | | 371 @ 80 mA | 108 @ 50 mA | 200 @ 1.17 A | |
| Response time TR * [$\mu$ s] | 130 | 35 | 9 | 590 | 700 | | 2.1 | | | |

TABLE I
PERFORMANCE OF D-LDOS REFERENCED IN THIS REPORT AGAINST DESIGNS 1-3

As a whole, the main adoption advantage of D-LDOs appear to be the small load capacitance and dropout they can provide over analog LDOs. However, while designing and using D-LDOs, it is important to keep potential pitfalls such as transient response time, operating clock frequency dependence and current efficiency impacts closely in mind. In addition to the architectures and techniques discussed in detail in this report, there are many more recent novel architectures and implementation proposed to improve the performance of D-LDOs. Some of these include transient cycle enhancement by using switched capacitors and voltage boosts [2], asynchronous actuation of the D-LDO control logic [8], time domain signal comparator signal processing to significantly improve response time [5][9], and ripple sensitive feedback/feedforward path incorporation [10] and many more. In addition, many other sources including [3][7] etc. focus as well on the ease of integration of digital LDOs into digital on top systems and also claim full synthesizability and compatibility with automatic industry PlaceRoute tools of D-LDO circuits. While these benefits are indeed significant over analog LDOs which require iterative analog/mixed signal layout and stability closure across corners, many of the claims of full synthesizability and automatic PnR compatbility rely on having custom standard cells for processes that allow for the easy creation and insertion of the power FET bank and the sensing circuits such as the $V_{ref}$ comparator, droop detectors, etc. As a result, in the implementations outlined in this proejct using the ASAP7 PDK, the targets of full synthesizability or automatic placement/routing were very difficult to meet.

Nonetheless, for the reasons outlined in this report, digital LDOs continue to be a fascinating and recent innovation with many more architectural and circuit level points for improvement and continue to be an excellent topic for further study or practical implementation in the area of power electronics.

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