PROJECT

CS/ECE/EEE/INSTR F241
Microprocessor Programming & Interfacing

Batch No. 29
Question no. 22

SPIRIT LEVEL REACTION TIME TESTER

SUBMITTED BY

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Description

It is a Spirit Level Reaction Time Tester which is used for testing sobriety of a person. When the ‘start’ button is pressed, a random delay of time interval(4 – 8 seconds) is generated after which the first LED of the LED bar graph (consisting of 9 LEDs) is lit after which the LEDs on the bar graph begin incrementing on a bar graph display so that they appear to 'rise' upwards. The user has to press the ‘Stop’ button as soon as she sees the LED bar rising.

The earlier the button pressed, fewer the LEDs lit and hence higher the sobriety. The entire bar graph of 9 LEDs will sweep to the top in 0.4 seconds (50ms delay between lighting of each LED) . The sobriety of a person on a scale of 1- 5 (1 – maximum intoxication) is displayed on a seven segment display according to the number of LEDs lit before the user has pressed the stop button.

Assumptions

1. The person who is getting tested does not know the time when the spirit level tester in powered on.
2. Pressing of start button will be ignored until one test finishes completely.
3. Intoxication level is assumed to be linearly dependent on led lit before stop button.
4. Assuming debounce time is very less compared to one test time. hence no need to take debounce into consideration because start debounce happens in between the game(which will be ignored) and stop debounce will happen after the game (which also will be ignored).

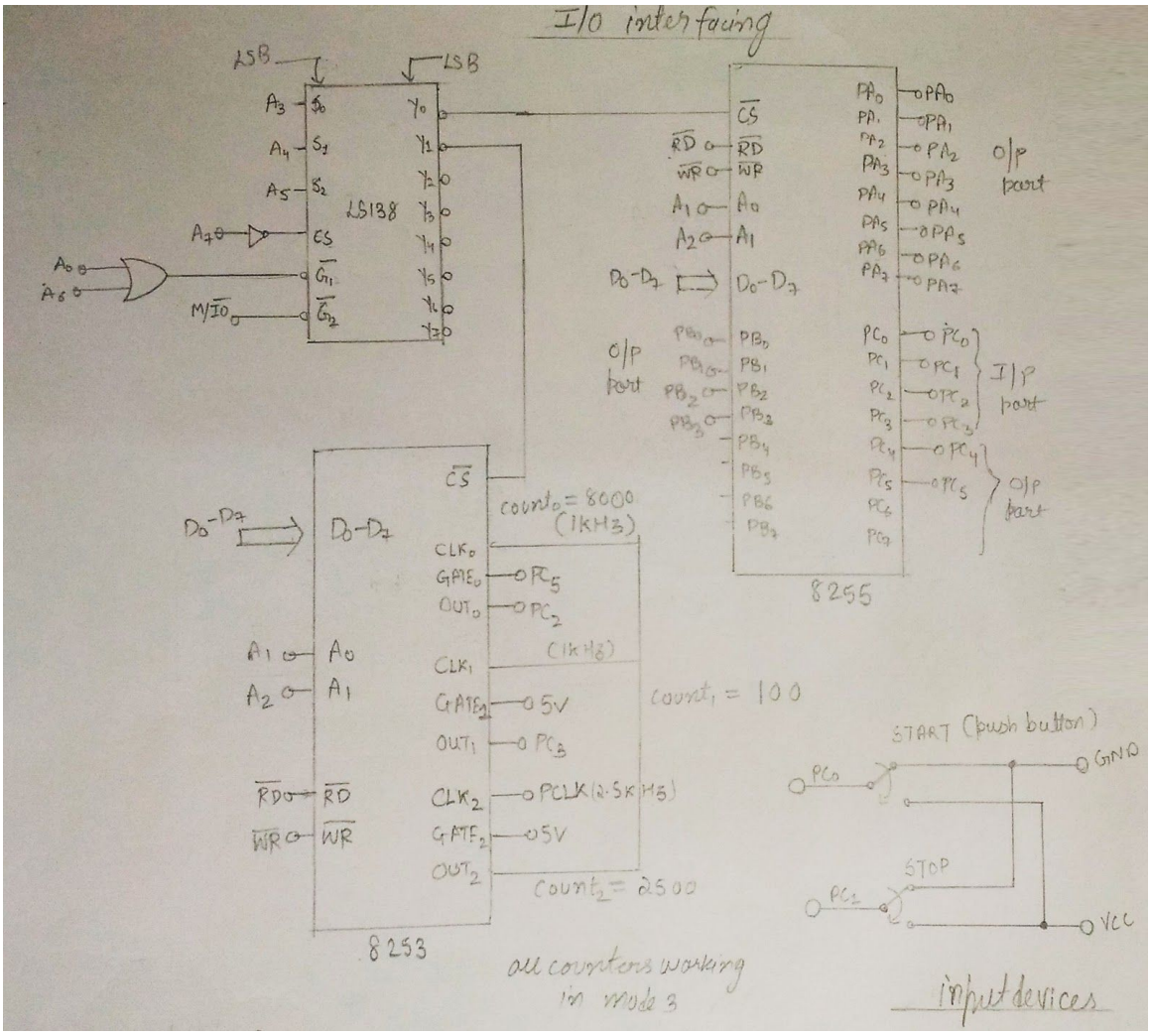
Components

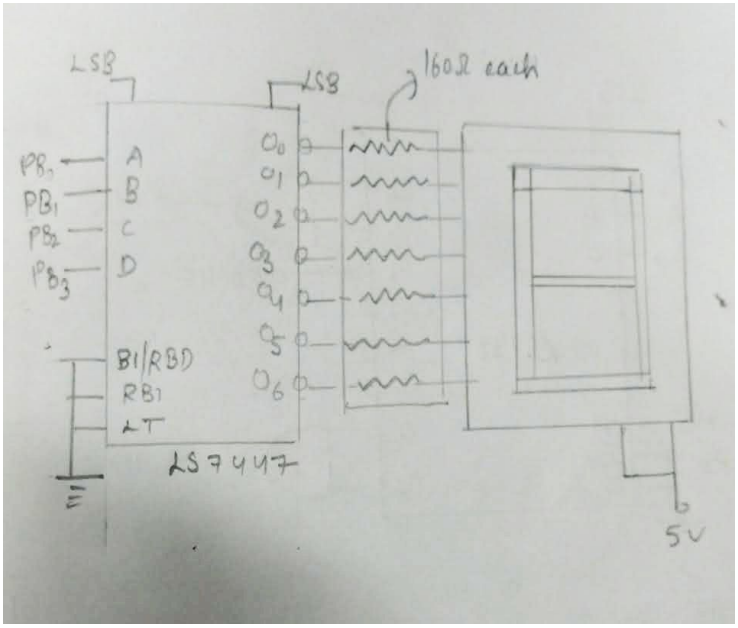
COMPONENT	QTY
8086 Microprocessor	1
8255 Programmable Peripheral Interface	1
8253 Programmable Interval Timer	1
8284 Clock Generator	1
7 Segment Display	1
9 LED Bar Graph (9 LEDs)	1
74LS47 BCD to 7-Segment Decoder	1
74LS373 Octal transparent latch with 3 state outputs(8 bit buffers)	3
74LS245 Octal bus trans-receiver (2-way 8 bit buffers)	2
6116 RAM chip	2
2732 ROM chip	4
74LS00 AND gates	4
74LS02 OR gates	1
74LS32 NOT gates	1
74LS138 3:8 Decoder	3
Buttons	2
Resistors	3
100nF Capacitors	2
15 MHz crystal	1

Interfacing

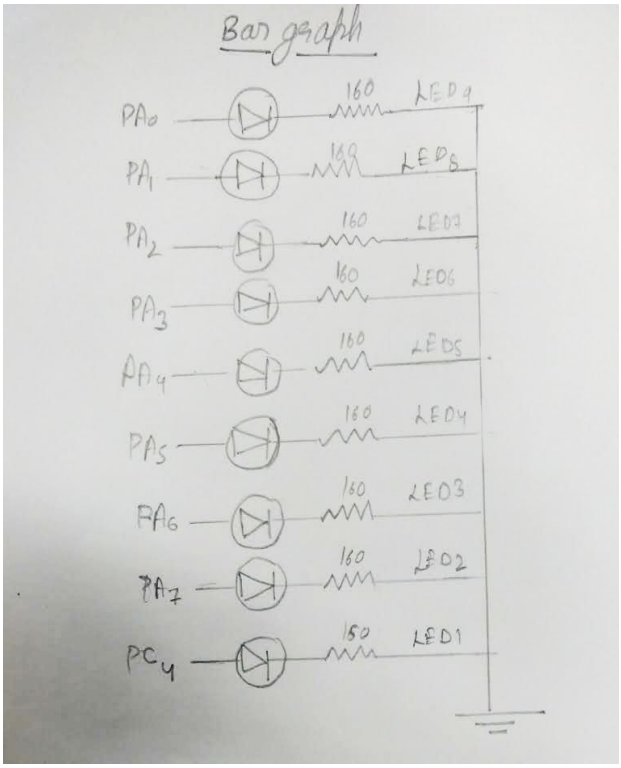
I/O Interfacing

Component	Address
8255	00h-06h
8253	08h-0Eh



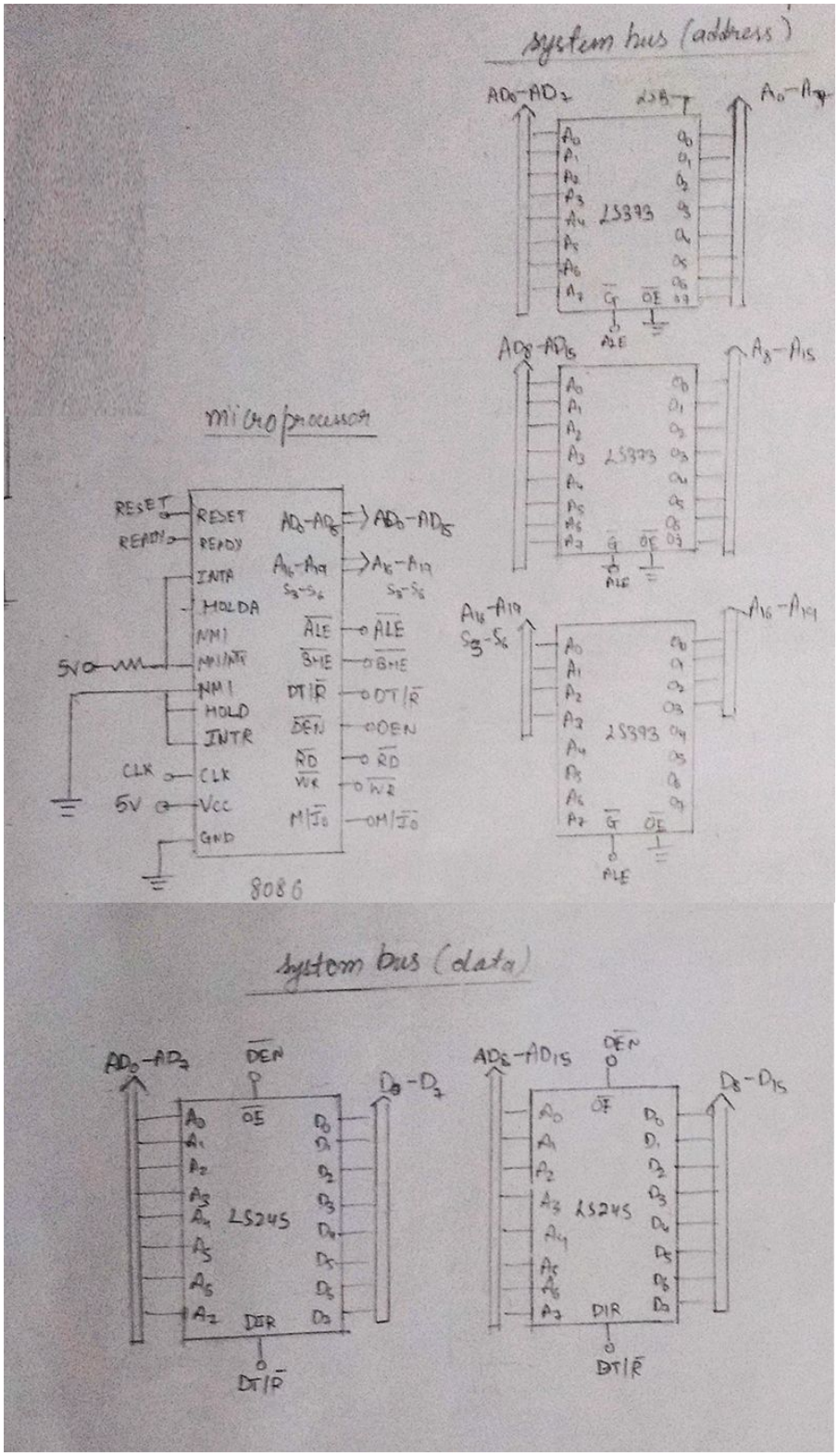


7 Segment Display



LEDs

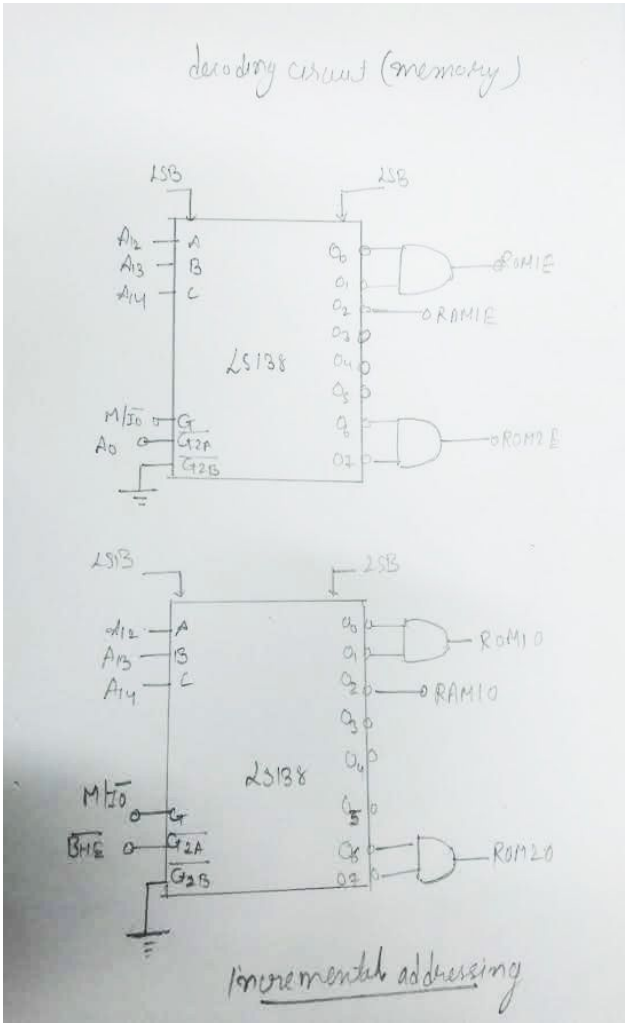
Data Interfacing



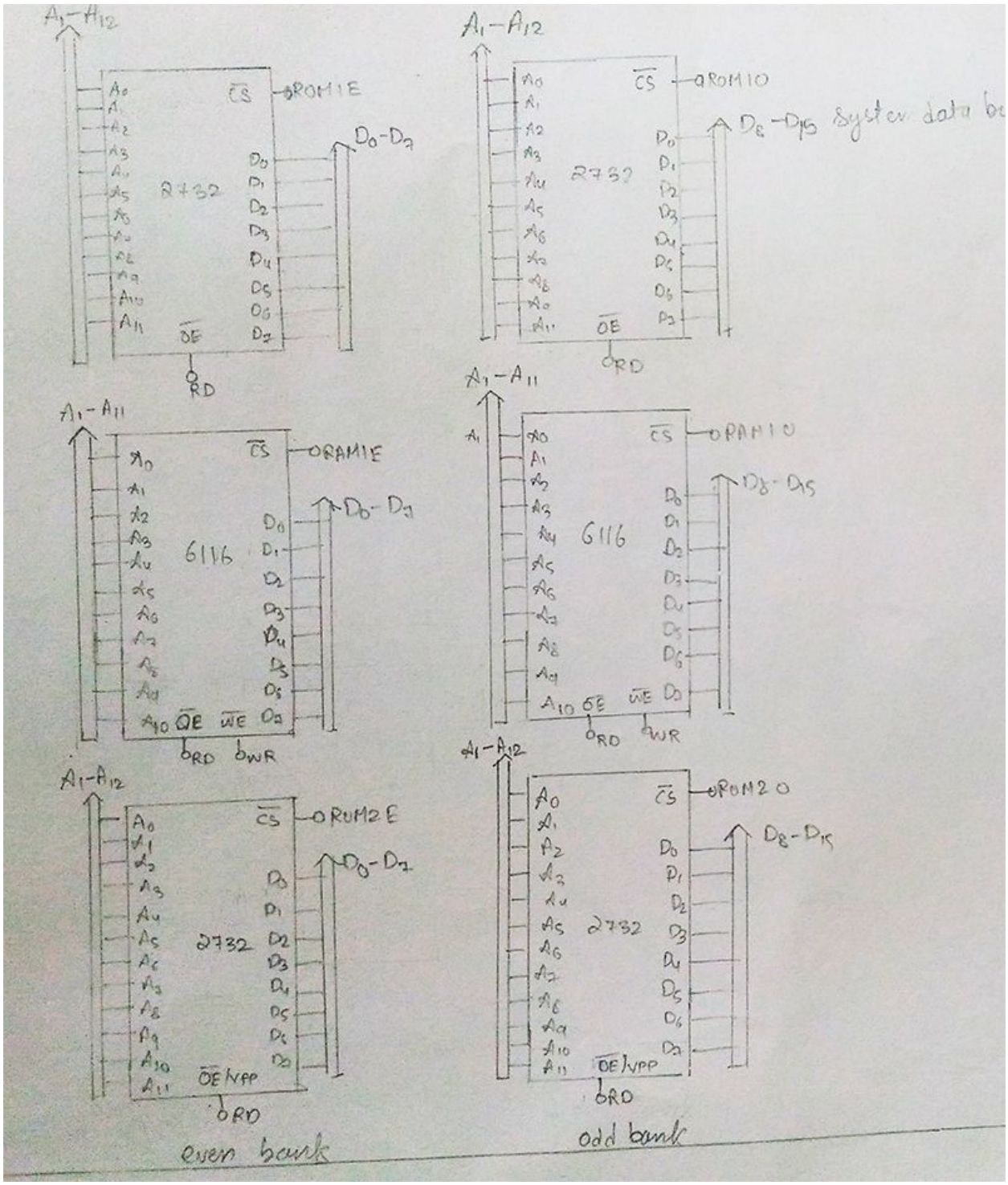
Memory Interfacing

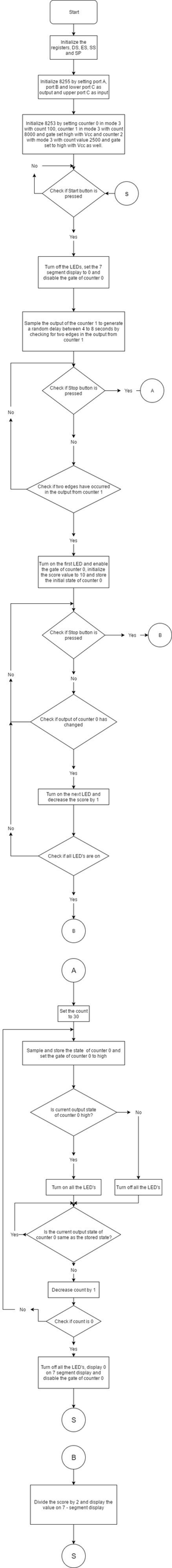
Component	Starting Address	Ending Address
ROM1	00000h	01FFFh
ROM2	FE000h	FFFFFh
RAM1	02000h	02FFFh

Decoding Circuit



Memory Mapping




Start
Initialize the registers, DS, ES, SS and SP
Initialize 8255 by setting port A, port B and lower port C as output and upper port C as input
Initialize 8253 by setting counter 0 in mode 3 with count 100, counter 1 in mode 3 with count 8000 and gate set high with Vcc and counter 2 with mode 3 with count value 2500 and gate set to high with Vcc as well.
No
Check if Start button is pressed
S
Yes
Turn off the LEDs, set the 7 segment display to 0 and disable the gate of counter 0
Sample the output of the counter 1 to generate a random delay between 4 to 8 seconds by checking for two edges in the output from counter 1
Check if Stop button is pressed
Yes
A
No
No
Check if two edges have occurred in the output from counter 1
Yes
Turn on the first LED and enable the gate of counter 0, initialize the score value to 10 and store the initial state of counter 0
Check if Stop button is pressed
Yes
B
No
No
Check if output of counter 0 has changed
Yes
Turn on the next LED and decrease the score by 1
No
Check if all LED's are on
Yes
B
A
Set the count to 30
Sample and store the state of counter 0 and set the gate of counter 0 to high
Is current output state of counter 0 high?
No
Yes
Turn on all the LED's
Turn off all the LED's
Yes
Is the current output state of counter 0 same as the stored state?
No
Decrease count by 1
No
Check if count is 0
Yes
Turn off all the LED's, display 0 on 7 segment display and disable the gate of counter 0
S
B
Divide the score by 2 and display the value on 7 - segment display
S