Introduction to HDL and VHDL

Hardware Description Language(HDL)

- A **H**ardware **D**escription **L**anguage (**HDL**) is a language used to describe a digital system, for example, a computer or a component of a computer.
- A digital system can be described at several levels:
  - **Register Transfer Level (RTL)** : registers and the transfers of information between registers.
  - **Gate level** : logical gates and flip-flops
  - **Switch level** : wires, resistors and transistors
- **Two Major HDLs in Industry**
  - VHDL (Mostly in Europe)
  - Verilog HDL (Mostly in USA)

Schematic design entry can be replaced by writing HDL code that CAD tools understand.

CAD tools can verify the HDL codes, and create the circuits automatically from HDL codes.

Verilog HDL vs. VHDL

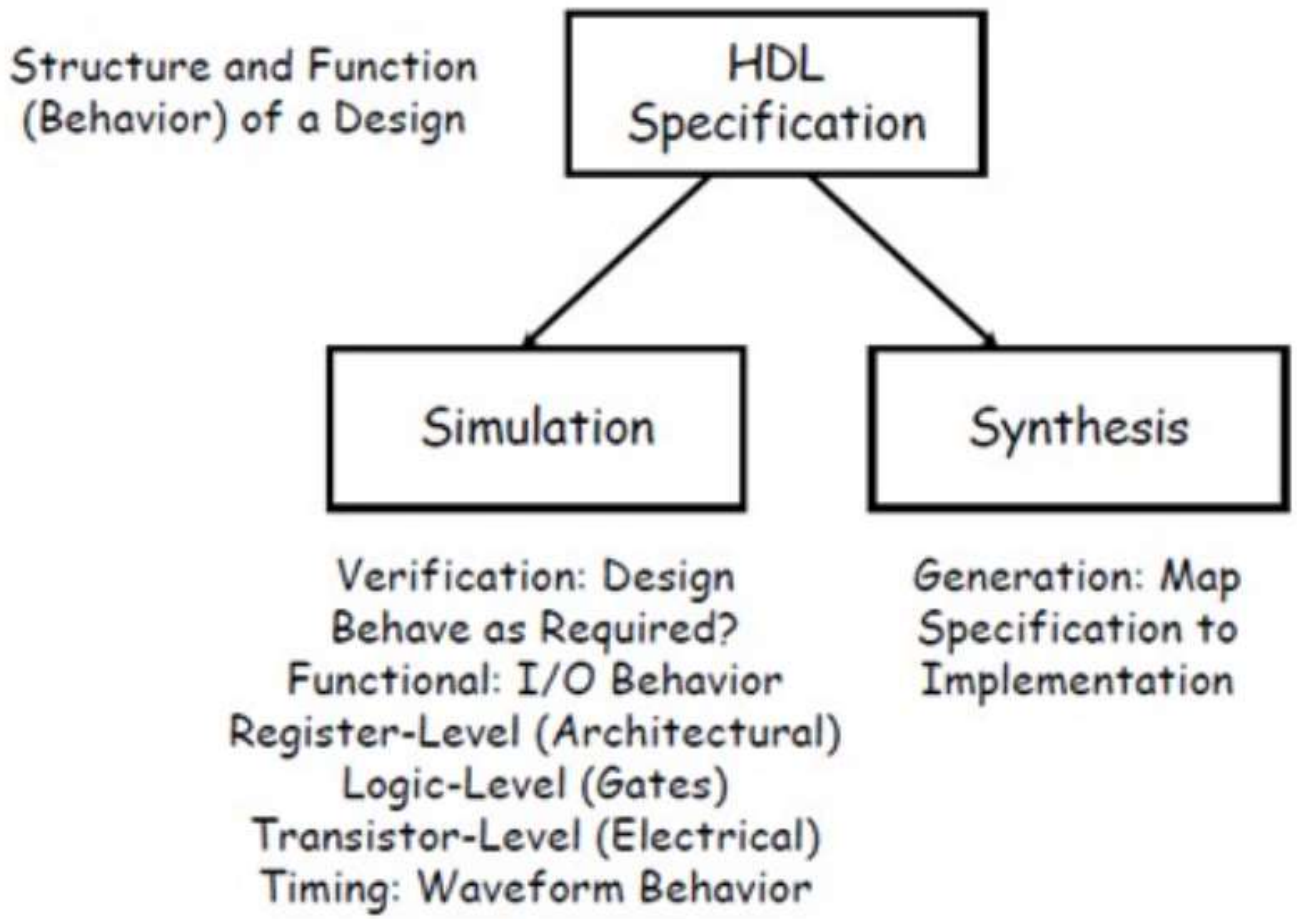
VHDL

- “V” is short for Very High Speed Integrated Circuits.
- Designed for and sponsored by US Department of Defense.
- Designed by committee (1981-1985).
- Syntax based on Ada programming language.
- Was made an IEEE Standard in 1987.

Verilog HDL

- Was introduced in 1985 by Gateway Design System Corporation, now a part of Cadence Design Systems, Inc.'s Systems Division.
- Was made an IEEE Standard in 1995 (IEEE 1364)
- Syntax based on C programming language.

Design Methodology



Advantages of HDL

- Can express large complex design
- Flexible modelling capabilities
- Productivity
- Reusability
- Documentation
- Description can include the very abstract to very structural level
- Case insensitive

Advantages of HDL

HDL is a program that allows the user to implement complex functions

Digital systems are complex. Example: Processor

Designing a function with 10,000 gates in schematic is very difficult.

An HDL makes it easy by simply describing the function.

A tool can convert the described function in HDL into logic gates (Synthesis step in the design flow)

VHDL(Very high speed integrated circuit(VHSIC)Hardware Description Language)

- VHDL was developed to provide a standard for designing digital systems.
- VHDL specifies a formal syntax. The designer creates a design file using that syntax .
- The designer then synthesizes the design using only design package that can accept VHDL files. This is equivalent to the programmer compiling the C-program. It checks for errors in syntax and declaration, but not in logic.
- Finally, the designer debugs the design using simulation tools.

Advantages of VHDL:

- PORTABILITY:
  Just as a valid C-program can be compiled by any compliant C compiler, a VHDL design can be synthesized by any design system that supports VHDL.
- DEVICE INDEPENDENT:
  The VHDL file is device independent. The same file can be used to implement the design on a custom ICs, on ASICs or any PLD that is capable of containing the design.
- SIMULATION:
  VHDL designs can be simulated by the design system, allowing the designer to verify the design performance before committing it to hardware.
- SYSTEM SPECIFICATION:
  The designer can design the system using a high level of abstraction , such as a finite state machine, down to a low level digital logic implementation.

Disadvantages of VHDL:

- VHDL source code often becomes long and difficult to follow, extreme verbose coding
- Missing a single signal may cause major difference between simulation and synthesis
- May be more difficult to visualize and troubleshoot a design.

VHDL Code Half adder

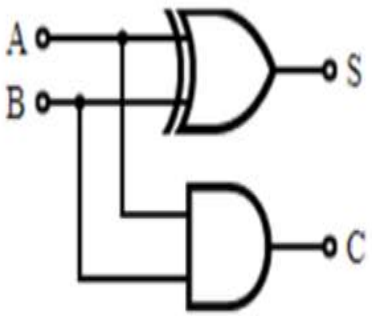
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity half_adder is
   port(a,b:in bit; sum,carry:out bit);
end half_adder;

architecture data of half_adder is
begin
   sum<= a xor b;
   carry <= a and b;
end data;
```

Half adder Circuit Diagram.

Half Adder Truth Table			
A	B	Carry	Sum
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0



Half-Adder Schematic

www.androideroded.com