

Pre-University Examination Questions

paper collection



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Pokhara University
Everest Engineering College
Final Internal Assessment
Spring- 2025

Level: Bachelor

F.M. 100

Program: BE CMP(4th Semester)

P.M. 45

Faculty: Science & Technology

Time: 3hrs

Section:

Subject: Computer Architecture

Attempt all the questions.

1 a) Define Computer Architecture. Draw a neat structure of a computer system and explain its four general functions. 8

b) Define addressing mode. Explain about different addressing modes with appropriate figures and example of each. 7

2 a) Draw an instruction cycle state diagram with interrupts and explain how it works. 8

b) Design a 4-bit ALU using one-bit ALU design. Also draw a sample 1-bit ALU along with the function table for all the works it can perform using S0, S1 and Cin. 7

3 a) What is associative memory? Explain the match logic for associative memory with the help of diagram and Boolean equation. 8

b) Multiply 13 by -7 using Booth's algorithm. 7

4 a) Why is DMA needed even though we have interrupt driven I/O and programmed I/O. Draw a neat diagram of a DMA controller connected to a CPU and then explain the operations of a DMA transfer. 7

b) Draw a block diagram of microprogrammed sequencer and explain the operation on a one address microinstruction format control unit. 8

5 a) What is pipelining. Explain the hazards prevalent in pipelining and provide the solution for all the hazards. 8

b) Explain on how can we connect multiprocessor system using the interconnection structures and explain them all. 7

6 a) Compare and contrast between dual core, quad core and octa core computers. 7

b) How can you achieve parallelism in uniprocessor system? Explain about Flynn's classification of Parallel Processors. 8

7 Write short notes on: (Any two)

2*5=10

a) RISC vs CISC

b) Vector Processor and Array Processor

c) Hardware Performance issues in multicore system.

****Best Wishes****

GANDAKI COLLEGE OF ENGINEERING AND SCIENCE

Level: Bachelor Semester: Spring Year : 2025
Programme: BE CE IV Full Marks: 100
Course: **CMP 262 : Computer Architecture** Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

Attempt all the questions.

- | | | |
|----|--|-----|
| 1. | a) Differentiate Computer organization and Computer architecture in detail with example. | 4+4 |
| | b) Explain various types of micro-operations in detail with examples. | 7 |
| 2. | a) What is the instruction cycle? Explain various sub cycles involved in instruction cycle with the help of T states. | 2+5 |
| | b) Explain about the micro-programmed and hardwired control unit in brief. | 8 |
| 3. | a) Verify the operation $(8) \times (-3)$ using Booth's algorithm. | 8 |
| | b) How is the floating-point number represented in a computer system explain in brief? | 7 |
| 4. | a) Register Windowing and Register Renaming is the techniques used in RISC pipeline. Explain this in detail with examples. | 7 |
| | b) Explain cache write policy in brief and explain FIFO, LFU cache replacement algorithm with example. | 4+4 |
| 5. | a) Explain in detail about I/O processor and I/O channel describing the communication steps in detail. | 8 |
| | b) Explain Flynn's classification of computer system in detail. | 7 |
| 6. | a) Explain different hardware and software performance issues in multicore computers. | 4+4 |
| | b) Explain different types of interconnection structures in multiprocessors. | 7 |
| 7. | Write short notes on (Any Two) | 2x5 |
| | a) GPU and TPU | |
| | b) VHDL program for Half Adder | |
| | c) Microinstruction sequencing and execution. | |

Term Test II

Date:	2082/04/11	Full Marks	70
Level	BE		
Programme	BCE	Time	
Semester	IV		2 hrs

Subject: - Computer Architecture

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt all questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

- 1) a. Explain in detail about the four stage instruction pipeline with necessary diagrams. [10]
- b. What is Parallel Processing? Show that the Speed up factor of a pipelined processor is equal to the number of stages in a pipeline. [10]
- 2) a. Explain about Direct Mapping in detail. Explain about Array Processing and its types. [10]
- b. What is System Bus? Draw the block diagram of micro programmed Control unit and explain in detail. [10]
- 3) a. Explain how data transfer is performed with Direct Memory Access (DMA) technique with necessary diagram. [10]
- b. Explain about the Conflicts that can be seen in instruction pipeline. How can they be resolved? Explain. [10]
- 4) Write Short Notes on: (Any ONE) [2*5=10]
 - a. CPU-IOP Communication
 - b. Interconnection structures in multiprocessors

**Madan Bhandari College of Engineering
Urlabari-3, Morang
Final Internal Examination**

Level: Bachelor of Computer Eng.

Full Marks: 100

Programme: BE

Pass Marks: 45

Year/Part: II/II

Time: 3 hrs

Subject: - Computer Architecture

1. a) Define instruction. Explain the Addressing mode of 8085 with an example. (8)
b) Define RTL, Explain the term SSI and VLSI. (7)
2. a) Draw internal CPU structure and explain each part. (7)
b) Define micro-operation? Explain the basic component used in register organization.(8)
3. a) Draw flowchart of Booth's algorithm and use it to multiply $(-3)_{10} * (-7)_{10}$.
b) Draw the flowchart of Unsigned Binary Division Algorithm and use to divide 8 by 3.
4. a) Differentiate between Hardwired and Micro-programmed control unit. Which one is Preferable and why? Illustrate. (8)
b) Evaluate the segments using arithmetic pipeline. Let the mathematical operation is $A_i * B_i + C_i$ for $i=1,2,3.....7$. (7)
5. a) What is cache coherence? Explain Direct mapping technique. (8)
b) Differentiate between HDL and VHDL (7)
6. Define Associative memory. Explain any two type of micro- instruction sequencing technique. (2+8)
7. Write short notes on: (7.5x2=15)
 - a) RISC vs CISC
 - b) Cache Replacement Algorithm

THE END

Universal Engineering & Science College

Affiliated to Pokhara University

Chakupat, Lalitpur

Level: Bachelor

Semester: 4th

Year : 2025

Programme : BE Computer

Time : 3 hours

Full Marks: 100

Subject: Computer Architecture

Pass Marks: 45

Pre-Board Examination-2082 (Spring 2025)

Candidates are required to give their answer in their own words as far as possible. The figure in the margin indicate full marks

Attempt all the questions:

1. a) What do you mean by addressing modes? Explain the different types of addressing modes with suitable examples and diagrams. [7]

- b) Evaluate the expression: $X = (A + B) * (C + D) / E$ using three-address, two-address, one-address, and zero-address instructions. [8]

OR

Explain the hierarchical structure of a computer system in detail. Also, briefly describe the future trends in computing.

2. a) What is an instruction cycle? Briefly explain the design principles of modern computer systems. [8]

- b) Write the basic structure of a VHDL program. Also, provide the VHDL code for a full adder using component instantiation. [7]

3. a) Define RTL. Explain bus and register transfer operations in RTL. [7]

- b) Registers in the CPU perform two major roles. Identify the various types of registers involved in fulfilling these roles. Draw a labeled diagram of the IAS computer. [8]

4. a) Define control memory. Explain the working of a microprogrammed control unit. Differentiate between horizontal and vertical microprogrammed control units. [8]

- b) Describe the hardwired control unit in detail with a block diagram. Why is it faster than the microprogrammed control unit? [7]

OR

Why is microinstruction sequencing important? Explain the variable address field sequencing technique with a necessary block diagram.

5. a) Use Booth's Algorithm to multiply 17 by 4. Also, differentiate between RISC and CISC architectures. [7]
- b) How are floating-point numbers represented in a computer? Also, explain how floating-point addition and subtraction are performed. [8]
6. a) Prove that the "speedup factor for a pipelined processor is equal to the number of pipeline stages." Assume the pipeline has $K=8$ segments and executes $n=212$ tasks in sequence. Let the time taken to process each sub-operation in a segment be 35 ns. Calculate the speedup ratio. [8]
- b) What are pipeline hazards? How can they be eliminated? [7]

OR

DMA overcomes the limitations of programmed I/O and interrupt-driven I/O. Justify this statement.

7. Write short notes on **any two** of the following: [5 × 2 = 10]
 - a) GPU vs. TPU
 - b) Flynn's Classification
 - c) Direct Mapping
 - d) Register Renaming and Register Windowing

NEPAL COLLEGE OF INFORMATION TECHNOLOGY
Assessment Spring 2025

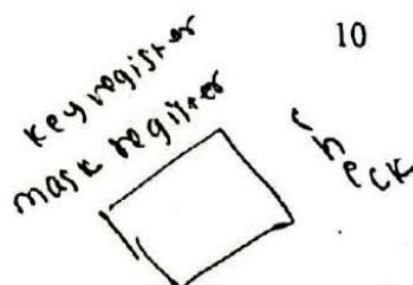
Level: Bachelor
Program: B.E.CE(IV_Mor and Day)
Course: Computer Architecture

Total Marks: 100
Pass Marks: 45
Time: 3 hrs

Attempt all the questions.

- 1) a) What are the functional requirements of a computer that leads to design the architecture of a computer system? Explain with their components. 8
- b) What are the principles that are required to design today's modern system? Explain in detail. 7 micro instructions, performance speed
- 2) a) Ordinary representation of number is not suitable in computer. Explain the way how they can be represented. 7
- b) Perform 16*5 multiplications using Booth's Algorithm. 8
- 3) a) Write control signal to involve various micro operations involved executing a instruction with help of data path diagram of a simple CPU. 7
- b) Differentiate hardwired control unit and micro programmed control unit in detail. 8
- 4) a) What is associative memory? Explain about read write operation in associative memory? 7
- b) Explain the role of an I/O module in computer architecture. Compare programmed I/O, interrupt-driven I/O, and direct memory access. 8
- 5) a) What is pipelining? What are the hazards of instruction pipelining and how can they be resolved? 8
- b) Differentiate dual core, quad core and octa core processors. 7
- 6) a) Perform unsigned binary division of 11/9. 8
- b) What is VHDL? Write VHDL code for 4 to 1 mux.
 7
7. Write Short notes on (any two): 10

- a) Register Organization
- b) Multithreaded architecture
- c) Vector Processors



NEPAL ENGINEERING COLLEGE
INTERNAL ASSESSMENT

Level: Bachelor	Semester – Spring	Year : 2025
Programme: BE (Computer 4 th Sem)		Full Marks : 100
		Pass Mark : 45
Course: Computer Architecture (New)		Time : 3 hrs

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | | |
|----|----|---|---|
| 1 | a. | What is RTL? Explain about different types of RTL transfer operation.[8] | 8 |
| . | | OR | |
| | | Write a VHDL code for Half Adder and Full Adder. | |
| b. | | What is the major criterion that distinguishes Computer Organization from Computer Architecture? List and briefly define some of the computer technologies that are trending presently or will be trending in the future. | 7 |
| 2 | a. | What is the difference between indirect addressing and register indirect addressing mode? Explain about the general organization of registers in CPU. | 8 |
| . | b. | What is a control memory? Explain the mechanism of variable format micro-instruction sequencing technique with a neat diagram. | 7 |
| 3 | a. | Using Booth's algorithm, evaluate the following expression: $-9 * -13$. | 8 |
| . | b. | Write an algorithm flowchart of restoring division algorithm and use it evaluate $7/5$. | 7 |
| 4 | a. | Define cache memory. Explain the types of write policy of cache memory. Give the appropriate reasons why replacement algorithm is required in associative mapping? | 7 |
| . | b. | What is/are the difference(s) between isolated I/O and memory-mapped I/O? Why peripherals are not connected to the system bus directly? Give at least three reasons. | 8 |
| 5 | a. | Draw instruction cycle state diagram with interrupt. Describe each state briefly. | 8 |
| . | b. | Draw a neat diagram of a DMA controller and describe its working | |

mechanism. Why read and write control lines in a DMA controller are bidirectional? 7

OR

How parallelism occurs in uniprocessor system? What is the inter-connections structure possible in multiprocessor system?

- 6 a. Explain data hazard in instruction pipelining and its various types. 7
Also determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline.

- b. Let us suppose an arithmetic operation $(A_i + B_i) * (C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for $i = 1$ through 6. 8

OR

What are the hardware and software performance issues that arise in multicore organization?

- 7 Write short notes on (Any Two): 2×5
- a) Differences between horizontal and vertical microinstruction
 - b) Control Memory, CAR and CBR
 - c) Communication between CPU and IOP with suitable diagram.
 - d) Flynn's classification.
 - e) RISC vs CISC

POKHARA ENGINEERING COLLEGE

Internal Assessment Examination

Level: Bachelor

Semester - Spring

Year : 2025

Programme: Computer

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define the term Computer Architecture. Explain different addressing modes with appropriate figures and example of each. 2+6
b) Define RTL. Explain different microoperations used in computers. 2+5
2. a) Define register. Explain about the register organization in detail. 2+6
b) Explain in brief about different microinstructions used in different sub cycles of instruction cycle. 7
3. a) Perform -12×-15 using Booth's algorithm. 7
b) How do we represent floating point numbers in computer? Explain floating point operation using Arithmetic Pipelining. 8
4. a) Compare and Contrast between RISC and CISC architecture. 7
b) Explain the different sequencing techniques applicable in Microprogrammed Control Unit. 8
5. a) Why is Cache Memory called influential memory? Explain how Set Associative Mapping overcomes the drawbacks of Associative and Direct Mapping. 2+6
b) Define DMA. Explain how DMA performs the control, transfer and execution of data accompanying CPU. 1+6
6. a) A non-pipeline system takes 100 ns to process a task. The same task can be processed in a six-segment pipeline with time delay of each segment in the pipeline is as follows; 30 ns, 35 ns, 40 ns. Determine the speed of ratio of pipeline for 50 tasks. 7
b) Define multiprocessor. Classify and explain computers in accordance to Flynn's classification. 2+6

7. Write short notes on **any two**:

- a) Pipelining Hazards
- b) VHDL
- c) Types of Interrupts

Good Luck

Computer Architecture (new), Ashar 31st, Spring 2025

Total marks: 100, Pass marks: 45

BoCE IV semester

Attempt all the questions.

1. a) What are the advantages of the Harvard architecture in relation to the Von Neumann architecture? Explain. (7)
b) Explain the terms. (4x2)
i) addressing modes ii) instruction set architecture iii) instruction cycle iv) micro-operation

2. a) What is CPU organization? Describe Register Organization in details (7)
b) What is Booth's Algorithm in Computer Architecture? Explain (8)

3. a) What is Cache Mapping? Explain Cache Replacement Algorithm with a suitable example. (2+5)

OR

Explain various storage devices of memory hierarchy.

- b) What is the difference between hardwired control unit and a micro programmed control unit? Explain the relative difference of each. (8)

4. a) DMA is a hardware-based transfer. Justify (7)
b) Why I/O module is necessary? Explain the communication process between CPU and I/O channel. (8)

5. a) What is register transfer language? Compare and contrast between arithmetic and logical micro-operation. (2+5)

- b) How can we improve performance on hardware and software while designing a processor? Explain. (8)

OR

What is power efficient processor? Explain dual core processor with respect to quad core processor.

6. a) Explain instruction pipelining with suitable example. (7)
b) Discuss about RISC pipeline with example. (8)

7. Write short notes on (Any Two): (2X5)

- i) GPU and TPU
ii) Floating point representation
iii) Cache Write Policy

UNITED TECHNICAL COLLEGE

Level Bachelor

Programme (II)

Course: Computer Architecture

Semester - Spring

Year 2025

Full Marks: 100

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) The term "computer architecture" and "computer organization" are same or different, explain with examples. 7
- b) Explain the functional view of the computer system with reference to each component. 8
2. a) Define RTL. Write RTL for fetch, indirect and interrupt cycle. 7
- b) Write a VHDL program for half and full adder. 8
3. a) Explain the operation of microprogram sequencer used in microprogramming CU with block diagram. 8
- b) Explain Booth algorithm and use it to multiply $(-5)_{10} * (-7)_{10}$. 7
4. a) Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. 7
- b) What is pipelining? Explain arithmetic pipelining. 8
5. a) Explain various communication techniques for I/O devices. 8
- b) How instruction pipelining supports in parallelism? Explain. 7
6. a) What is cache mapping? Explain cache replacement algorithm with a suitable example. 7
- b) Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems. 8
7. Write short notes (Any Two): 2
 a) Vector processors and Array processors x
 b) Control Unit 5
 c) DMA

National Academy of Science and Technology

(Affiliated to Pokhara University)

Dhangadhi, Kailali

Pre-University Examination

Level: Bachelor

Semester: IV_Spring

Year : 2025

Program: B.E. Computer

F.M. : 100

Course: Computer Architecture

P. M. : 45

Time : 3 Hrs.

Candidates are required to give their answer in their own words as far as practicable. The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the basics of designing computer architecture? 7
b) Define RTL. Write in RTL for the following statements:
 - i. Add R1 and R2 and transfer to R3 when I is true. 8
 - ii. Logical shift R3 through right and transfer it to R3.
 - iii. R3 and R4 are XORed and transferred to R5.
2. a) Explain about design principles for modern systems. 8
b) Perform -6×-7 using Booth's algorithm. 7
3. a) What is the basic architecture of microprogrammed control unit? Explain. 7
b) How are microinstructions sequenced? 8
4. a) Instruction pipelining increases system performance without increasing processor number, explain how? What are pipelining hazards and how can these be removed? 8
b) Divide 13 by 4 using restoring algorithm. 7
5. a) Differentiate between programmed I/O and interrupt driven I/O. How DMA is better than programmed I/O and interrupt driven I/O? 8
b) What is associative memory? Explain. 8
6. a) Explain Flynn's Classification. 8
b) Explain different types of hardware and software performance issues in multicore computers. 7
7. Write short notes on any two: 2×5
 - a) RISC
 - b) VHDL code for full adder
 - c) Multithreaded Architecture

LUMBINI ENGINEERING MANAGEMENT AND SCIENCE COLLEGE
FINAL INTERNAL ASSESSMENT

Level: Bachelor

Year: 2025

Programme: Computer/ 4th semester

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time: 3 hrs.

Attempt all the questions.

1.

- a. Determine the following based on given instruction format where the number of bits in each field is specified. [2+2+1+3]

I Field	Opcode Field=8	Register Code Field=7	Address Field=16
---------	----------------	-----------------------	------------------

- i. Memory size and data size of the system.
 - ii. Total number of register used by the system and size of register.
 - iii. Total number of instructions used in the system
 - iv. The address of four consecutive microinstruction in the control memory of 2KB.
- b. Define micro-operation. Explain different types of micro-operation.[2+5]
[OR]

Define control memory. Explain the working of microprogrammed control unit. Differentiate between vertical and horizontal microprogrammed control unit.[1+3+3]

2.

- a. What is the significance of addressing modes? Explain different addressing modes with suitable example.[1+6]
- b. Write the structure of VHDL programming and write the VHDL code for full adder using component.[3+5]
- c. A digital computer has a common bus system for 8 registers of 8 bits each. The bus is constructed with multiplexers. [2+1+1+3]
 - i. How many selection inputs are there in each multiplexers?
 - ii. What size of multiplexers are needed?

- iii. How many multiplexers are there in the bus system?
- iv. Draw your bus system.

- b. Why CPU registers are necessary? implement the expression $X = (A + B) * (C - \frac{D}{E})$ in [2+2+4]

- i. Single accumulator organized CPU.
- ii. Stack organized CPU.
- iii. Register organized CPU.

4.

- a. How a negative number can be represented? Find the product of $(-12) * (+10)$ using Booth's multiplication algorithm. [2+6]

- b. How parallel processing can be achieved? In a certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i) * (C_i + D_i)$ with stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for $i=1$ to 6. [2+5]

5.

- a. Given a cache memory with access time of 200 ns and RAM with access time of 2000 ns, if the hit ratio is 90%; find the average memory access time. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 1 MB. Find-[3+2+2]

- i. Number of bits in tag
- ii. Tag directory size

- b. Why page replacement is necessary? Consider the following pages references and determine the hit ratio and the pages in the frame at the end of replacement, if there are three frames.

- i. Using FIFO
- ii. Using LRU
- iii. Using Optimal page replacement

Reference pages:- 6, 1, 1, 2, 0, 3, 4, 6, 0, 2, 1, 2, 1, 2, 0, 3, 2, 1, 2, 0.
[2+2+2+2]

6.

- a. DMA overcome the drawbacks of programmed I/O and interrupt driven I/O, clarify the statement. [7]

- b. Define multiprocessor. List the different types of interconnection of multiprocessor and explain any one of it. [2+1+5]

7. Write short note (ANY TWO) [2*5=10]

- a. Multicore organization
- b. I/O interface module
- c. Computer organization vs computer architecture

1900

128x2 256

2x2x2x2x2x2