

Converters

(i) Digital to Analog Converter

(a) Weighted Resistive Network

(b) R-2R Ladder

(a) Weighted Resistive Network :-

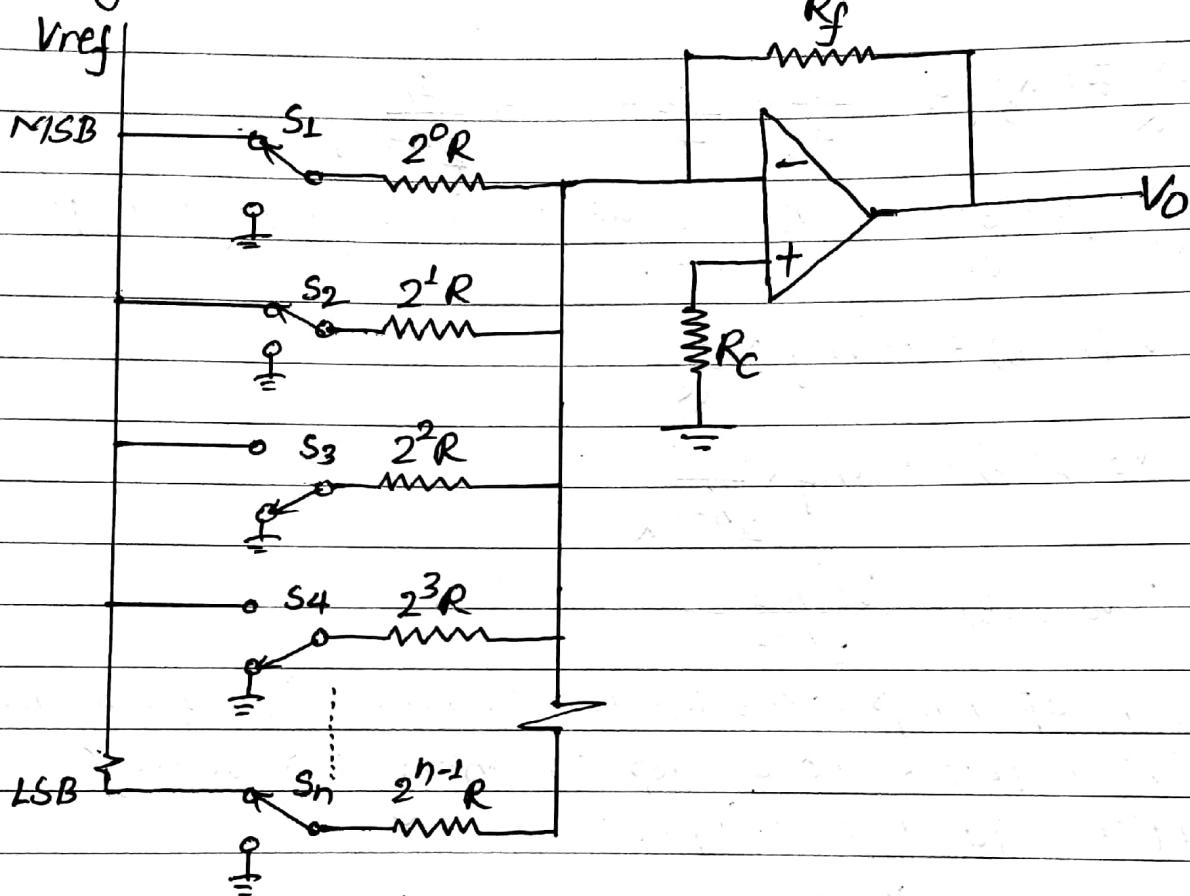


Fig: Weighted Binary Resistance type DAC

The network consists of a set of resistors with different values which represents the binary weights of the i/p bits of the digital codes. The resistor values are weighted inversely as that of the binary weight associated with it. Here, the MSB contains a resistor having lowest value i.e. R so the current thru it is maximum. As we go on from MSB to LSB, the resistance value goes on double in each successive steps i.e. the resistance for LSB is $2^{n-1} R$. The magnitude of current proportional

to the value of each bit in the digital i/p word is generated by the reference voltage.

V_o in the given ckt is given by

$$V_o = -V_{ref} \left[\frac{R_f}{2^0 R} \times S_1 + \frac{R_f}{2^1 R} \times S_2 + \frac{R_f}{2^2 R} \times S_3 + \dots + \frac{R_f}{2^{n-1} R} \times S_n \right]$$

$$= -\frac{V_{ref} \times R_f}{R} \left[S_1 + \frac{S_2}{2} + \frac{S_3}{4} + \dots + \frac{S_n}{2^{n-1}} \right]$$

where $S_1, S_2, S_3, \dots, S_n$ has value '1' for high digital i/p and '0' for low digital i/p.

$$V_o(\text{MSB}) = -V_{ref} \times \frac{R_f}{R}$$

$$V_o(\text{LSB}) = -V_{ref} \times \frac{R_f}{2^{n-1} R}$$

$$\therefore V_o(\text{LSB}) = \frac{V_o(\text{MSB})}{2^{n-1}}$$

Hence, the op-Amp adds up the currents flowing in the resistive network to develop an analog o/p voltage proportional to digital input.

(b) R-2R Ladder type DAC :

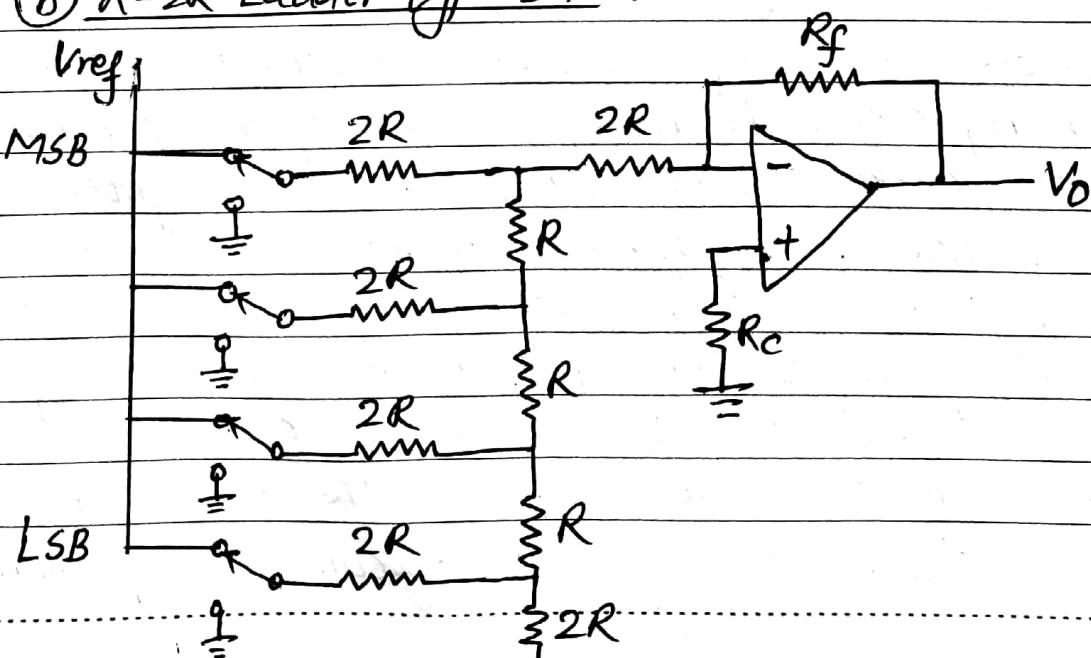
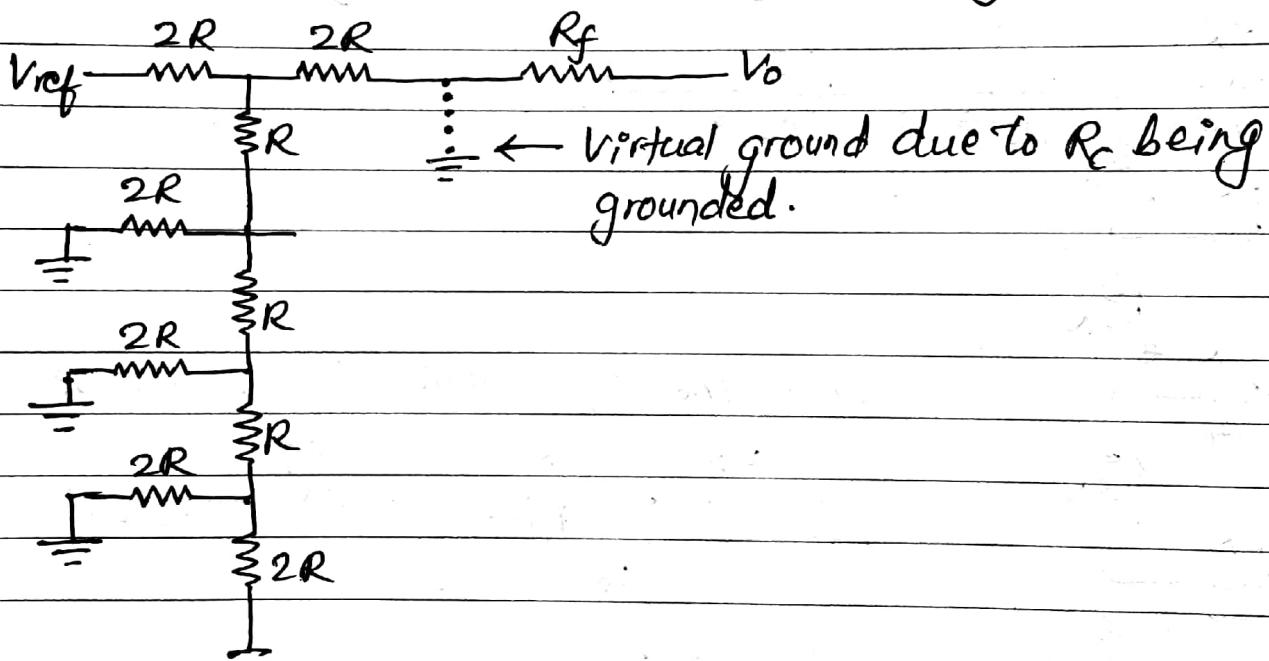


Fig: R-2R ladder DAC (4-bit)

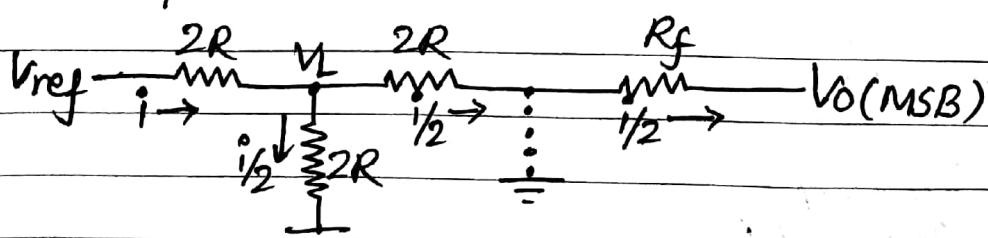
The binary R-2R ladder now largely overcomes the problems of the weighted binary resistive type. It uses only two values of resistances either R or $2R$. This eliminates the problem of requirement of large range of resistors as in case of WBRN. Furthermore, the resistances are arranged in a single chip and they have almost identical characteristics which minimizes the problem of tolerance.

Let us find V_o due to MSB:

In this condition, V_{ref} is applied to MSB and all other branches are connected to the ground as:



The equivalent circuit will be



$$\text{Here, } i = \frac{V_{ref} - V_L}{2R}$$

$$\text{or, } i = \frac{V_{ref} - (\frac{i}{2})2R}{2R}$$

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$$\text{or}, 2Ri = V_{ref} - Ri$$

$$\text{or}, 3Ri = V_{ref}$$

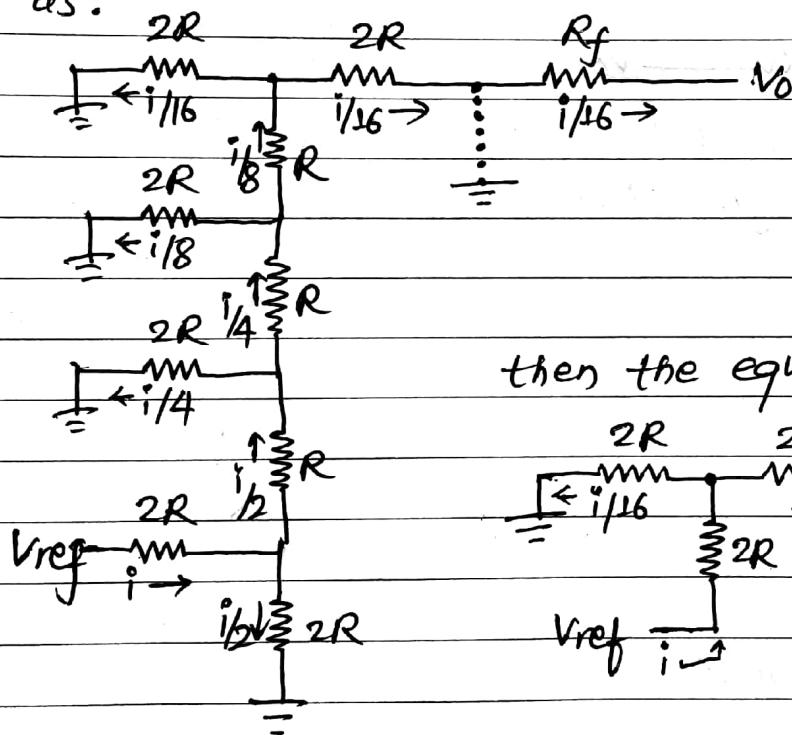
$$\therefore i = \frac{V_{ref}}{3R}$$

$$\text{and } V_o(\text{MSB}) = R_f \times \frac{i}{2}$$

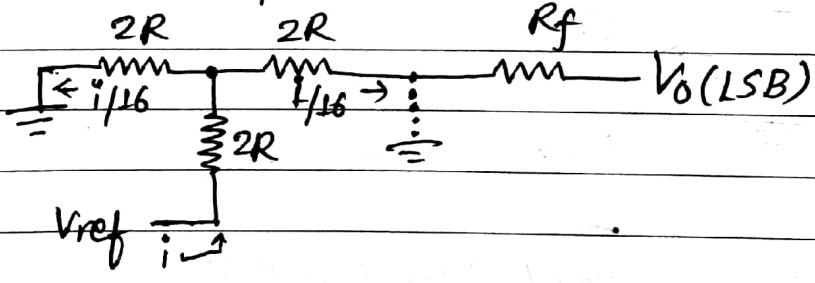
$$= R_f \times \frac{V_{ref}}{6R}$$

$$\therefore V_o(\text{MSB}) = \frac{V_{ref} \times R_f}{6R}$$

Let us consider the case $\text{LSB} = 1$ & others are '0'. In this case we can find o/p voltage due to LSB only. The ckt is as:



then the equivalent circuit will be



$$\text{Now } V_o(\text{LSB}) = \frac{1}{16} \times R_f$$

$$\text{or, } V_o(\text{LSB}) = \frac{V_{ref} \cdot R_f}{48R}$$

Comparing o/p voltage due to MSB & LSB,

$\frac{V_o(\text{MSB})}{V_o(\text{LSB})} = 8$ Here we see that the current flowing through the feedback resistor due to MSB is 8 times the current due to the LSB.

The o/p voltage which is in analog form becomes proportional to the digital i/p and is given by the expression,

$$V_{out} = \left[d_0 \times 2^0 + d_1 \times 2^1 + d_2 \times 2^2 + d_3 \times 2^3 \right] V_{ref}$$

$$\therefore V_{out} = \frac{V_{ref}}{2^4} [d_0 + 2d_1 + 4d_2 + 8d_3]$$

In general, the above expression can be written as:

$$V_{out} = \frac{V_{ref}}{2^n} [d_0 + 2d_1 + 4d_2 + 8d_3 + \dots + 2^{n-1}d_{n-1}]$$

Here, voltage step or voltage resolution = $\frac{V_{ref}}{2^n}$

(ii) Analog to Digital Converters

① Stair Case Ramp type ADC

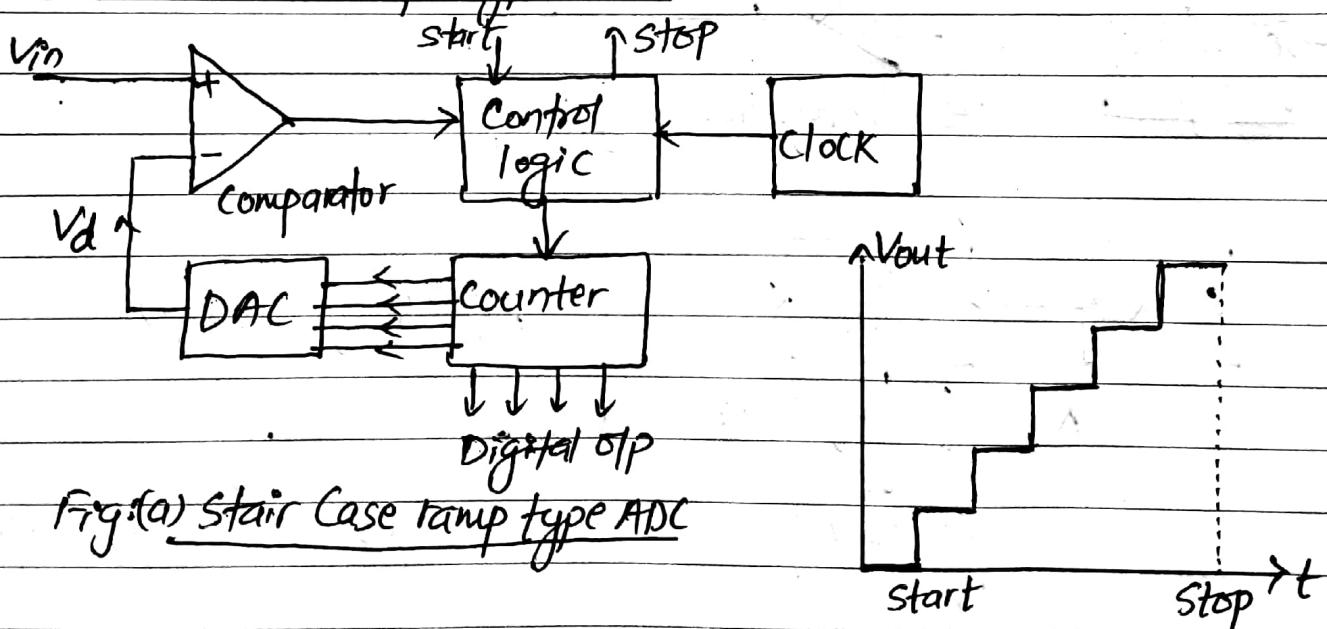


Fig.(a) Stair Case ramp type ADC

∴ when a start command is issued to the control logic, the analog i/p voltage is compared to a voltage o/p of DAC. The o/p of DAC begins at zero and is increased by one LSB increment with

Fig(b)

each pulse of the clock as shown in fig(b). As long as V_{in} is greater than o/p voltage of the DAC, the comparator produces an o/p signal that continues to allow the clock pulses to be fed to the counter. When the o/p voltage of DAC exceeds the V_{in} , the comparator o/p changes & this action stops the clock pulses from reaching the counter. The counter state at that time represents the value of V_{in} in digital form.

The drawback of this converter type is that inspite of its simplicity, it is quite slow and the conversion time depends on the amplitude of V_{in} .

(b) Dual Slope ADC :-

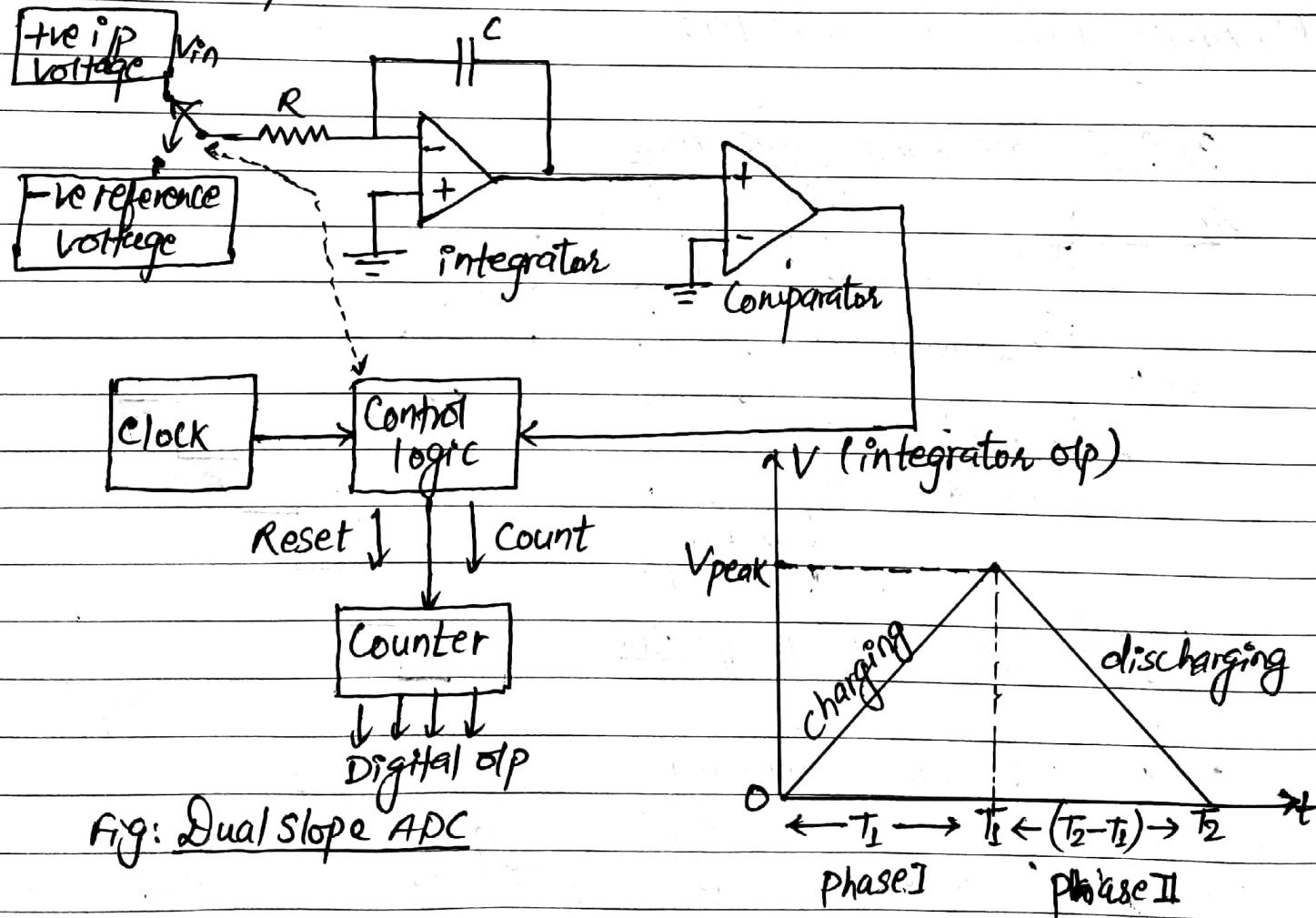


Fig: Dual Slope ADC

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1st integration:

$$\frac{V_{peak}}{T_1} = \frac{V_{in}}{RC}$$

2nd integration,

$$\frac{V_{peak}}{T_2 - T_1} = \frac{V_{ref}}{RC}$$

$$\text{or, } (T_2 - T_1) = \frac{V_{peak} \times RC}{V_{ref}}$$

$$\text{or, } (T_2 - T_1) = \frac{V_{peak}}{V_{ref}} \times T_1$$

$$\therefore (T_2 - T_1) \propto V_{peak}$$

and $V_{peak} \propto V_{in}$ andhence $(T_2 - T_1) \propto V_{in}$

→ The reference voltage and the i/p analog voltage are sequentially connected to the integrator with the help of a switch.

→ The reference voltage and the analog voltage must be of opposite polarity.

→ The i/p voltage is integrated for a fixed i/p sample time.

→ The integrated value is then discharged at a fixed rate & the time to do this is measured by a counter.

→ When a convert command is received by the counter, it automatically resets to all zeros & the switch connects the i/p voltage to the integrator.

→ The o/p from the comparator is designed such that at this time it will permit the counter to count up for an op from the integrator will be steadily increasing in value.

→ The state of counter for $(T_2 - T_1)$ time is the digital o/p of V_{in} provided because slope $\propto V_{peak} \propto V_{in} \propto (T_2 - T_1)$.

① Successive Approximation type ADC :-

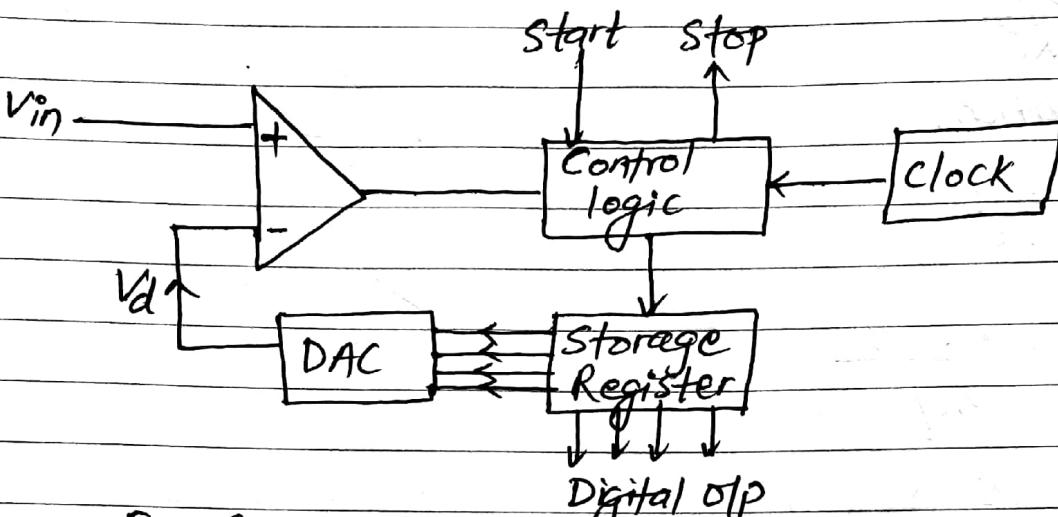


Fig: Successive approximation type ADC

These are very widely applied because of their combination of high resolution and speed (i.e. they can perform conversion within 1 to 50 μ s rather than the milliseconds required by staircase ramp type & dual slope).

When start of conversion goes high, the register is cleared i.e. all the bits are set to zero and V_d drops to zero.

This V_d goes to the comparator and is compared to V_{in} .

Obviously, this $V_d = 0$ is less than V_{in} , so the comparator o/p goes high so that the clock pulse is given to the register. During the first clock pulse, the control logic circuit loads a high MSB into the register (for eg 1000 for 4-bit ADC).

This digital data is converted to analog by DAC. If this analog value is more than V_{in} , the low o/p of comparator

signals the control logic to reset the MSB to 0 & set the next bit to MSB to '1'. On the other hand,

if $V_{in} > V_d$, then the high o/p of comparator indicates the MSB to remain at '1' & also set next bit to MSB to '1'. This process continues till all bits are tested.

After 'n' bits, the storage register will contain all those bits stored as '1' or '0' and the total contents will be a digital approximation of the analog i/p voltage signal.

* Start \uparrow , Register \rightarrow cleared

$V_d = 0$, V_{in} always $> V_d$, so comparator o/p = high, the CLK is given to the register.

* During first CLK;

MSB = 1, rest ~~bit~~ bit = 0

This data is converted to analog by DAC & compared to V_{in} .

* if $V_{in} > V_d \rightarrow$ o/p of comparator is high, which signals the MSB remains '1' & set next to MSB to '1'

* if $V_{in} < V_d \rightarrow$ the low o/p of comparator signals: reset the MSB to 0 & set next bit to MSB to '1'.

\rightarrow this process continues till all bits are tested.

\rightarrow the content of storage register is the digital o/p of the i/p voltage.

⑧ Digitize 9.2V using successive approximation type ADC.
Show all the steps in tabular form.

\Rightarrow	Storage Register Value		Comparator o/p	Value stored after comparison
	S.N	Initial		
1.	0000	1000	$V_{in} > V_d$, o/p = 1	1000
2.	1000	1100	$V_{in} < V_d$, o/p = 0	1000
3.	1000	1010	$V_{in} < V_d$, o/p = 0	1000
4.	1000	1001	$V_{in} > V_d$, o/p = 1	1001

(d) Flash type ADC (or Parallel ADC)

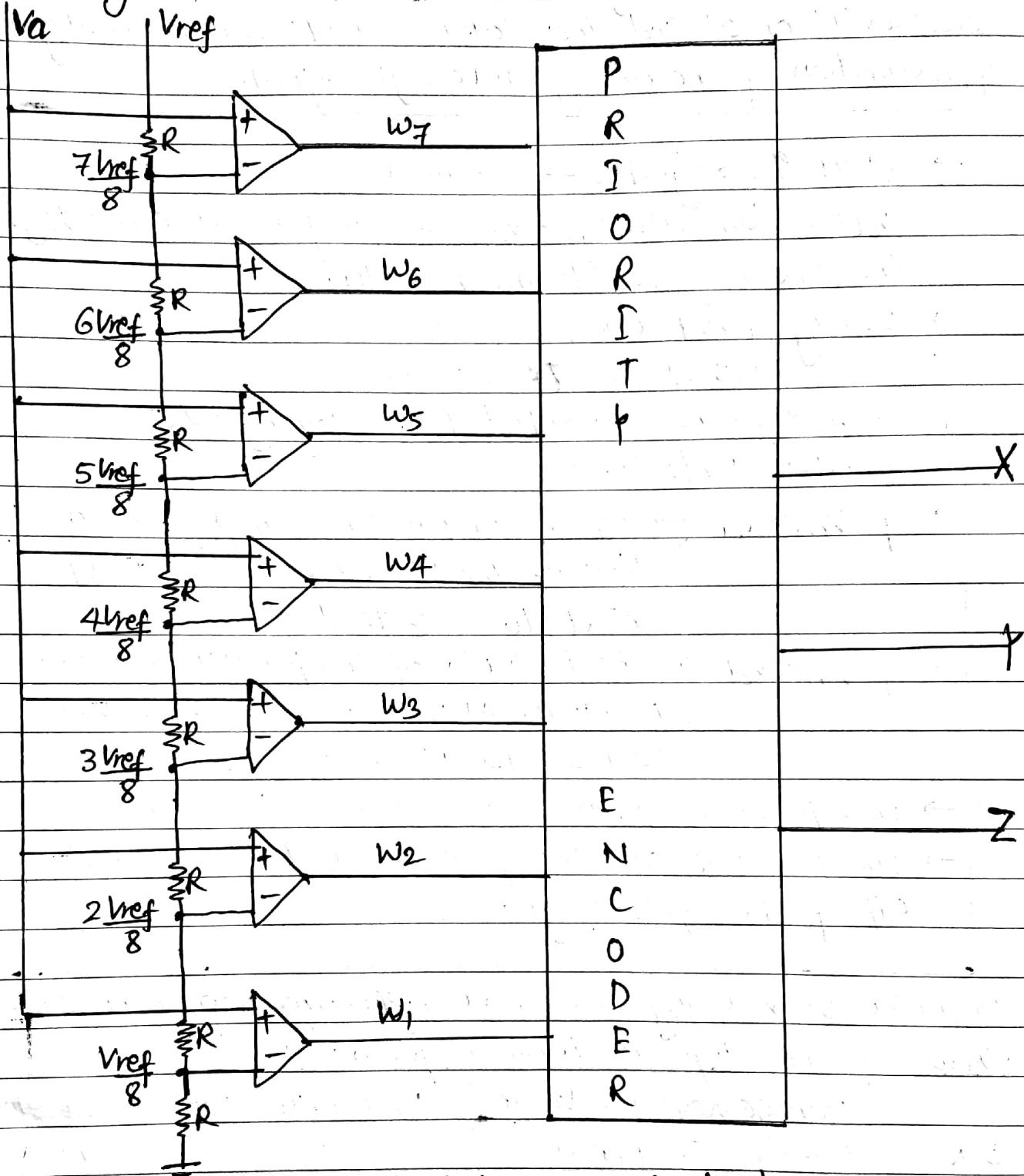


Fig: A flash type ADC (3-bit)

For an n -bit converter, $(2^n - 1)$ separate voltage comparators are used. Each comparator has the i/p analog voltage. A reference voltage is applied to a ladder of resistance so that a reference voltage applied to each comparator is one bit higher size than

than the reference voltage applied to the lower previous comparators. When analog voltage is applied, all these comparators for which the analog voltage (V_a) is greater than the reference voltage (V_{ref}) will go high and those for which the analog voltage is less than the reference voltage will go low. The resulting O/P of the comparators are fed to the priority encoder which translates them into digital O/P . Because all the bits of the O/P digital word are simultaneously produced, a complete conversion can be obtained within one clock and hence is fast.

~~Diagram~~
The operation of encoder is as

$$V_{ref} = V_a + 2.0 \text{ or } 2.5V$$

I/P of Encoder	O/P
w ₇ w ₆ w ₅ w ₄ w ₃ w ₂ w ₁	x y z
0 0 0 0 0 0 0	0 0 0
0 0 0 0 0 0 1	0 0 1
0 0 0 0 0 1 1	0 1 0
0 0 0 0 1 1 1	0 1 1
0 0 0 1 1 1 1	1 0 0
0 0 1 1 1 1 1	1 0 1
0 1 1 1 1 1 1	1 1 0
1 1 1 1 1 1 1	1 1 1

Advantage: requires only one clock cycle.

Disadvantage: Hardware complexity
Power consumption high.