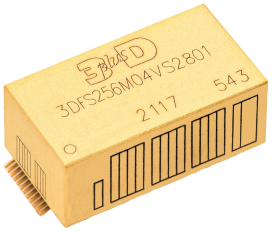
QSPI NOR FLASH

256 Mbit QSPI TMR NOR Flash

3DFS256M04VS2801

Datasheet

PRODUCT OVERVIEW



The 3DFS256M04VS2801 is a 256 Mbit QSPI NOR Flash embedding an ASIC, a power management block and triplicated NOR Flash memories.

This latch-up immune memory is radiation hardened by design with a protection against potential SEE ensured by TMR mitigation electronics, and an enhanced TID performance controlled by an embedded power on/off switch.

In addition, an ECC flag is present to help the user with error (SEE) management. These features provide the user to improve the functional performance and to extend the lifetime of the module in radiation environments.

The 3DFS256M04VS2801 also provides two distinct QSPI user buses. It allows the module to be updated/reconfigured in flight by another device and thus to enhance its fault tolerance.

APPLICATIONS

- FPGA (e.g.: V5Q, KU060) configuration bitstream,
- Boot code storage for microcontrollers and microprocessors

KEY BENEFITS

- Intelligent memory
- Plug and play solution
- Area saving
- Radiation guarantee

KEY FEATURES

PERFORMANCES

- 256 Mbit density
- Single supply voltage: 3.3 V
- Supports standard SPI, Dual, QSPI modes
- **Supports only 16 bits word access (read and write) at even address**
- Two QSPI user buses
- Up to 50 MHz in Fast Read Mode
- 100,000 + erase/program cycles
- More than 20 year data retention
- Low Instruction Overhead Operations
- Continuous Read 8-byte burst
- Available Temperature Range: 0°C to +70°C, -40°C to +85°C, -55°C to +105°C
- Package: SOP 24 -0.65mm pitch
- ITAR free
- Radiation Effect/Data integrity failure notification bit (ECC_Flag)
- Qualified for Space Applications

SPACE QUALIFICATION

- Qualified with 3D PLUS ESA certification per ESCC 2566001,
- Up to NASA Level 1,
- High Longevity and Reliability,
- Flight heritage : 3D PLUS expertise in space memories for more than 20 years

RADIATION TOLERANCE

- TID > 40 krad(Si) (off)
- SEL LET > 62.5 MeV.cm²/mg
- SEE immune, mitigated by design

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1. DOCUMENTS

1.1 APPLICABLE DOCUMENTS

[AD1] **3DPA-8204:** Detail Specification 256 Mbit TMR QSPI Flash NOR P/N: 3DFS256M04VS2801
[AD2] **3300-1300:** Manual Assembly Recommendations
[AD3] **3300-1301:** Automatic Assembly Recommendations
[AD4] **3000-1350**: Pinout P/N : 3DFS256M04VS2801
[AD5] **3250-0107**: Footprint
[AD6] **3200-3732**: Step file
[AD7] **3641**-0841 : Recommendations for underfill

1.2 REFERENCE DOCUMENTS

[RD1] 3DFS256M04VS2801_IBIS: IBIS Model

[RD2] FlashNor_3DFS256: RTL Model

1.3 ACRONYMS

ASIC	Application Specific Integrated Circuit	**SET**	Single Event Transient
ECC	Error Correcting Code	**SEU**	Single Event Upset
ESD	ElectroStatic Discharge	**SPI**	Serial Peripheral Interface
FPGA	Field Programmable Gate Array	**SI**	Signal Input
HBM	Human Body Model	**SO**	Signal Output
I/O	Input/Output	**TBC**	To Be Characterized
NOR	Not OR	**TID**	Total Ionizing Dose
QSPI	Quad SPI	**TMR**	Triple Modular Redundancy
SEE	Single Event Effect		
SEL	Single Event Latch up		

2. GENERAL DESCRIPTION

2.1 INTRODUCTION

The 3DFS256M04VS2801 is a 256 Mbit QSPI NOR Flash memory. The module embeds NOR QSPI memories, a power management block and an ASIC

- The three 256 Mbit QSPI NOR Flash memories are used for data storage. Each 256 Mbit memory is made with 2 banks of 128 Mbit. In this module, the user cannot access a single 128 Mbit memory bank.
- The power management block is used to control the supply voltage of the QSPI NOR Flash, through the PWR_EN_N pin. Thus, the user can power off the memories when they are unused while still supplying the module with a V_{CC} voltage. This feature allows the user to achieve higher TID performance. If the PWR_EN_N always active, the QSPI NOR Flash memories can achieve 15 Krad (Si). If they QSPI NOR Flash memories are off, the module can meet a TID up to 40 krad (Si).
- The ASIC provides a bridge between the QSPI buses and the QSPI NOR Flash memories. The ASIC includes a Triple Modular Redundancy (TMR) majority voting function to ensure SEU immunity. It integrates transceivers connecting the memories and two distinct QSPI interfaces.

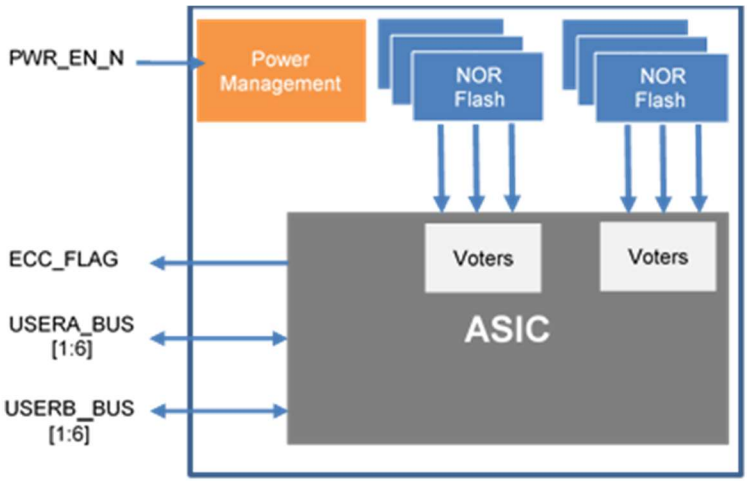

Figure 1: 3DFS256M04VS2801 block diagram

2.2 TYPE VARIANTS

Quality grades of the module are given in Table 1 below:

VARIANT- PART NUMBER	OPERATING TEMP. RANGE	GRADE	CASE	LEAD MATERIALS AND FINISH
3DFS256M04VS2804 IB	-40°C to +85°C	Industrial	SOP 24 pins- 0.65 mm pitch- package CB2	Kovar Ni-Au plating
3DFS256M04VS2801 IS	-40°C to +85°C	Space	SOP 24 pins- 0.65 mm pitch- package CB2	Kovar Ni-Au plating
3DFS256M04VS2801 SS	-55°C to +105°C	Space	SOP 24 pins- 0.65 mm pitch- package CB2	Kovar Ni-Au plating

Table 1: 3DFS256M04VS2801 type variants

2.3 PIN DESCRIPTION

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
1	GND	13	GND
2	USERA_SCK	14	ECC_FLAG
3	USERA_CE_N	15	VCC
4	VCC	16	USERB_IO3
5	USERA_IO0	17	USERB_IO2
6	USERA_IO1	18	GND
7	GND	19	USERB_IO1
8	USERA_IO2	20	USERB_IO0
9	USERA_IO3	21	VCC
10	VCC	22	USERB_SCK
11	PWR_EN_N	23	USERB_CE_N
12	GND	24	GND

Table 2: Pinout

Table 3: Pin list description hereafter gives a description of each signal

SIGNAL NAME	DESCRIPTION	COMMENTS
USERy_CE_N(1)	Chip Enable	Enable or disable all memories in the module. Active Low.
PWR_EN_N	Power Enable	When PWR_EN_N is low, the QSPI NOR Flash memories are powered with V_{CC} and the various data and commands are transmitted to the memories selected with CE_N pin. When PWR_EN_N is high, the supply of the powered memories is cut-off, and their input are in High-Z state
ECC_FLAG	Radiation failure notification	Output
USERy_IO0(1)	Data Input used to write to the device on the rising edge of the clock (SCK).	USERy_IO0 is a bidirectional IO to write instructions, addresses or data to the device on the rising edge of the clock and read data or status from the device on the falling edge of SCK. In Quad SPI, USERy_IO1 is only an output.
USERy_IO1(1)	Data Output used to read data or status of the device on the falling edge of SCK	
USERy_IO2(1) (WP#)	Data Input/Output	The WP# pin is used in conjunction with SRWD bit to protect the Status Register. For more details, please refer to section 5.3.1 In Quad SPI mode (QE bit set at “1”), this pin is used as USERy_IO2.
USERy_IO3(1) (HOLD#)	Data Input/Output	The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and USERy_CE_N is low, the USERy_IO1 pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. In Quad SPI mode (QE bit set at “1”), this pin is used as USERy_IO3.
USERy_SCK(1)	Synchronized clock	
VCC(2)	Voltage Supply	
GND(2)	Ground	

Table 3: Pin list description

Note 1: USER_BUS = [CE_N, SCK, IO0, IO1, IO2, IO3]

Note 2: There are already decoupling capacitors inside the module. Therefore, we recommend to add additional decoupling capacitors between VCC and GND We recommend 1 x 0.1 µF 0402 X7R dielectric ceramic capacitors per V_{CC} pin

2.4 THE TWO QSPI USER INTERFACES

The 3DFS256M04VS2801 is a 256 Mb SPI NOR Flash embedding an ASIC. The pin list is similar as a standard NOR SPI Flash except for:

- PWR_EN_N pin for power management
- ECC_FLAG pin for error management and monitoring
- Two SPI buses interfaces instead of a single bus. Each SPI bus includes: [CE_N,SCK, IO0, IO1, IO2, IO3]

2.4.1 Using only one SPI bus

When using only one of the SPI bus,

- Use USERB interface (it has priority over USERA interface)
- USERA_CE_N shall be tied to V_{CC} through a pull-up resistor (typically 10k), thus interface A will be disabled
- All other pins tied to GND through a pull-down resistor (typically 10k resistor).

Once USERA_CE_N is set HIGH, instruction sent through other bits of USERA interface will never be transmitted to the memories. Thus, it is better to ground them for power consumption reduction.

2.4.2 Using both SPI bus

The two SPI buses allow access to the memory module by up to two distinct users for example an FPGA and a microprocessor as shown in Figure 2. Memory access by two distinct users shall be managed through the USERy_CE_N pin. Only one of the CE_N pin shall be activated (set low) at time. We recommend connecting one of the USERy_CE_N pin as an input of the second memory user. In the illustration below, USERB_CE_N is an input of USERA also.

Assuming USERA_CE_N is activated prior to CE_N_B activation, USERA will have the priority to interact with the memory. Any command sent through USER_B interface will be ignored until USERA_CE_N is deactivated. First user accessing (USERy_CE_N low) the memory has priority over the other one.

Assuming both USERy_CE_N are set low at the same time. Then USERB has priority over USERA (decision is internally made by the memory module). All commands, data, address … sent through USERA interface are irrelevant until USERB_CE_N is set high.

Note: y denotes A or B

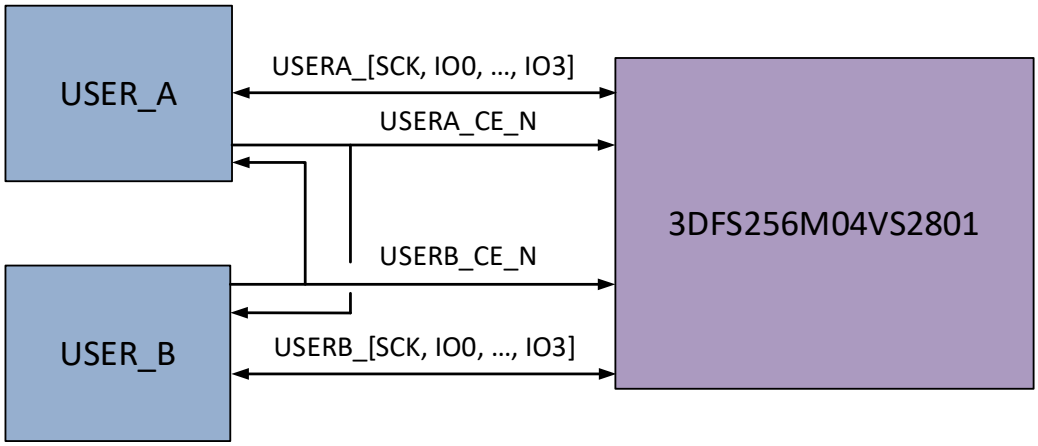

Figure 2: How to use both QSPI interfaces

2.5 RADIATION PERFORMANCES

The radiation tolerant space grade 3DFS256M04VS2801 is suitable for use in space applications with the following TID and SEE characteristics:

PARAMETERS	DESCRIPTIONS	
Total Dose Radiation (TID)	PWR_EN_N = “1”	> 40 krad (Si)
	PWR_EN_N = “0”	> 15 krad (Si)
Single Event Latchup (SEL)	V_{CC} = 3.6 V	> 62.5 MeV.cm^2/mg
Single Event Effect	Immune, mitigated by design	

Table 4: Radiation performances

3. FLASH OPERATIONS

Here is the list of NOR Flash commands supported by the memory module

SPI COMMAND	OPCODE
Write status register	01h
Page Program	02h
Read Page	03h
Write disable	04h
Read status register	05h
Write enable	06h
Fast Read	0Bh
Fast Read, 32-bit address	0Ch
Page Program 32 bits	12h
Read 32 bits	13h
Exit 4 bytes mode	29h/E9h
Quad Page Program	32h
Quad Page Program 32 bits	34h
Dual Output Fast Read	3Bh
Dual Output Fast Read, 32-bit address	3Ch
Reset enable	66h
Quad Output Fast Read	6Bh
Quad Output Fast Read, 32-bit address	6Ch
Reset	99h
Read JEDEC ID	9Fh
Enter 4 bytes mode	B7h
Chip Erase	C7h/60h
Block Erase	D8h
Block Erase 32 bits	DCh

Table 5: SPI commands supported

The 3DFS256M04VS2801 module only supports 16 bits word access (read and write) at even address except for commands on status register (01h and 05h).

3.1 MODE 0 (0, 0) AND MODE 3 (1, 1)

The NOR Flash supports two SPI modes: Mode 0 (0, 0) and Mode 3 (1, 1). The difference between these two modes is the clock polarity. The serial clock is idle at “0” (SCK=0) for Mode 0 and the clock is idle at “1” (SCK =1) for Mode 3. Please refer toFigure 3 below for SPI

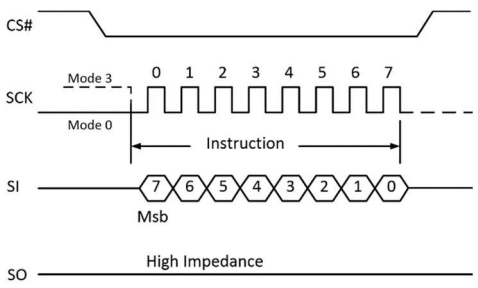

Figure 3: Mode 0 and Mode 3 in SPI mode

3.2 READ OPERATIONS

3.2.1 Read Page (03h) and Read Page 32 bits (13h)

The Read Page (NORD) instruction is used to read memory contents of the device at a maximum frequency of 20 MHz.

The instruction is transmitted via the SI line

- 03h is followed by a 3-byte address (A23-A0),or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 13h is followed by a 4-byte address (A31-A0)

Then the memory contents, at the address given, are shifted out on SO. The address can start at any even address location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

The read operation can be terminated at any time by driving CE_N (CS#) high (V_{IH}) after the data comes out.

It is prohibited to issue a Read Page instruction while an Erase, Program or Write operation is in process (BUSY = 1).

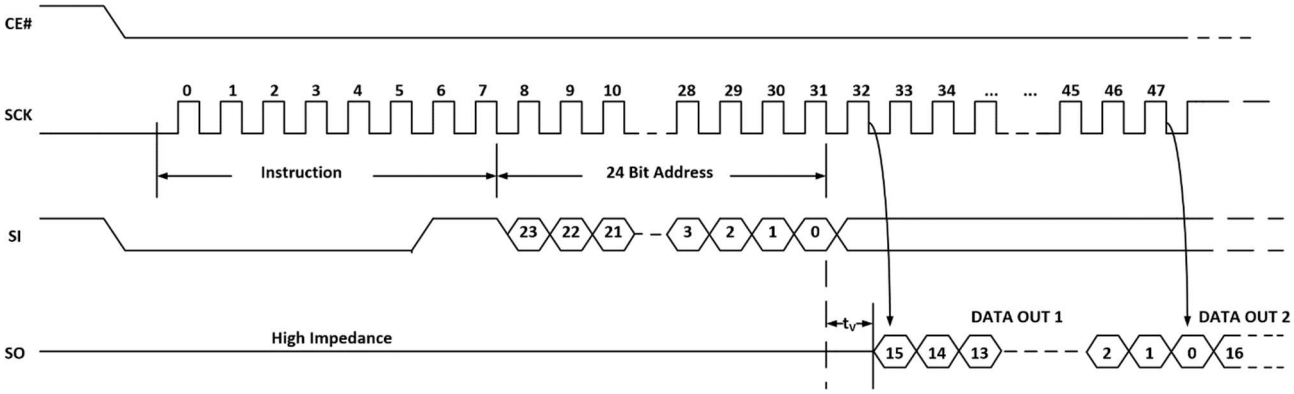

Figure 4: Read Page sequence (03h)

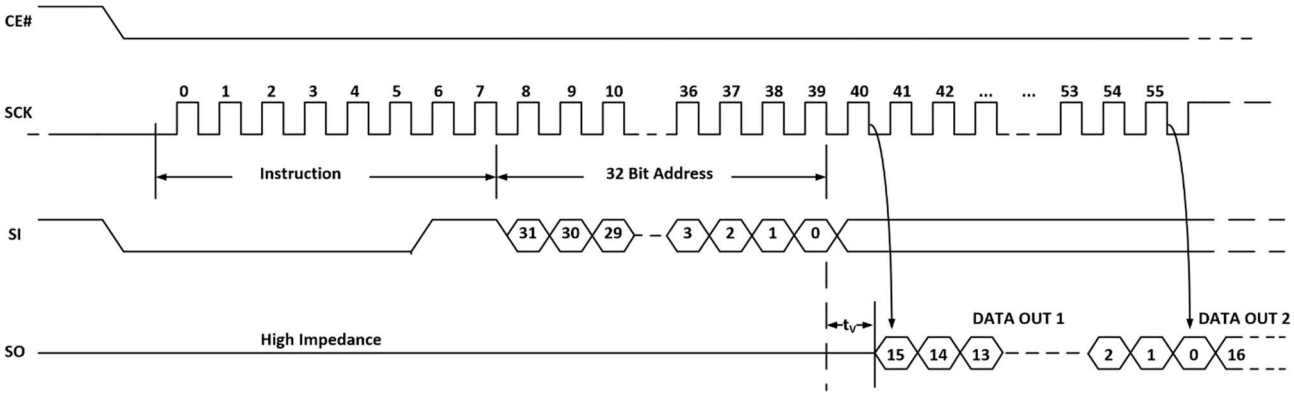

Figure 5: Read Page 32 bits sequence (13h)

3.2.2 Fast Read (0Bh) and Fast Read 32 bits (0Ch)

The Fast Read (FRD) instruction is used to read memory data up to 50 MHz clock. The instruction is transmitted via the SI line

- 0Bh is followed by a 3-byte address (A23-A0) or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 0Ch is followed by a 4-byte address (A31-A0)

The address is followed by ten dummy cycles. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on SO is “don’t care” and must be high impedance. Then the memory contents, at the address given, are shifted out on SO. The address can start at any even address location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

The FAST READ instruction is terminated by driving CE_N (CS#) high (V_{IH}).

It is prohibited to issue a Fast Read instruction while an Erase, Program or Write cycle is in process.

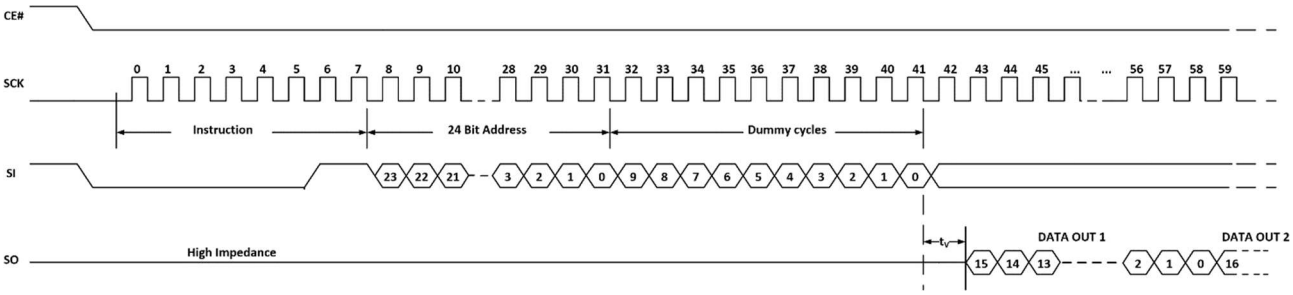

Figure 6: Fast Read sequence (0Bh)

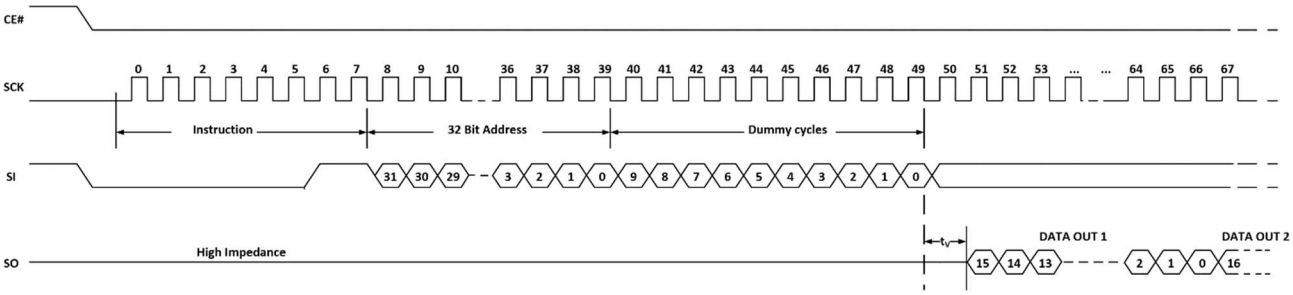

Figure 7: Fast Read 32 bits sequence (0Ch)

3.2.3 Dual Output Fast Read (3Bh) and Dual Output Fast Read 32 bits (3Ch)

The Dual Output Fast Read (FRDO) instruction is used to read memory data on two output pins each at up to a 50 MHz clock. The instruction

- 3Bh is followed by a 3-byte address (A23-A0) or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 3Ch is followed by a 4-byte address (A31-A0)

Then the memory contents, at the address given, is shifted out two bits at a time through IO0 (SI) and IO1 (SO). Two bits are shifted out at the SCK frequency by the falling edge of the SCK signal. For Dual Output

Read commands, there are ten dummy cycles required after the last address bit is shifted into SI before data begins shifting out of IO0 and IO1. During the dummy cycles, the data value on SI is a “don’t care” and may be high impedance. The address can start at any even address location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

The FRDO instruction is terminated by driving CE_N (CE#) high (V_{IH}).

It is prohibited to issue a FRDO instruction while an Erase, Program or Write cycle is in process (BUSY=1).

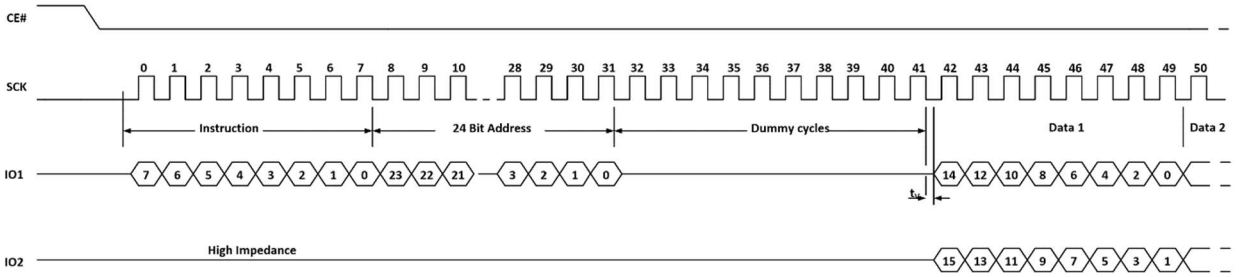

Figure 8: Dual Output Fast Read sequence (3Bh)

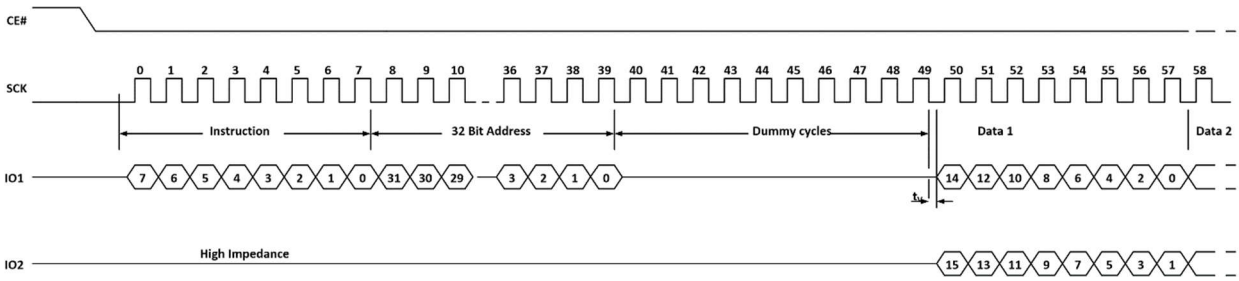

Figure 9: Dual Output Fast Read 32 bits sequence (3Ch)

3.2.4 Quad Output Fast Read (6Bh) and Quad Output Fast Read 32 bits (6Ch)

The Quad Output Fast Read (FRQO) instruction is used to read memory data on four output pins each at up to a 50 MHz clock.

A Quad Enable (QE) bit of Status Register must be set to "1" before sending the Fast Read Quad Output instruction. The instruction

- 6Bh is followed by a 3-byte address (A23-A0) or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 6Ch is followed by a 4-byte address (A31-A0).

Then the memory contents, at the address given, is shifted out four bits at a time through IO0-IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal. For Quad Output Read Mode, there are ten dummy cycles required after the last address bit is shifted into SI before data begins shifting out of IO0-IO3. This latency period (i.e., dummy cycles) allows the device’s internal circuitry enough time to set up for the initial address. During the dummy cycles, the data value on IO0-IO3 is a “don’t care” and may be high impedance. The address can start at any even address location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

FRQO instruction is terminated by driving CE_N (CE#) high (V_{IH}).

It is prohibited to issue a FRQO instruction while an Erase, Program or Write cycle is in process (BUSY=1).

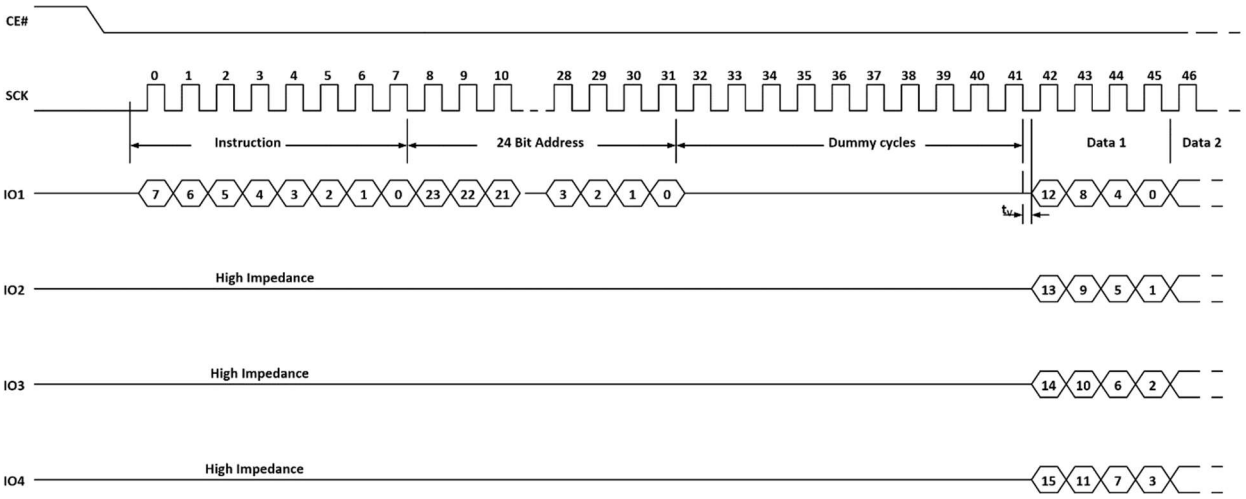

Figure 10: Quad Output Fast Read sequence (6Bh)

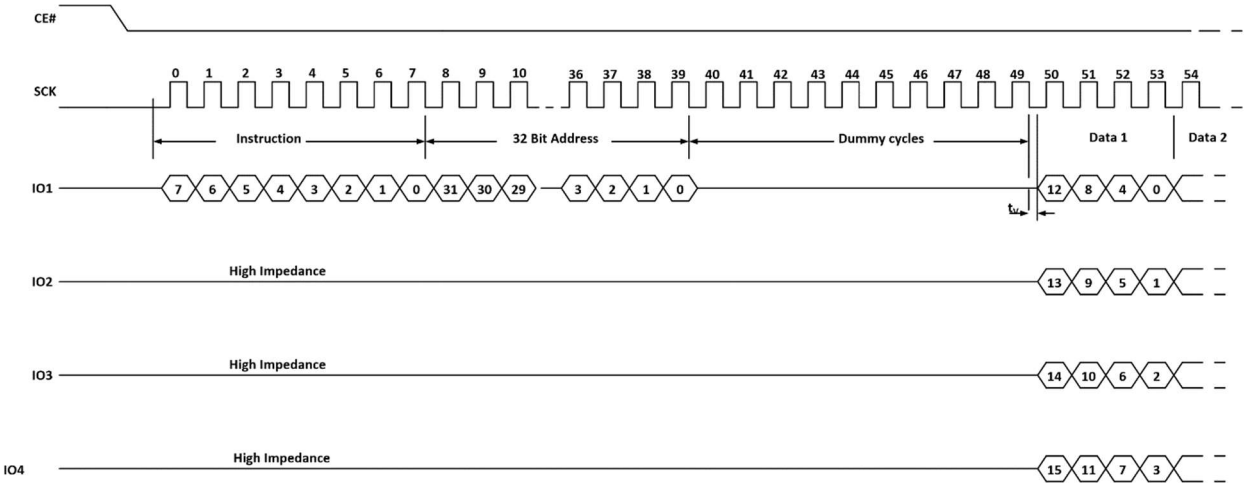

Figure 11: Quad Output Fast Read 32 bits sequence (6Ch)

3.2.5 Read JEDEC ID (9Fh)

The Read JEDEC ID (RDID) instruction allows the user to read the Manufacturer and product ID of devices. After the RDID command (9Fh in SPI mode) is input, the Manufacturer ID is shifted out MSB first followed by the 2-byte electronic ID (ID15-ID0) that indicates Memory Type and Capacity, one bit at a time. Each bit is shifted out during the falling edge of SCK. If CE_N (CS#) stays low after the last bit of the 2-byte electronic ID, the Manufacturer ID and 2-byte electronic ID will loop until CE_N is pulled high.

It is prohibited to issue a RDID command while a program, erase, or write cycle is in progress.

MODULE	DENSITY	JEDEC ID
3DFS256M04VS2801	256 Mbit	0x9D6019

Table 6: Product identification table

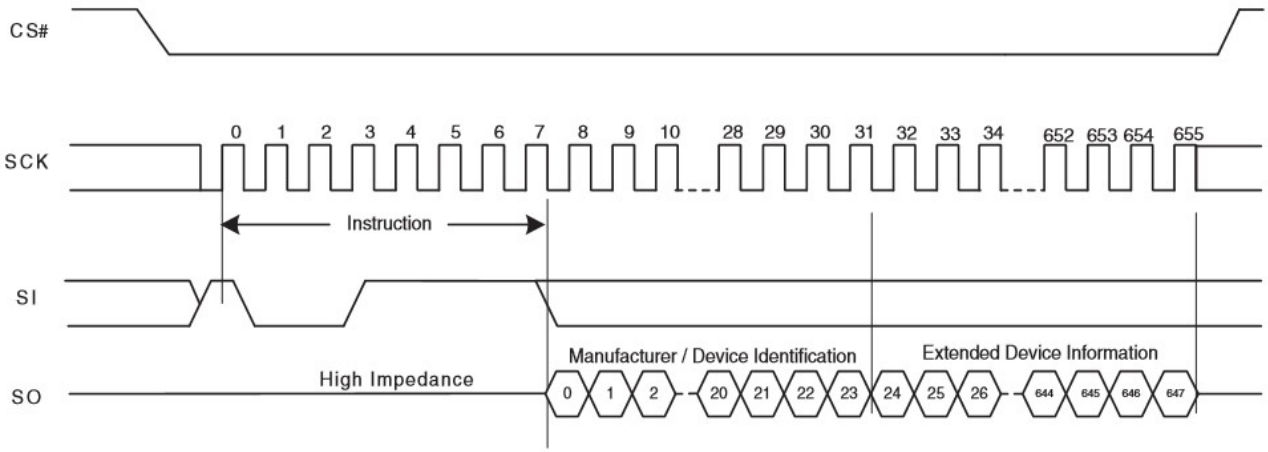

Figure 12: Read JEDEC ID sequence (9Fh)

3.3 PROGRAM OPERATIONS

Programming data requires two commands: Write Enable (WREN), and Page Program (PP or QPP). The Page Program command accepts from 1 byte up to 512 consecutive bytes of data (page) to be programmed in one operation. Programming means that bits can either be left at 1, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

3.3.1 Write Enable (06h)

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit of the Status Register to 1. The WEL bit is reset to the write-protected state after power-up. The WEL bit must be write enabled before any write, program and erase commands. CE_N must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. Without CE_N (CS#) being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI, the write enable operation will not be executed.

The WEL bit will be reset to the write-protected state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

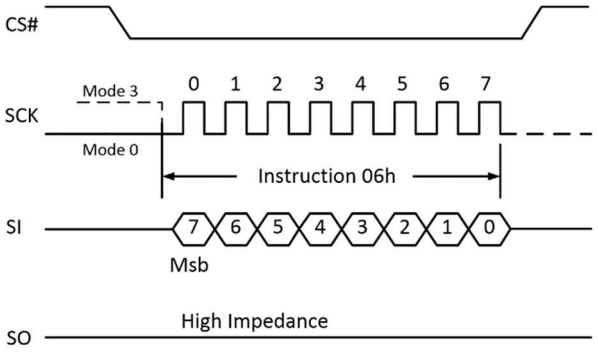

Figure 13: Write Enable sequence (06h)

3.3.2 Write Disable (04h)

The Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction, since the WEL bit is automatically reset.

The user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory can use the WRDI command. The WRDI command is ignored during an embedded operation while

WIP bit =1. CE_N must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI, the write disable operation will not be executed.

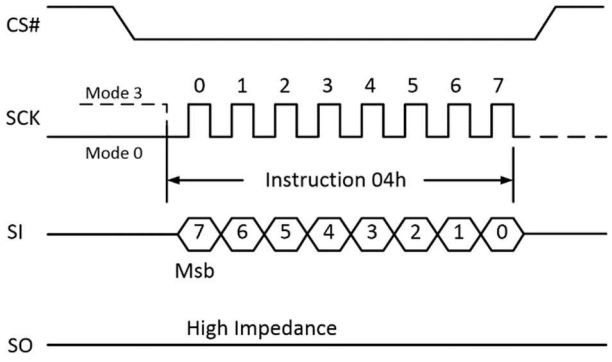

Figure 14: Write Disable sequence (04h)

3.3.3 Page Program (02h) and Page Program 32 bits (12h)

The Page Program (PP) commands allows bytes to be programmed in the memory (changing bits from 1 to 0). Before the Page Program (PP) commands can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A PP instruction which attempts to program into a page that is write-protected will be ignored.

After the Write Enable (WREN) command has been decoded successfully, the device sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The instruction

- 02h is followed by a 3-byte address (A23-A0) or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 12h is followed by a 4-byte address (A31-A0)

and at least one data byte on SI. Up to a page can be provided on SI after the 3-byte address with instruction 02h or 4-byte address with instruction 12h has been provided. If the 9 least significant address bits (A8-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 9 least significant bits (A8-A0) are all zero) i.e. the address wraps within the page aligned address boundaries. This is a result of only requiring the user to enter one single page address to cover the entire page boundary. If less than a page of data is sent to the device, these data bytes will be programmed in sequence, starting at the provided address within the page, without having any affect on the other bytes of the same page. For optimized timings, using the PP command to load the entire page size program buffer within the page boundary will save overall programming time versus loading less than a page size into the program buffer. The programming process is managed by the flash memory device internal control logic.

The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is ‘1’, the program operation is still in progress. If WIP bit is ‘0’, the program operation has completed. During a program operation, all instructions will be ignored except the RDSR instruction

Program operation will start immediately after the CE_N (CS#) is brought high, otherwise the PP instruction will not be executed.

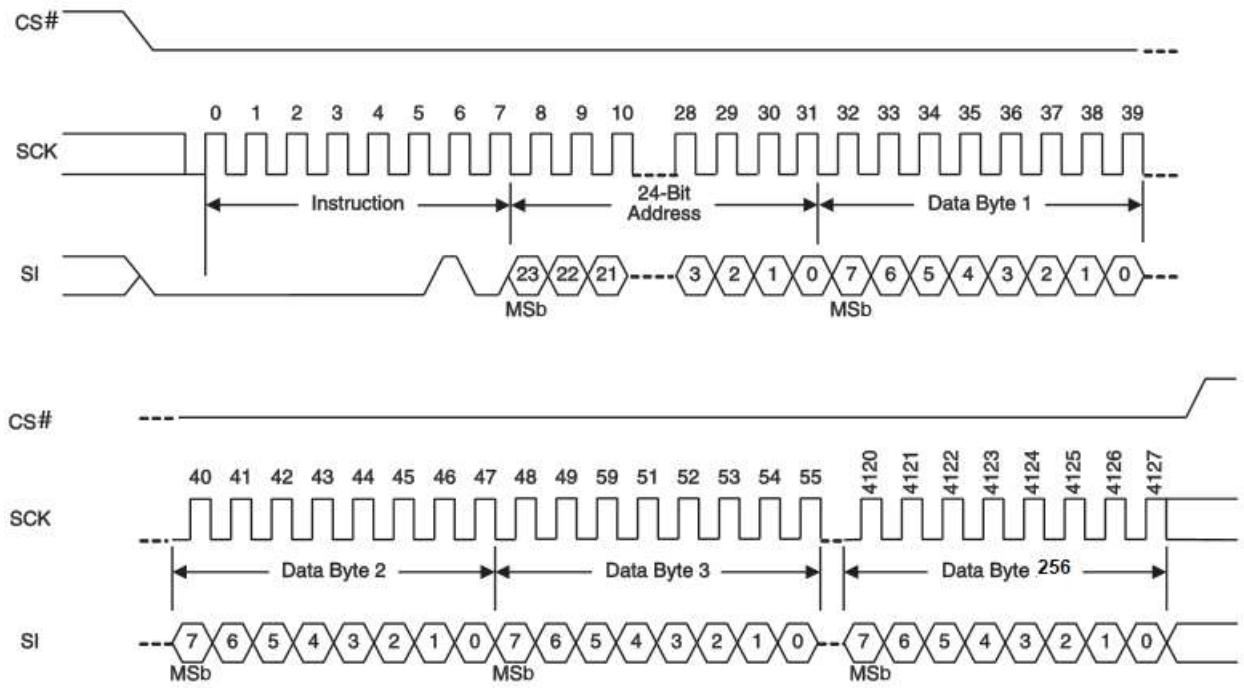

Figure 15: Page Program sequence (02h)

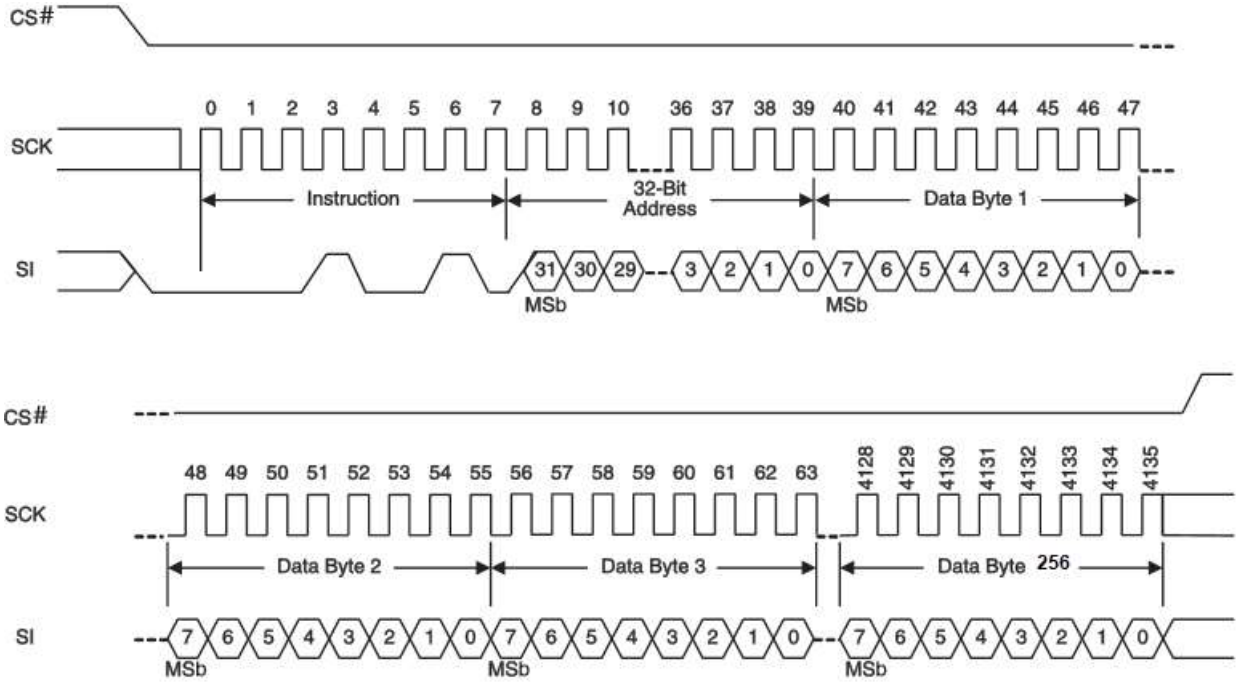

Figure 16: Page Program 32 bits mode sequence (12h)

3.3.4 Quad Page Program (32h) and Quad Page Program 32 bits (34h)

The Quad Page Program (QPP) command allows bytes to be programmed in the memory (changing bits from 1 to 0). The QPP command allows up to a page size of data (512 bytes) to be loaded into the Page Buffer using four signals: IO0-IO3. QPP can improve performance for PROM Programmer and applications that have slower clock speeds (< 12 MHz) by loading 4 bits of data per clock cycle. The QE bit in the Status Register

must be set to “1” and a Write Enable command must be executed before the device will accept the QPP command (WEL=1). The instruction

- 32h is followed by a 3-byte address (A23-A0) or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- 34h is followed by a 4-byte address (A31-A0)

and at least one data byte, into the IO signals. Data must be programmed at previously erased (FFh) memory locations. The programming page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each Page programming operation. All other functions of QPP are identical to Page Program.

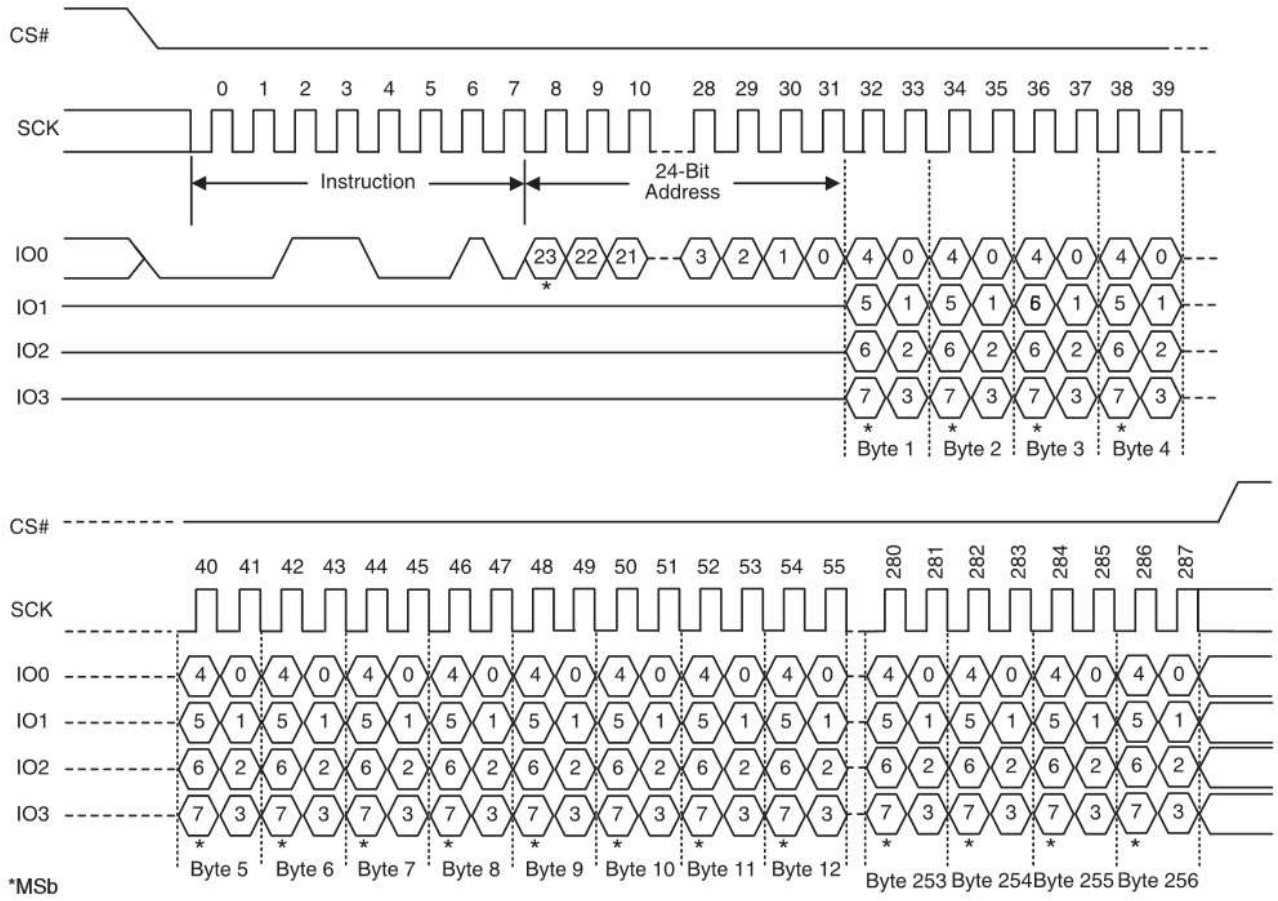

Figure 17: Quad Page Program sequence (32h)

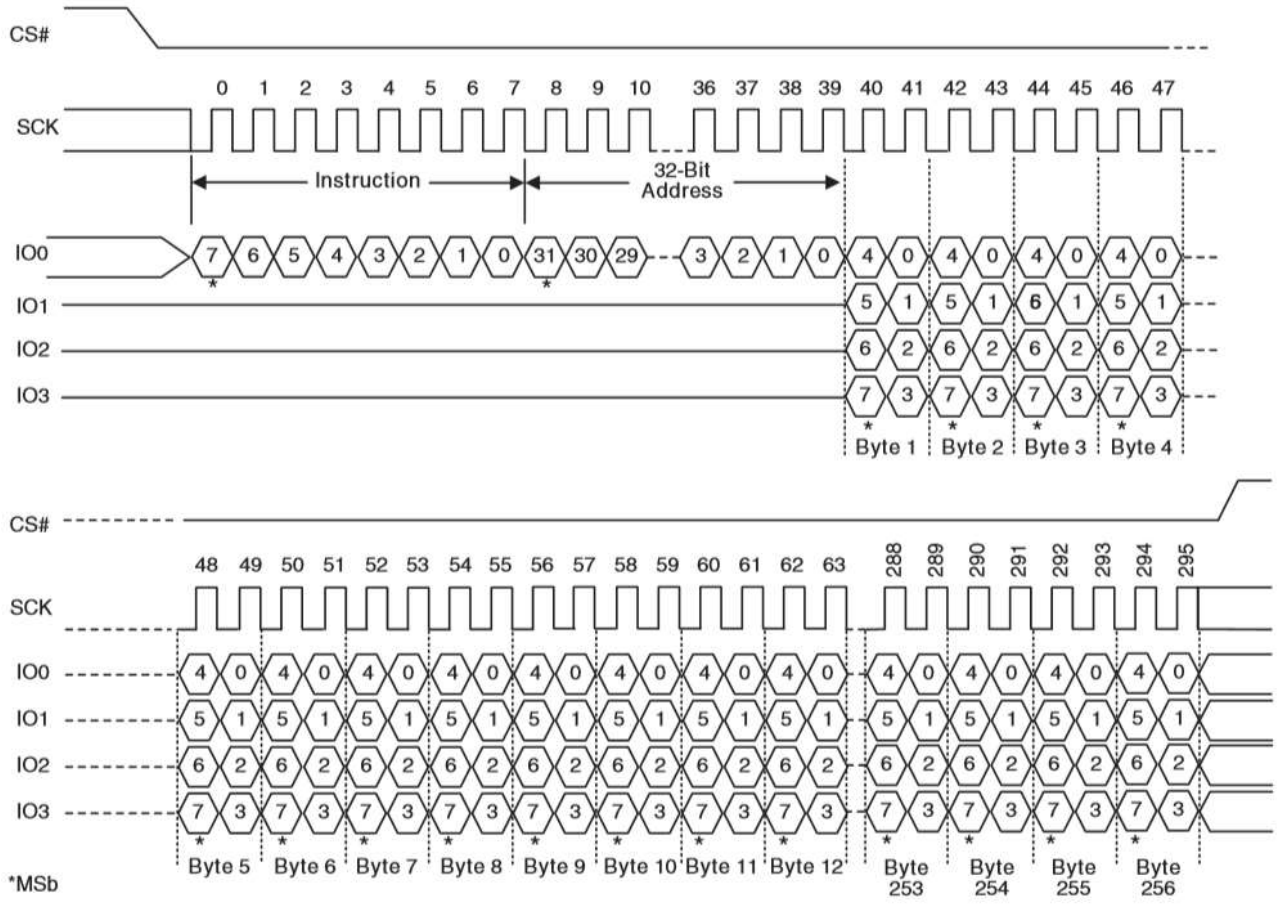

Figure 18: Quad Page Program 32 bits sequence (34h)

3.4 ERASE OPERATIONS

3.4.1 Chip Erase (C7h/60h)

A Chip Erase (CER) instruction erases the entire memory array ((all bytes are FFh). Before the execution of CER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is automatically reset after completion of a chip erase operation.

The CER instruction code is input via the SI. CE_N (CS#) must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the erase cycle, which involves the pre-programming and erase of the entire flash memory array. If CS# is not driven HIGH after the last bit of instruction, the CER operation will not be executed. As soon as CS# is driven into the logic HIGH state, the erase cycle will be initiated. With the erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a 1 when the erase cycle is in progress and a 0 when the erase cycle has been completed.

The internal control logic automatically handles the erase voltage and timing.

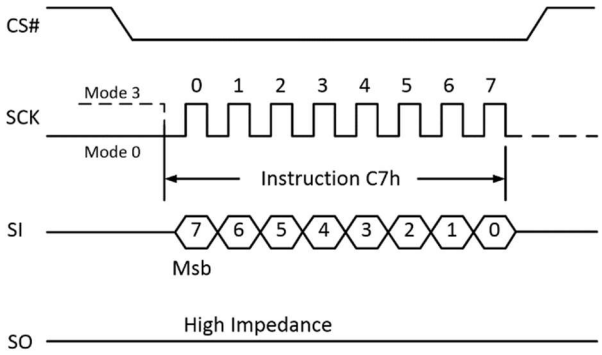

Figure 19: Chip Erase sequence

3.4.2 Block Erase (D8h) and Block Erase 32 bits (DCh)

A Block Erase (BER) instruction erases a 128 Kbyte block. Before the execution of a BER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

The instruction

- D8h is followed by a 3-byte address (A23-A0), or a 4 byte address (A31-A0) when “enter 4 bytes mode” is activated
- DCh is followed by a 4-byte address (A31-A0).

CE_N (CS#) must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of address has been latched in on SI. This will initiate the erase cycle, which involves the pre-programming and erase of the chosen sector. If CE_N is not driven HIGH after the last bit of address, the sector erase operation will not be executed. As soon as CS# is driven into the logic HIGH state, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a 1 when the erase cycle is in progress and a 0 when the erase cycle has been completed.

The internal control logic automatically handles the erase voltage and timing.

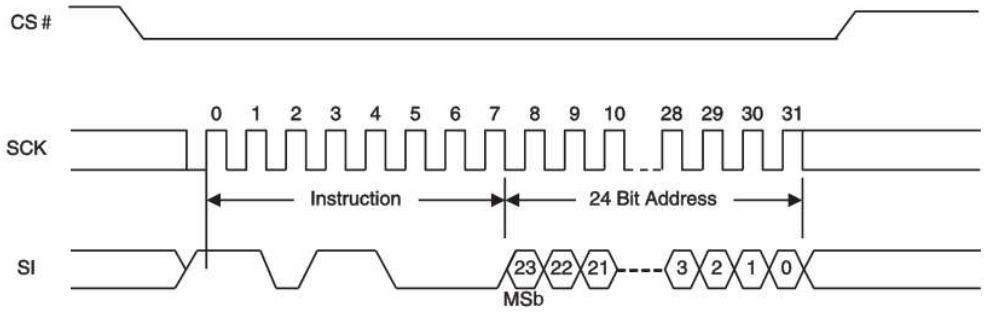

Figure 20: Block Erase sequence (D8h)

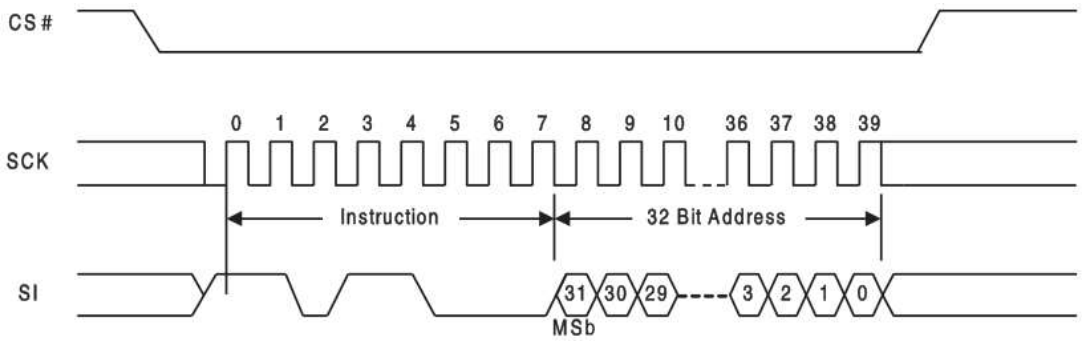

Figure 21: Block Erase 32 bits sequence (DCh)

3.5 REGISTER ACCESS

3.5.1 Write Status Register (01h)

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and Status Register write protection features by writing zeros or ones into the non-volatile BP3, BP2, BP1, BP0, and SRWD bits. Also WRSR instruction allows the user to disable or enable quad operation by writing '0' or '1' into the non-volatile QE bit.

Before the device can accept the WRSR command, a Write Enable (WREN) command must be received. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WRSR command is entered by shifting the instruction and the data bytes on SI. The Status Register is one data byte in length.

As soon as CS# is driven to the logic HIGH state, the self-timed WRSR operation is initiated. While the operation is in progress, the Status Register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a 1 during WRSR operation, and is a 0 when it is completed. When the is completed, the Write Enable Latch (WEL) is set to a 0.

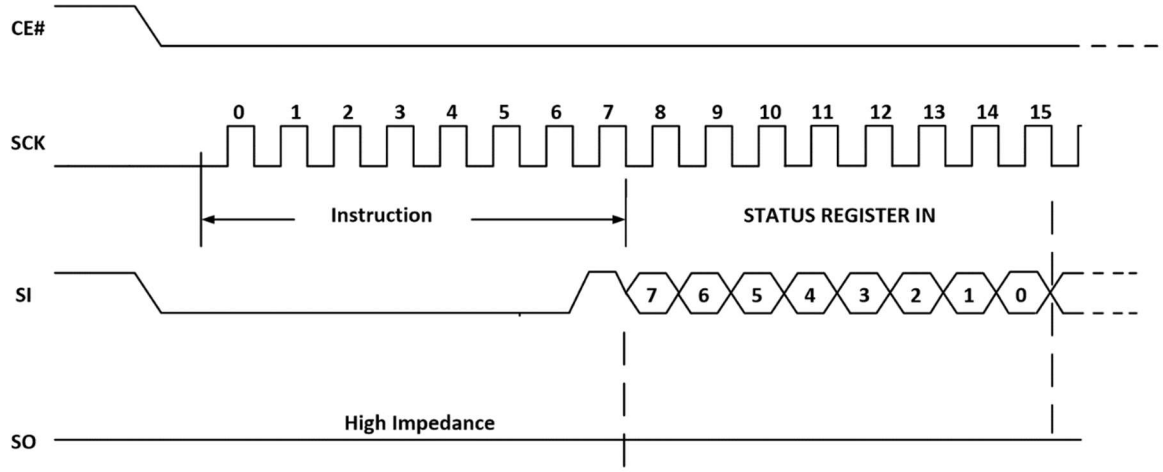

Figure 22: Write Status Register sequence (01h)

3.5.2 Read Status Register (05h)

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write Status Register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of

Status Register. It is possible to read the Status Register continuously by providing multiples of eight clock cycles. The status is updated for each eight-cycle read. **Maximum frequency for this command is 20 MHz**.

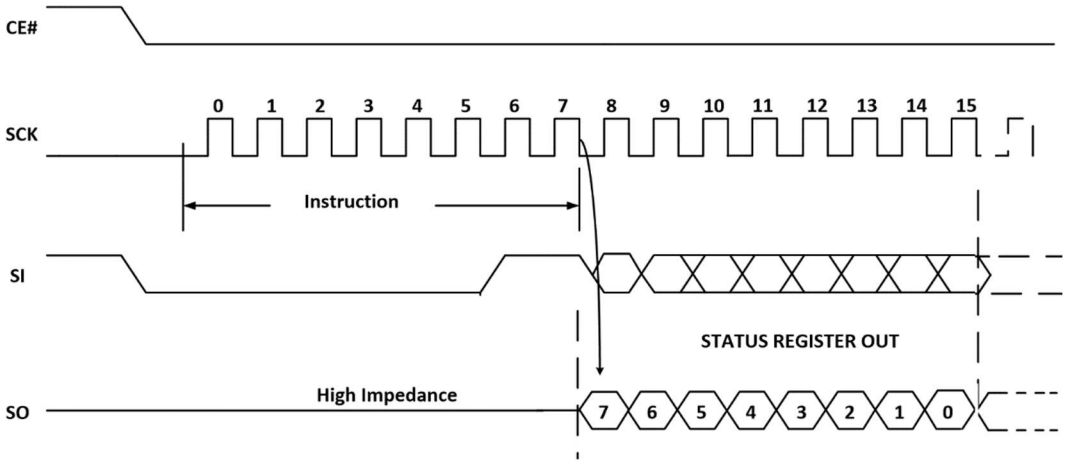

Figure 23: Read Status Register sequence (05h)

3.6 SOFTWARE RESET OPERATIONS: RESET ENABLE (66H) AND RESET (99H)

The Software Reset operation is used as a system reset that puts the device in normal operating mode. During the Reset operation, the value of volatile registers will default back to the value in the corresponding non-volatile register. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST). The operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset Enable.

Execute the CE_N pin low, sends the Reset-Enable command (66h), and drives CE_N high. Next, the host drives C_N low again, sends the Reset command (99h), and pulls CE_N high.

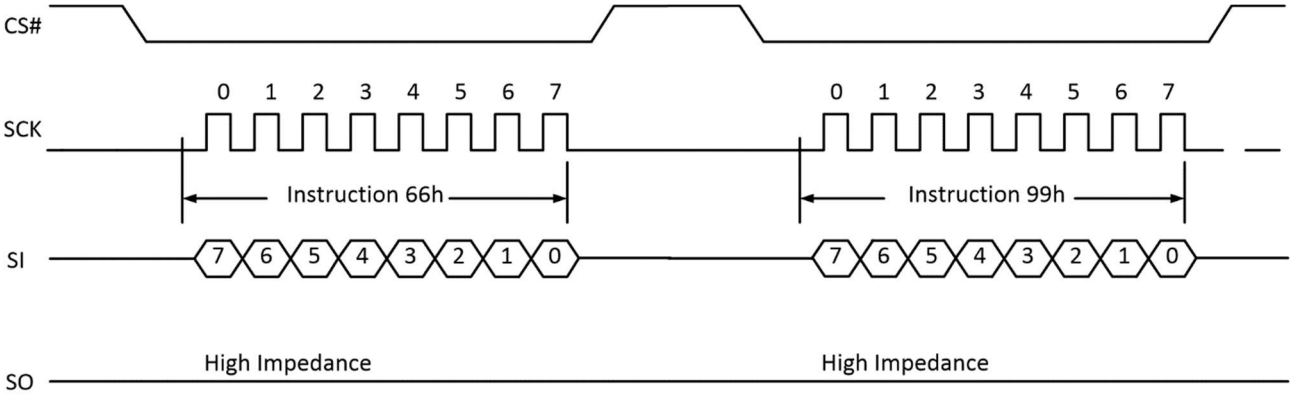

Figure 24: Reset Enable and Reset sequence

3.7 FOUR BYTES MODE

3.7.1 Enter 4 Bytes Mode (B7h)

The enter 4 Bytes Address Mode command sets internal register bit to change all bytes address commands to require 4 bytes of address. This command will not affect 4 bytes only commands.

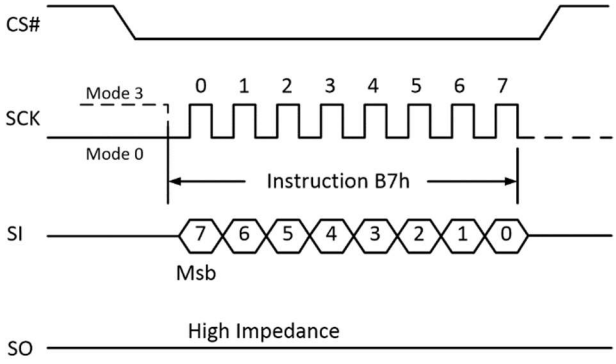

Figure 25: Enter 4 Bytes mode sequence

To return to 3 Bytes Address Mode see command below. In addition, a hardware or software reset may be used to return to the 3 bytes address mode.

3.7.2 Exit 4 Bytes Mode (29h/E9h)

The exit 4 Bytes Address Mode command sets internal register bit. This will change byte address commands to require 3 bytes of address. This command will not affect 4 bytes only commands, which will continue to expect 4 bytes of address.

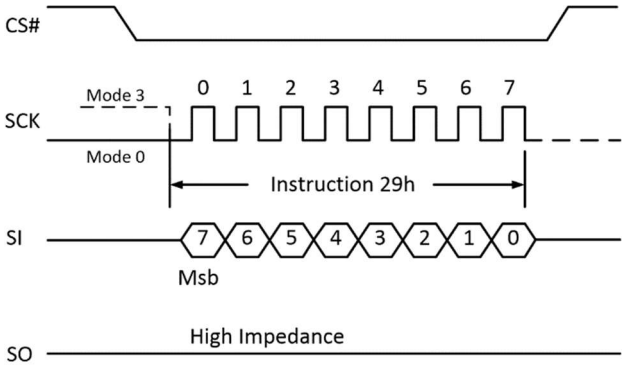

Figure 26: Exit 4 Bytes mode sequence

4. ERROR MANAGEMENT

4.1 DESCRIPTION OF RADIATION EVENTS

Radiation events (SEU, SET) can occur at different levels of a system. They are shown in the diagram below:

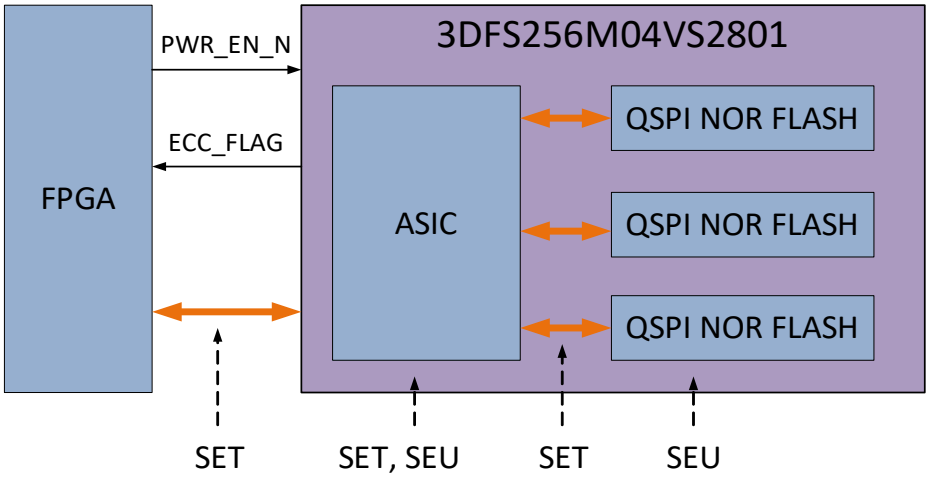

Figure 27: Radiation events occurrence

An SET may occur directly at the USER interface; a user provided algorithm protects against the effect of such events. 3D PLUS recommends to making three consecutive readings. The SET will only affect one out of the three readings, which can then be corrected. Reading systematically after each write operation ensures that the write operation has not been disturbed and can be repeated if a disturbance has occurred.

In the 3DFS256M04VS2801, an error can occur in the ASIC, the memories and the interface between ASIC and memories.

An SEU will change the value of a flip-flop (DFF), while an SET will disturb a signal and be recorded in a flip-flop if this disturbed signal is synchronized with a clock edge. In the ASIC, each flip-flop has the following TMR (Triple Modular Redundancy) structure:

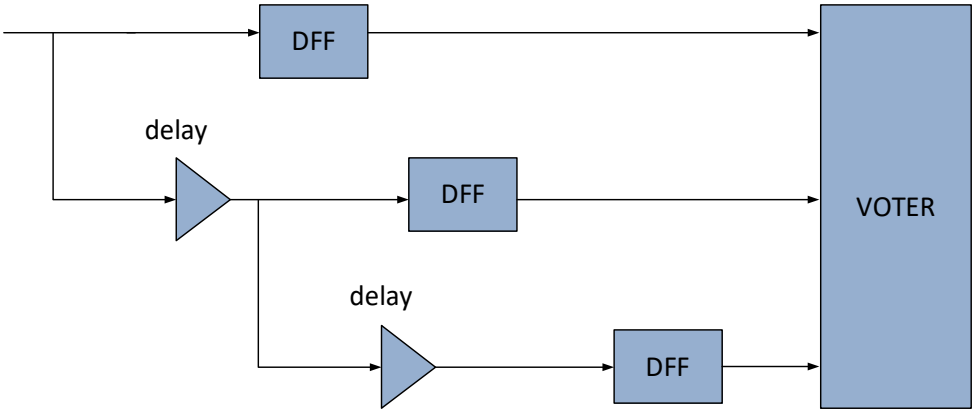

Figure 28: TMR structure within the ASIC

The majority voter of the TMR structure suppresses an SEU in any one of the three flip-flops. These delays between DFFs guarantee that a single SET can be stored in only one of the DFFs of the TMR structure and therefore the voter eliminates the error.

In case an SEU occurs in the QSPI NOR Flash memories, a majority voter in the ASIC will correct it.

4.2 ECC_FLAG AND MEMORY SCRUBBING

To help the user manage and monitor SEE errors in the module, an ECC_Flag signal is provided. This signal is generated from the ASIC voters and can be reset by PWR_EN_N signal or software reset operations. When there is no unanimity, the ECC_Flag will be raised and be visible during two clock cycles. The user should monitor the ECC_Flag and perform memory scrubbing in case of error detection.

During read operation, the ECC_Flag signal is presented along with the data on the user interface. Thus, the user receives data that has been corrected and is notified of the correction (by way of the ECC_Flag). The user will be able to rewrite the correct value (the one just received) in the memory in order to overwrite the SEU. At the end of the read operation, the ECC_Flag will be raised showing that an error or multiples errors occurred during the operation and that the user need to correct the data in the memory.

Until a PWR_EN_N signal or a software reset is issued by the used, the ECC_Flag will not be cleared.

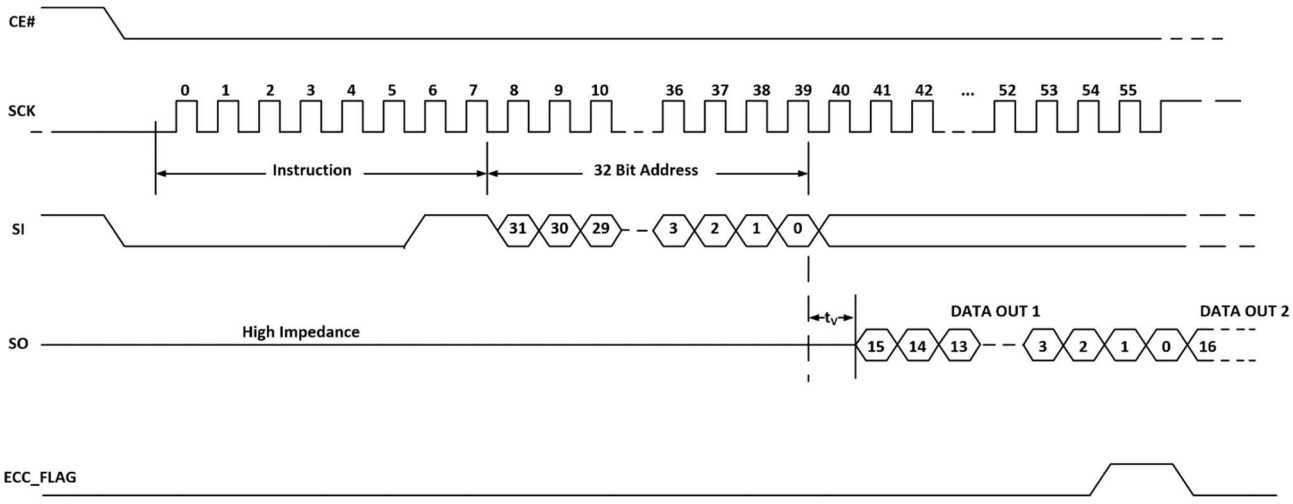

Figure 29: ECC_Flag timing diagram on READ (13h)

Note: The error is located on at least one of the bits 0 or 1.

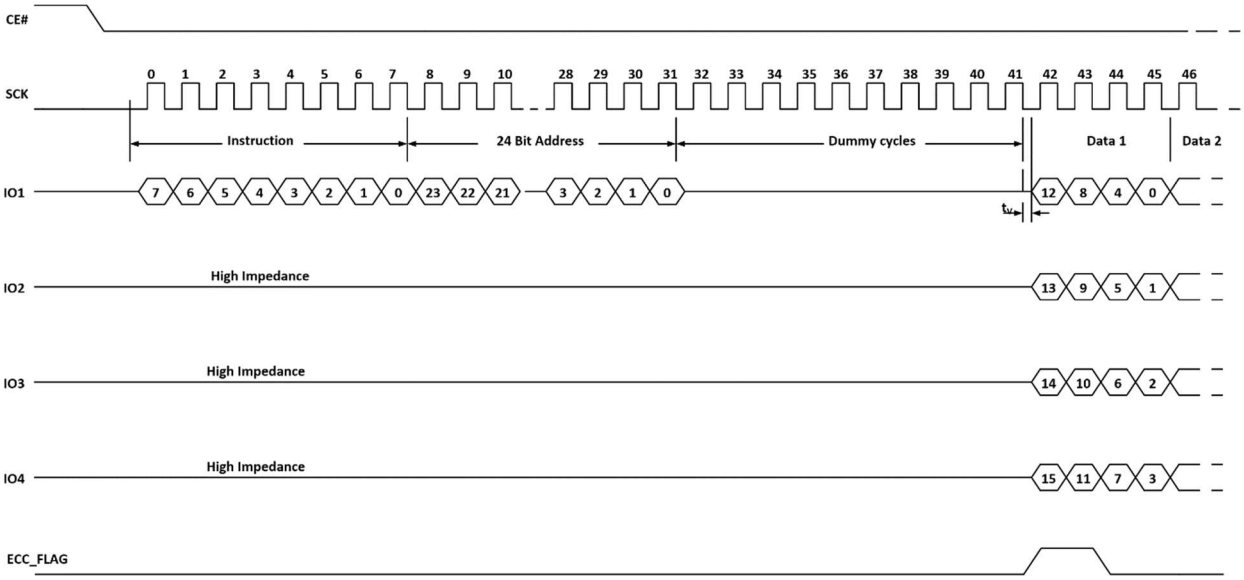

Figure 30: ECC_Flag timing diagram on READ (6Bh)

Note: The error is located on at least one of the bits among byte [8, 15].

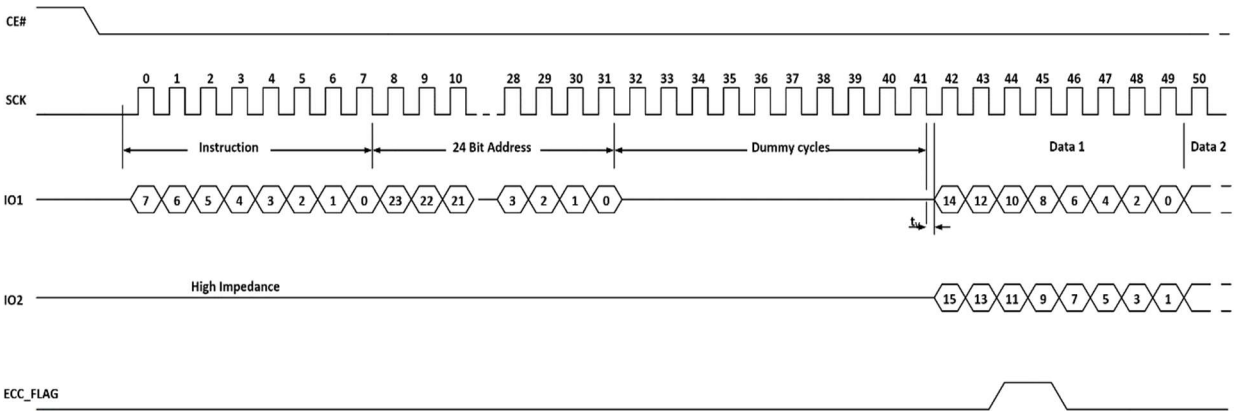

Figure 31: ECC_Flag timing diagram on READ (3Bh)

Note: The error is located on at least one of the bits of nibble [8, 11].

5. NOR FLASH DESCRIPTION

In all this section, we name the 256 Mbit embedded device the NOR Flash memory. The 3DFS256M04VS2801 is the module.

5.1 SYSTEM CONFIGURATION

Each NOR Flash memory array is divided into uniform 8 KByte sectors or uniform 64/128 KByte blocks. A block consists of eight/sixteen adjacent sectors respectively. Table 7 below illustrates the memory map of the NOR Flash.

BANK/EMBEDDED DEVICE DENSITY	BLOCK # (128 KBYTE)	BLOCK # (64 KBYTE)	SECTOR #	SECTOR SIZE (KBYTE)	ADDRESS RANGE (HEXA)
256 Mbit	Block 0	Block 0	Sector 0	8	0000 0000-0000 1FFE
			:	:	:
		Block 1	:	:	:
			Sector 15	8	0001 E000-0001 FFFE
	Block 1	Block 2	Sector 16	8	0002 0000-0002 1FFE
			:	:	:
		Block 3	:	:	:
			Sector 31	8	0003 E000-0003 FFFE
	Block 2	Block 4	Sector 32	8	0004 0000-0004 1FFE
			:	:	:
		Block 5	:	:	:
			Sector 47	8	0005 E000-0005 FFFE
	:	:	:	:	:
	Block 63	Block 126	Sector 1008	8	007E 0000-007E 1FFE
			:	:	:
		Block 127	:	:	:
			Sector 1023	8	007F E000-007F FFFE
	:	:	:	:	:

	Block 127	Block 254	Sector 2032	8	00FE 0000-00FE 1FFE
			:	:	:
		Block 255	:	:	:
			Sector 2047	8	00FF E000-00FF FFFE
	:	:	:	:	:
	Block 254	Block 508	Sector 4064	8	01FC 0000-01FC 1FFE
			:	:	:
		Block 509	:	:	:
			Sector 4079	8	01FD E000-01FD FFFE
	Block 255	Block 510	Sector 4080	8	01FE 0000-01FE 1FFE
			:	:	:
		Block 511	:	:	:
			Sector 4095	8	01FFE000-01FF FFFE

Table 7: SPI NOR Flash block/sector address

5.2 STATUS REGISTER

Status register format and Status register bit definitions are provided in Table 8 and Table 9 respectively.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
DEFAULT	0	0	0	0	0	0	0	0

Table 8: Status register format

BIT	NAME	DESCRIPTION	READ/WRITE	TYPE
Bit 0	WIP	Write In Progress Bit: '0' the device is ready (default) '1' a write cycle is in progress, device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch '0' the device is not write enabled (default) '1' the device is write enabled	R/W (1)	Volatile
Bit 2	BP0	Block Protection Bit (See Table 11 for details) '0' the specific blocks are not write-protected (default) '1' write protection enabled on the specific blocks	R/W	Non-Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit '0' the Quad output function is disabled (default) '1' the Quad output function is enabled	R/W	Non-Volatile
Bit 7	SRWD	Status Register Write Disable (see Table 13 for details): '0' not write protected (default) '1' write protected	R/W	Non-Volatile

Table 9: Status register bit definition

Note 1: WEL bit can be written by WREN and WRDI commands, but cannot by WRSR command.

The BP0, BP1, BP2, BP3, QE, and SRWD can be written by a Write Status Register (WRSR) instruction. The default value of the BP0, BP1, BP2, BP3, QE, and SRWD bits were set to '0' at factory. The Status Register can be read by the Read Status Register (RDSR).

Status Register bits are described as follows:

WIP: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is '0', the device is ready for Write Status Register, program or erase operation. When the WIP bit is '1', the device is busy.

WEL: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is '0', the write enable latch is disabled and the write operations described in Table 10 are inhibited. When the WEL bit is '1', the write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction except for Set volatile Read Register and Set Volatile Extended Read Register must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any write operation.

BP*i* (i from 0 to 3): The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 11 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

SRWD: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to '0', the Status Register is not write-protected. When the SRWD is set to '1' and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to'1' and WP# is pulled high (VIH), the Status Register can be changed by a WRSR instruction.

QE: The Quad Enable (QE) is a non-volatile bit in the status register that allows quad operation.

HEX CODE	OPERATION
02/12	Serial Input Page Program
32/34	Quad Input Page Program
D8/DC	128 Kbyte Block Erase
C7/60	Chip Erase
01	Write Status Register

Table 10: Instructions requiring WREN instruction ahead

STATUS REGISTER BITS				PROTECTED MEMORY AREA
BP3	BP2	BP1	BP0	TBS(T/B selection)=0, Top area
0	0	0	0	0 -- None
0	0	0	1	1 -- Block 255
0	0	1	0	2 -- Blocks 254 and 255
0	0	1	1	4 -- Blocks 252 to 255
0	1	0	0	8 – Blocks 248 to 255
0	1	0	1	16 Blocks 240 to 255
0	1	1	0	32 Blocks 224 to 255
0	1	1	1	64 Blocks 192 to 255
1	0	0	0	128 Blocks 128 to 255
1	0	0	1	All Blocks
1	0	1	x	
1	1	x	x	

Table 11: 128 Kbyte block assignment by Block Write Protect (BP) bits

Note : x = don't care

READ MODES	MODE	DUMMY CYCLES	REMARK	P4, P3
Read Page 03h	SPI	0	Max 20 MHz	xx
Fast Read 0Bh	SPI	10	Max 50 MHz	xx

Table 12: Dummy cycles vs Read modes

Note 1 : Dummy cycles in the table are including Mode bit cycles . Must satisfy bus I/O contention. For instance, if the number of dummy cycles and AX bit cycles are the same, then X must be Hi-Z.

5.3 PROTECTION MODES

The NOR Flash supports hardware and software write-protection mechanisms.

5.3.1 Hardware Write Protection

The Write Protection (WP#) pin in combination with SRWD bit provide a hardware write protection method for the Status Register and thus a hardware input controlled protection.Table 13 below clearly shows :

- If SRWD bit is LOW, there is no hardware protection
- If SRWD bit is HIGH, the WEL bit is arguably LOW. WEL bit is automatically reset after a write/program/erase operation. When the WP# is pulled LOW, the bits of Status Register become read-only, and 01h (write status register) instruction will be ignored.
- If SRWD bit is HIGH, to write again the memory, user need first to pull WP# HIGH, then SRWD bit can be changed to LOW by 01h instruction.

Write inhibit voltage (V_{WI}) is specified in section TBC. All write sequence will be ignored when V_{CC} drops to V_{WI}.

SRWD	WP#	STATUS REGISTER
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Table 13: Hardware Write Protection on status register

Note : Before the execution of any program, erase or write Status Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If WEL bit is not enabled, the program, erase, or write register instruction will be ignored.

5.3.2 Software Write Protection

The device also provides a software write protection feature. The Block Protection (BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage are as described in Table 14 below.

CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Power Supply	V_{CC}	0 to +5.0	V	(Note 2)
Input Voltage with Respect to GND on all Pins	V_T	-0.5 to V_{CC} + 0.5	V	(Note 2)
All Output Voltage with Respect to Ground	-	-0.5 to V_{CC} + 0.5	V	(Note 2)
Storage Temperature Range	T_{STG}	-55 to +150	°C	-
Power Dissipation	P_{DMAX}	0.7	W	-
Maximum Junction Temperature	T_{JMAX}	+150	°C	-
Body Temperature (short exposure only)	T_{BODY}	+215	°C	Measured at module side level (exposure < 60s)

Table 14: Absolute Maximum Ratings

Note 1: Permanent module damage, including package and Die, may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods could affect device reliability.

Note 2: Minimum DC voltage on inputs or I/O pins is –0.5 V. During voltage transitions, inputs or I/O pins may undershoot GND by -2.0 V for periods not exceeding 20 ns. Maximum DC voltage on inputs or I/O pins is V_{CC} + 0.5 V. During voltage transitions, inputs or I/O pins may overshoot V_{CC} by +2.0 V for periods not exceeding 20 ns.

6.2 RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Frequency for Normal Mode	f	-	-	20	MHz
Frequency for Fast Read Mode	f	-	-	50	MHz
Input High Voltage	V_{IH}	0.7 x V_{CC}	-	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Thermal Resistance Junction to Case	$R_{TH(J-C)}$ (Note 1)	-	-	15	°C/W
Thermal Resistance Junction to Ambiant with underfill	$R_{TH(J-A)\_underfill}$ (Note 2)	-	-	27	°C/W

Table 15: Recommended operating conditions

Note 1: In $R_{TH(J-C)}$ (Thermal resistance Junction to Case), Case is defined as the temperature at the module lateral sides, Junction is defined as the highest temperature at junction within the module.

Note 2: In $R_{TH(J-A)\_underfill}$, Ambient is defined as the temperature at the bottom of the leads in contact with the board.

This module shall be underfilled to ensure its performances at all the temperature ranges specified in [AD1]. The underfill shall have a thermal resistance lower or equal to 2.17 °C/W. For example an underfill with an area of 170 mm², a thickness of 1.4 mm and a thermal conductivity equal to 1.67 W/m°C (Stycast 2850 for example) is compliant.

6.3 PIN CAPACITANCE

For the 256Mbit QSPI TMR FLASH NOR module 3DFS256M04VS2801, the capacitance values are provided in the table below: (T_a = 25°C, V_{CC} = 3 V):

PARAMETERS	SYMBOL	MAX	UNIT
Input Capacitance PWR_EN_N	C_{IN1}	4	pF
Input Capacitance (CE_N, SCK) on each USERy_BUS	C_{IN2}	5.5	pF
Output Capacitance (IO3, IO2, IO1, IO0) on each USERy_BUS	C_{IO}	5.5	pF

Table 16: Module capacitance table

Note: y denotes A or B for USERy_BUS.

6.4 DC PARAMETERS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Active Current NORD	I_{CC1}	V_{CC} = V_{CCMAX} = 3.6 V f = 20 MHz	-	100	mA
Active Current FAST READ	I_{CC1_FRD}	V_{CC} = V_{CCMAX} = 3.6 V f = 50 MHz	-	100	mA
Program Current	I_{CC2}		-	125	mA
Sector Erase Current	I_{CC4}		2	150	mA
Chip Erase Current	I_{CC5}		-	125	mA
V_{CC} Standby Current	I_{SB1}	V_{CC} = V_{CCMAX} = 3.6 V PWR_EN_N = 0 V USERy_CE_N = 0.95*V_{CC}	-	10	mA
Deep Power Down Current	$I_{SB\_DeepPower}$	V_{CC} = V_{CCMAX} = 3.6 V PWR_EN_N = 0 V USERy_CE_N = 0 V Flash NOR Memories in Deep Power Mode	-	10	mA
Input Leakage Current Low for each input on USERy_BUS except USERy_CE_N	I_{LIL}	V_{CC} = V_{CCMAX} = 3.6 V V_{IN} = 0 V	-1	+1	µA
Input Leakage Current Low for each USERy_CE_N	I_{LIL}		-50	+50	µA
Input Leakage Current Low for PWR_EN_N	$I_{LIL\_PWR\_EN}$	V_{CC} = V_{CCMAX} = 3.6 V V_{IN} = 0 V	-50	+50	µA
Input Leakage Current High for each input on USERy_BUS except USERy_CE_N	I_{LIH}	V_{CC} = V_{CCMAX} = 3.6 V V_{IN} = V_{CCMAX}	-1	+1	µA

Input Leakage Current High for each USERy_CE_N	I_{LIH}		-50	+50	µA
Input Leakage Current High for PWR_EN_N	$I_{LIH\_PWR\_EN}$	$V_{CC} = V_{CCMAX} = 3.6$ V $V_{IN} = V_{CCMAX}$	-4	+4	mA
Output Low Voltage (SO0, SO1, SO2 and SO3) for each USERy_BUS	V_{OL}	$V_{CC} = V_{CCMIN} = 3.0$ V $I_{OL} = 100$ µA	-	0.2	V
Output High Voltage (SO0, SO1, SO2 and SO3) for each USERy_BUS	V_{OH}	$V_{CC} = V_{CCMIN} = 3.0$V $I_{OH} = -100$ µA	V_{CC} – 0.2 V	-	V

Table 17: Electrical characteristics - DC parameters

Note 1: The memory is initialized before measurements.

Note 2: y denotes A or B for USERy_BUS.

6.5 AC PARAMETERS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Clock frequency for normal read mode	f	--		20	MHz
Clock frequency for all other modes	f	--		50	MHz
Clock rise time	t_{CLCH} (1)		0.1		V/ns
Clock fall time	t_{CHCL} (1)		0.1		V/ns
Clock high time	t_{CKH} (1)		0.45 x 1/fmax		ns
Clock low time	t_{CKL} (1)		0.45 x 1/fmax		ns
USERy_CE_N high time	t_{CEH} (1)		7		ns
USERy_CE_N hold time	t_{CH} (1)		8		ns
Output Valid NOR	t_V	$V_{CC} = V_{CCMIN}$ $V_{IL} = 0$ V $V_{IH} = 0.95 \times V_{CC}$ $V_{OL} = 0.5 \times V_{CC}$ $V_{OH} = 0.5 \times V_{CC}$ f = 20 MHz		23	ns
Output Valid FRD	$t_{V\_fastread}$			8	ns
USERy_CE_N setup time	t_{CS}		6		ns
Output Hold Time	t_{OH}		2	-	ns
Sector Erase Time (8 KByte)	t_{ECS}		-	300	ms
Block Erase Time (64 KByte)	t_{ECB64}			0.5	s
Block Erase Time (128 KByte)	t_{ECB128}			1	s
Page program time	t_{PP}		-	0.8	ms

Output disable time	t_{DIS}	V_{OL} = 0.5 x V_{CC} – 0.2 V V_{OH} = 0.5 x V_{CC} + 0.2 V	-	30	ns
Data in setup time	t_{DS} (1)		2		ns
Data in hold time	t_{DH} (1)		7		ns
Chip Erase Time	t_{EC_2} (1)			90	s
Write status register time	t_W (1)			15	ms
Reset recovery time	t_{RST} (1)			100	µs
Memory readiness time	$t_{Ready\_"0"}$ (1)	PWR_EN_N toggling (1 to 0)		15	ms
	$t_{Ready\_"HZ"}$ (1)	PWR_EN_N in HZ		15	ms
CE_N disabled to power supply off	t_{OFF} (1)		2.5		ms

Table 18: Electrical characteristics - AC parameters

Note 1: These parameters are characterized and not 100% tested.

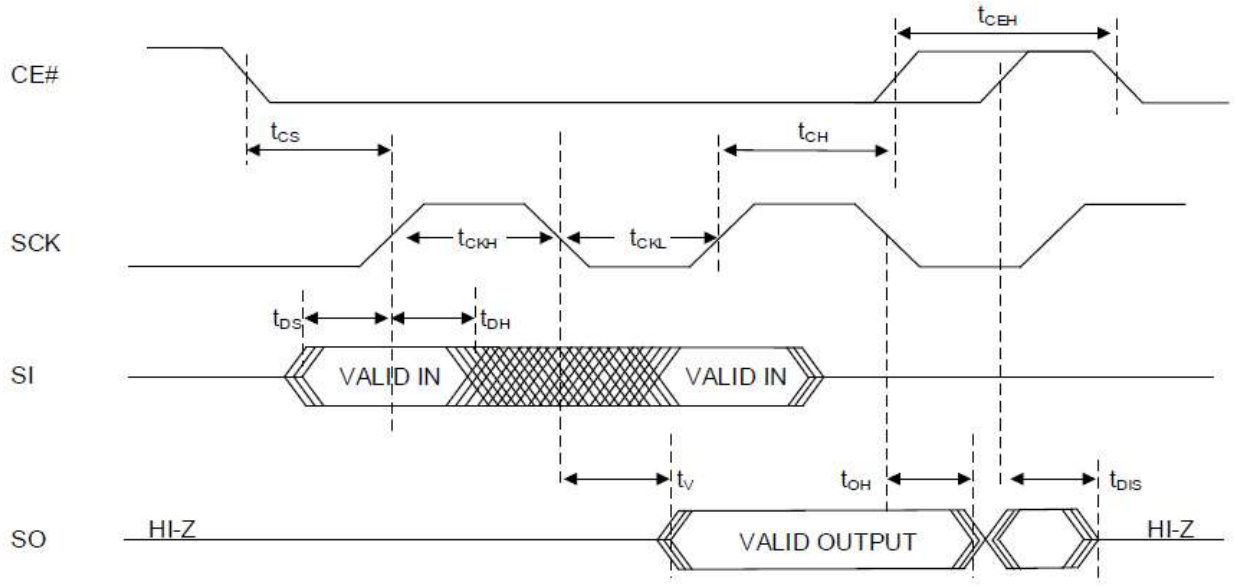

Figure 32: Serial input/output timing (Normal Mode)

Note: For SPI Mode 0 (0, 0)

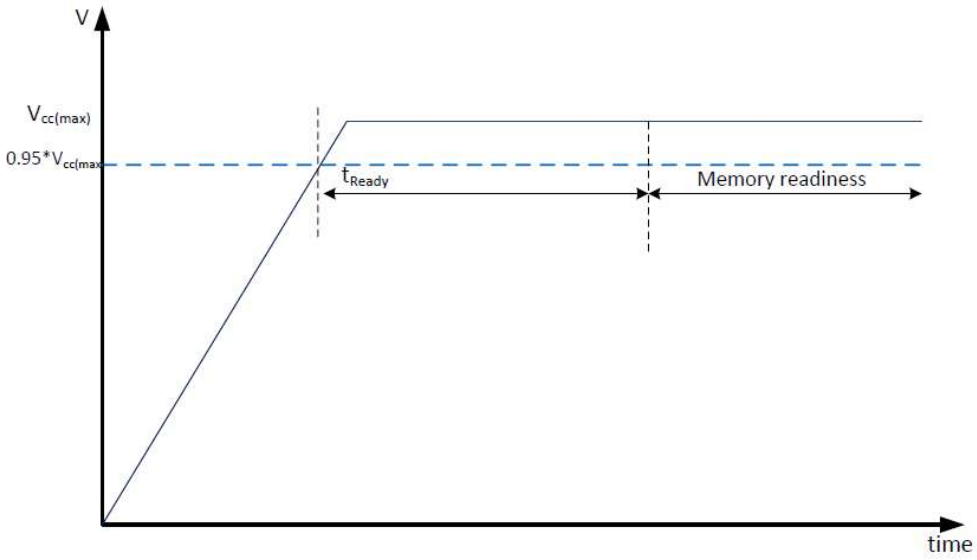

Figure 33: Power up timing

7. ORDERING INFORMATION

The 256 Mbit QSPI NOR Flash module is available with a combination of Temperature Ranges and screening levels to serve a broad range of applications and customers' requirements:

'CN', 'IB' or 'SB' Quality Grade to address Prototype/Engineering Models,

'IS' or 'SS' Quality Grade to address Flight Models.

For more details, please refer to 3D PLUS Website: https://www.3d-plus.com/quality-grades-reliability.php

3DFS256M04VS2801 X X X

Temperature range

C = (0°C to +70°C)
I = (-40°C to +85°C)
S = (-55°C to +105°C)

Screening level

N = Commercial grade
B = Industrial grade
S = Space Grade

Coating (option)

A = Arathane coating
M = Mapsil coating

Figure 34: Ordering information

A specific Source Control Drawing (SCD#) referenced [AD1] is available for the space qualified product and may be used for its procurement.

7.1 PACKAGING

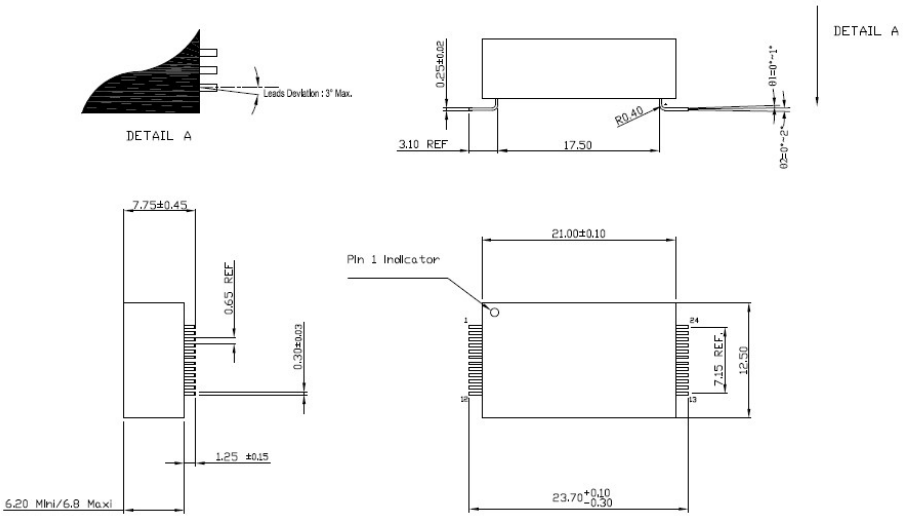

Figure 35: 3DFS256M04VS2801 mechanical drawing

Note:
Dimensions are in mm.
Standard Metallization: Ni-Au surface treatment on both body and leads (FeNiCo)
Case connected to GND.
Weight of the module is 4.50 g max.

7.2 UNDERFILL

This module shall be underfilled to ensure its performances at the temperature ranges specified in Table 1. The underfill shall have a thermal resistance lower or equal to 5°C/W.

We suggest to use an underfill with an area of 170 mm², a thickness of 1.4 mm and a thermal conductivity equal to 1.6 W/(m.K) (LOCTITE STYCAST 2850 MT CAT 27-1 for example) to achieve the thermal performances

For more details on how to underfill the module, please refer to [AD7]. The figure below is a drawing of the module footprint with underfilled area in blue.

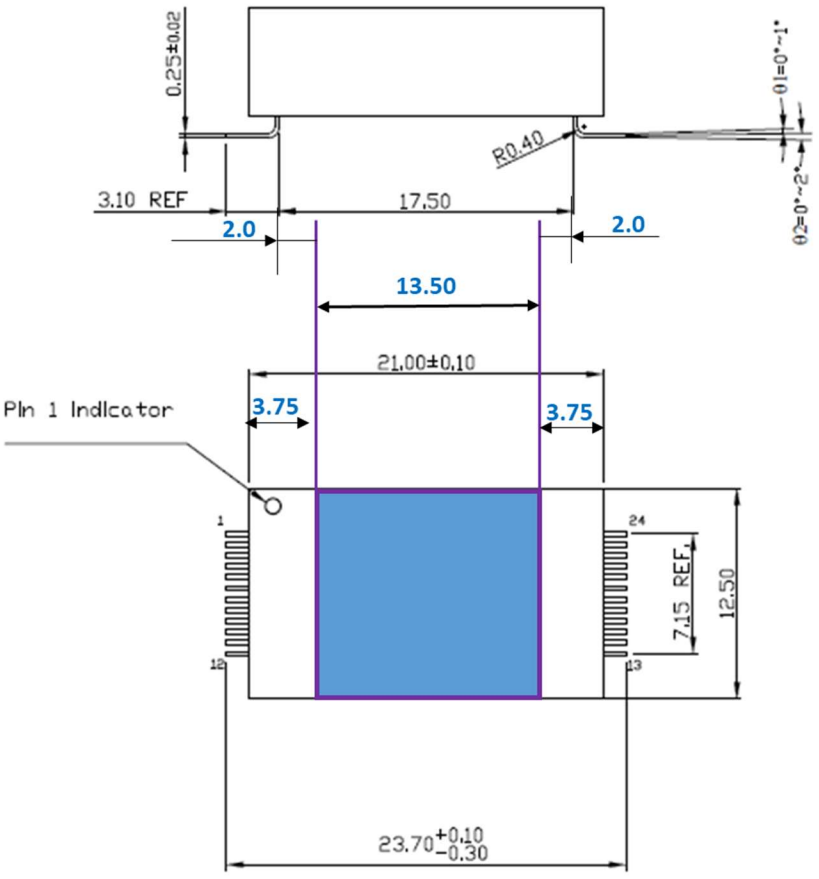

Figure 36: 3DFS256M04VS2801 with underfill

7.3 FOOTPRINT

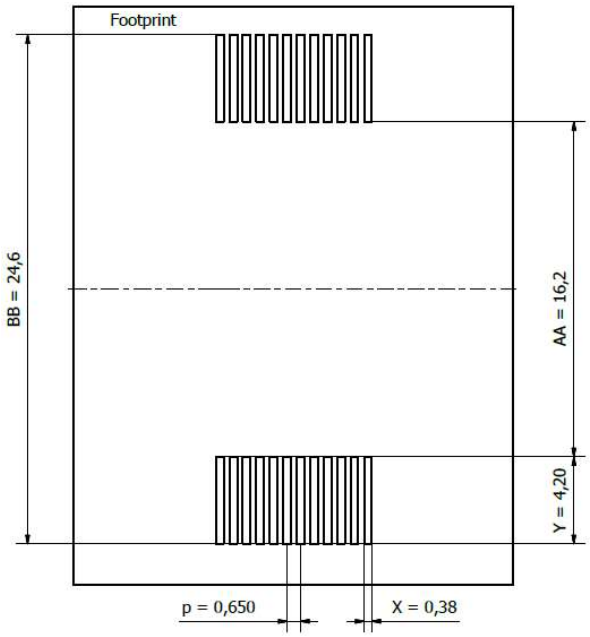

Figure 37: 3DFS256M04VS2801 footprint

Note:
The module is suitable for automatic reflow assembly process. Module assembly on board must follow reflow guidelines as defined in: http://www.3d-plus.com/technical-documentation.php

7.4 HANDLING AND ASSEMBLY RECOMMENDATIONS

Detailed recommendations concerning 3D PLUS module storage and assembly conditions are available in [AD2] and [AD3].

7.4.1 Handling

3D PLUS modules must be handled with antistatic gloves and an ESD wrist strap. The use of tools that could damage sides of components is prohibited. Refer to [AD2] and [AD3] for details. See section 7.4.4 herein for specific ESD rating.

7.4.1 Packing

Modules are packed in mini- trays. Made in polymeric material, these mini- trays fulfil JEDEC (EIAJ EDR 7602) requirements except about overall height. They are adaptable to 3D PLUS module form factor.
Each mini-tray is sealed with antistatic bag under vacuum with desiccant sachet.

Each module is marked as described hereafter:

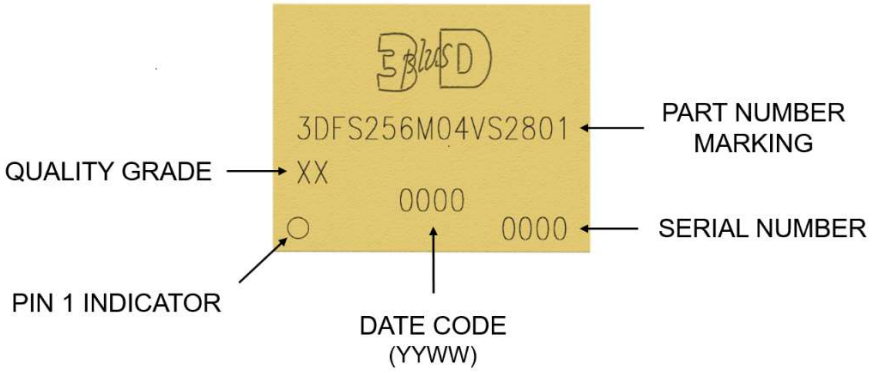

Figure 38: 3DFS256M04VS2801 marking

7.4.2 Storage

In order to avoid degradation due to humidity, 3D PLUS recommends storing the modules in dry environments (dry sealed bags, dry cabinet).

Storage in sealed bags: The calculated shelf life for dry sealed packed components is 12 months from the pack seal date, when stored in a non-condensing atmospheric environment of < 40 °C and < 90% RH. Beyond this period, modules should be baked at 125 °C for 48 hours.

If the provided sealed bags are opened, please refer to [AD2] and [AD3] for bakeout instructions

7.4.3 Board Assembly

After opening the sealed bags, 3D PLUS modules must be baked for 24 hours at 125°C. The use of any adhesive tape (e.g. Kapton®) on the side of the module during assembly is prohibited. Module assembly on board must follow reflow guidelines as defined in http://www.3d-plus.com/technical-documentation.php

It shall be noted that recommendations are different for manual assembly and automatic reflow. Module reinforcement, coating and lead tinning operations are also described in these documents.

Module cleaning after assembly must be done with isopropylic alcohol preferentially, or with de-ionized water otherwise. For other cleaning products, please consult 3D PLUS for further information.

7.4.4 Electrostatic Discharge Sensitivity

In order to avoid ESD damage and to guarantee reliable assembling of the 256 Mbit QSPI Flash NOR module, 3D PLUS methods and instructions for ESD protections or equivalent must be applied.

Human Body Model Classification (JS-001-2014) is 2000 V.

8. REVISION HISTORY

ED./REV.	DATE (DD/MM/YYYY)	DESCRIPTION
1	15/08/2020	Preliminary Datasheet
2	28/01/2021	Added Key Benefits (cover page) Added [AD4], [AD5], [AD6] Added section 0 Added Decoupling capacitors see Table 3, Note 2 Added section 3.1 Added chapter 6 Updated max frequency in read page mode Number of dummy cycles is ten. Added section 3 “Command starts on even address only” Added page size is 512 bytes
3	28/04/2021	Added key features: Supports only 16 bits word access (read and write) at even address Added section 2.2 Added sections 2.4.1 and 2.4.2 Changed sentence section 3 “Command starts on even address only” to “The 3DFS256M04VS2801 module only supports 16 bits word access (read and write) at even address». Timing diagrams of some operations updated accordingly Updated temperature range [-55°C, +125°C] to [-55°C, +105°C] Updated weight Added sections 6.3, 6.4 and 6.5 Added thermal resistances (R_{TH}) in Table 15 Added Timing diagrams on ECC_Flag in section 4.2 Modified: Note on Figure 37
4	21/09/2021	Timing parameters updated in Table 18 Section 7.2 added for underfill.
5	10/02/2022	QE bit removed Table 3 updated. IO1, IO2 and IO3 updated. Status Register updated. QE changed in DNU. Figure 22 and Figure 23 updated Section 4.2 clarified Table 11 modified: bottom sector removed Section 3.5.1: Added “Maximum frequency for this command is 20 MHz”
6	17/02/2022	**QE bit fixed and status register updated.** Maximum frequency for this command is 20 MHz” removed in section 3.5.1 Section 3.5.2: Added “Maximum frequency for this command is 20 MHz”
7	18/05/2022	WP# and HOLD# pins explained in Table 3

Table 19: Revision history

9. 3D PLUS SALES OFFICES

HEADQUARTERS (FRANCE)	TECHNICAL CENTER (USA)	DISTRIBUTOR
408, rue Hélène Boucher - ZI 78530 Buc Tel: +33 (0)1 30 83 26 50 E-mail: sales@3d-plus.com www.3d-plus.com	151 Callan Avenue - Suite #310 San Leandro, CA 94577 Tel: (510) 824-5591 E-mail: sales@3d-plus.com	