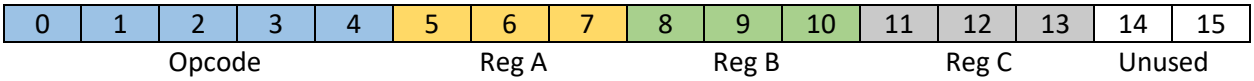
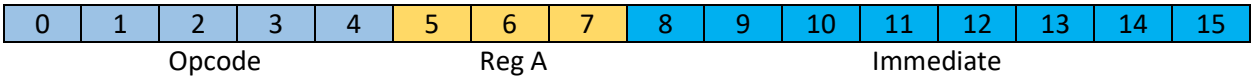
Instruction set architecture (RISC)

Instruction formats

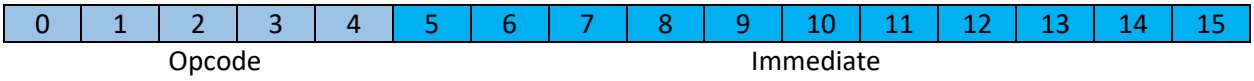
1. RRR type



2. RI type



3. I type



Architecture

Data Memory (RAM) – 8M x 16 bits

Instruction Memory (ROM) – 4K x 24 bits

MAR – 24-bit Register

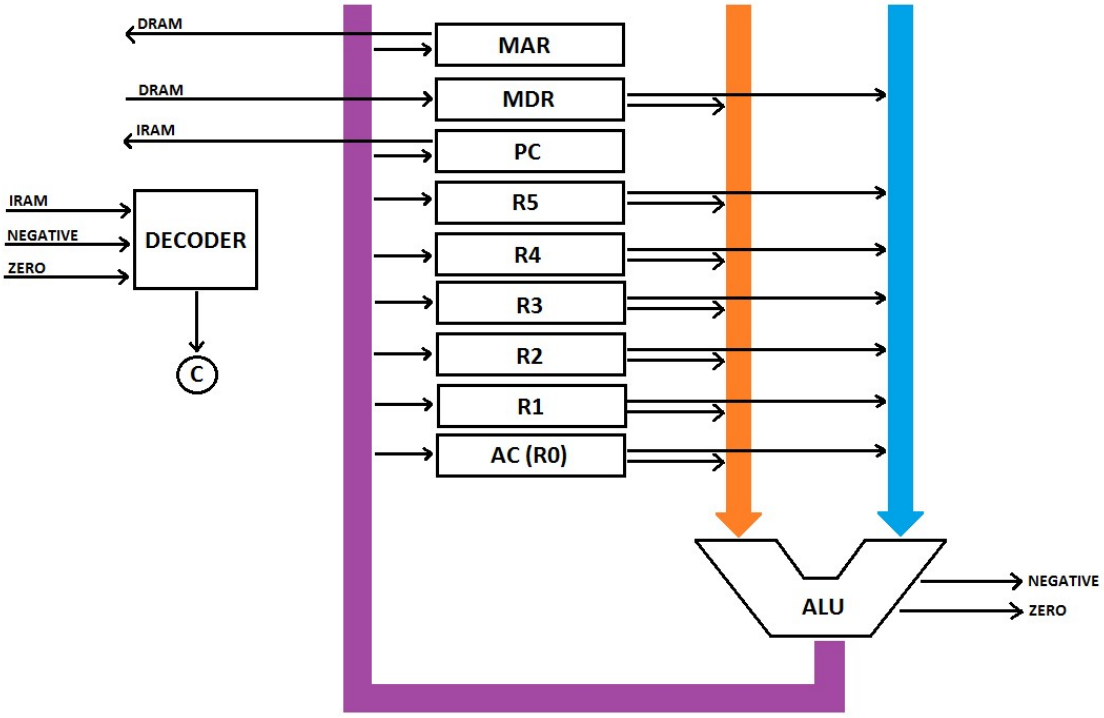
PC – 24-bit Register

Accumulator (AC, R0) – 24-bit Register

R1 – R7 General Purpose Registers – 24-bit

Instruction	Opcode	operation
NOP	00000	No operation
LOAD	00001	Reg A ← RAM[MAR]
STORE	00010	RAM[MAR] ← Reg A
MOVE		Reg A ← Reg B
LDPC		PC ← Reg A
LDMAR		MAR ← Reg A
LOADI		Reg A ← signed immediate (8-bit)
LDACI		AC ← signed immediate (11-bit)
ADD		Reg A ← Reg B + Reg C
SUB		Reg A ← Reg B - Reg C
MUL		Reg A ← Reg B << Reg C
DIV		Reg A ← Reg B >> Reg C
INC		Reg A ← Reg A + 1
DEC		Reg A ← Reg A - 1
NEG		Reg A ← -Reg B
NOT		Reg A ← Reg B (NOT) Reg C
AND		Reg A ← Reg B (AND) Reg C
OR		Reg A ← Reg B (OR) Reg C
XOR		Reg A ← Reg B (XOR) Reg C
JGT		If ALU out > 0 then PC ← Reg B else PC ← PC + 1
JEQ		If ALU out = 0 then PC ← Reg B else PC ← PC + 1
JGE		If ALU out >= 0 then PC ← Reg B else PC ← PC + 1
JLT		If ALU out < 0 then PC ← Reg B else PC ← PC + 1
JNE		If ALU out != 0 then PC ← Reg B else PC ← PC + 1
JLE		If ALU out <= 0 then PC ← Reg B else PC ← PC + 1
JMP		PC ← Reg B (Unconditional Jump)

Data path


DRAM
DRAM
IRAM
IRAM
NEGATIVE
ZERO
DECODER
C
MAR
MDR
PC
R5
R4
R3
R2
R1
AC (R0)
ALU
NEGATIVE
ZERO