The "hello_world" example

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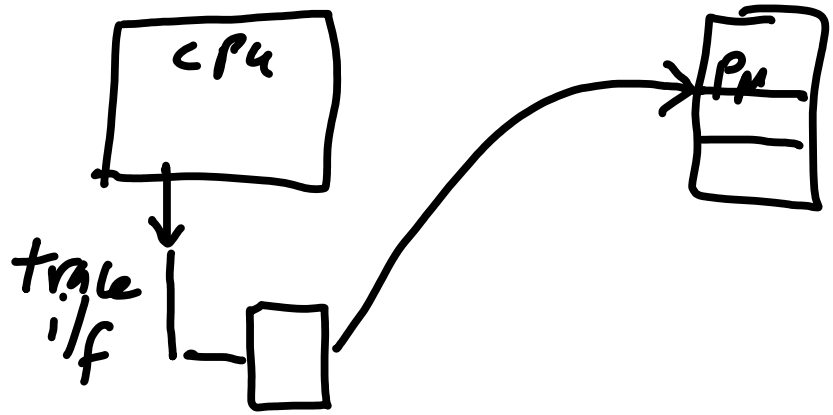
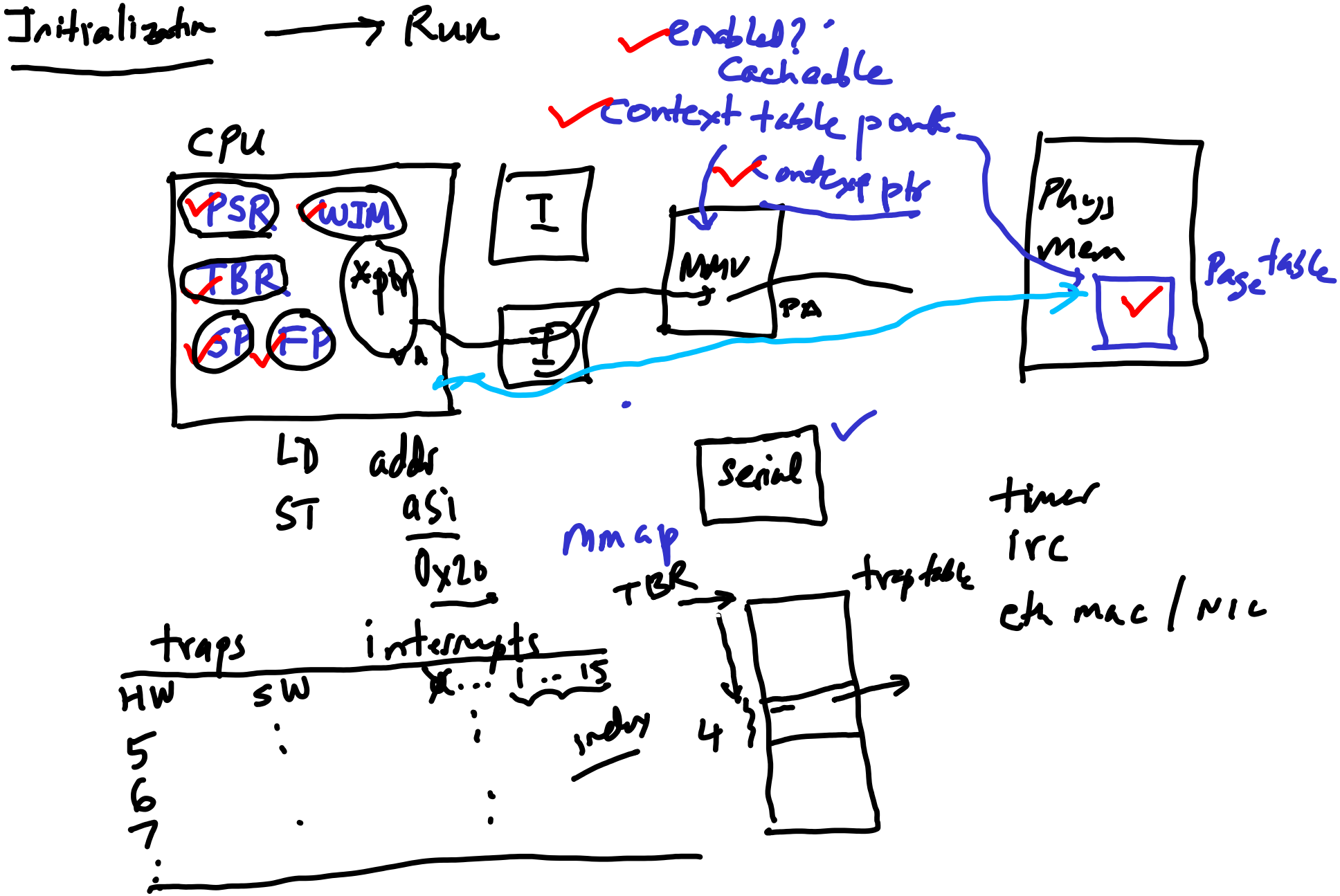
Overview

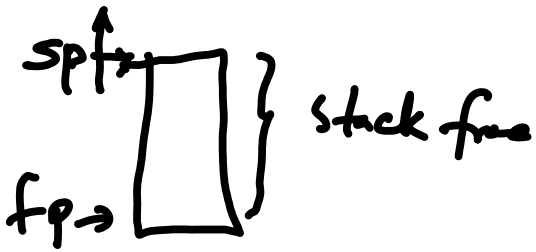


- Print “hello_world” and stop.
- Single core version.
  - Without MMU.
  - With MMU.
- Multi core version.
  - With MMU.

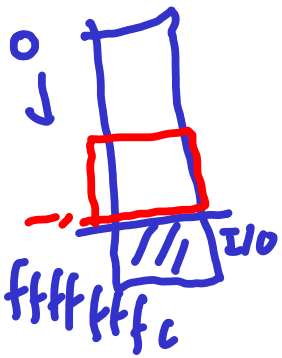
Blank slide: initialization of a processor core



Single core version: setting up the run-time environment without using the MMU



- Set up the stack and frame pointers.
  - We use virtual addresses from 0*xffff*3000 onwards for memory mapped I/O.
  - Set the initial stack and frame pointers at 0xffff2ffc since we are not passing anything to the main program in this example.
  - In general, you can set up the initial stack pointer and frame pointer to define a stack frame which can be used to pass arguments to your main program.



- Set the processor state register (PSR) to enable interrupts.
- Set the window invalid mask register to reserve one window for the trap handler.
- Set the default cacheable bit in the MMU control register.
  - This marks all accesses as cacheable (other than the bypass ASI accesses).

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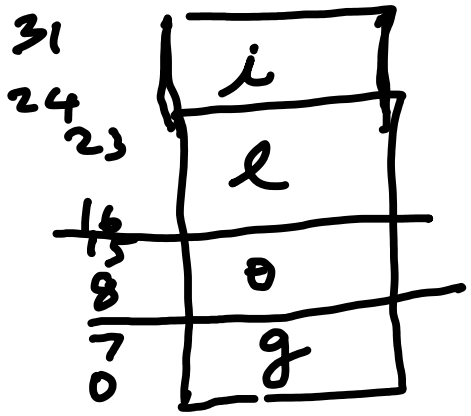
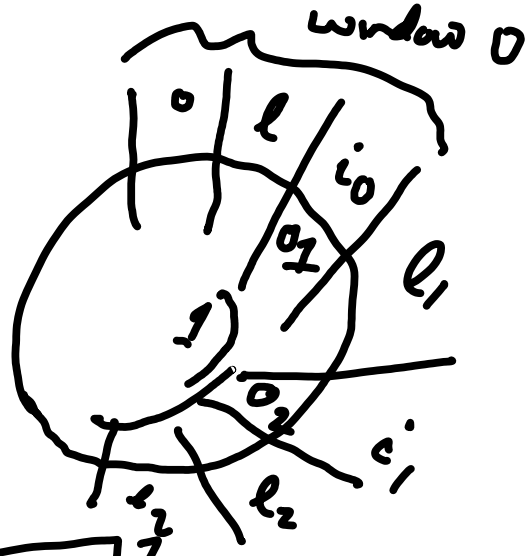
CPU

Sparcv8





Programmer visible

Window

0

Save ↓ 7

restore $g_0 \ldots g_7$

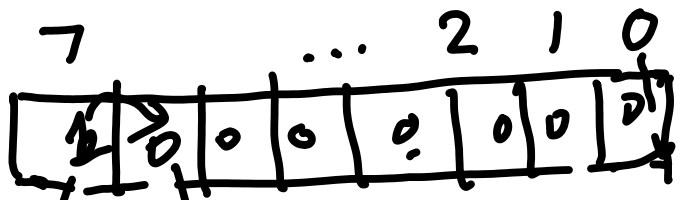
Min 2

max 32

AJIT (8)

1 window Reserved for TRAP handler

WIM



save to slm

Single core version: setting up the run-time environment using the MMU

- Same procedure as before, except for changes related to virtual to physical mapping.
- Write a VMAP file.
  - The script generates an assembly subroutine which sets up the page table in memory.
- Call the page table setup assembly subroutine and set the context table pointer.
- Enable the MMU.
- Run with full protection.

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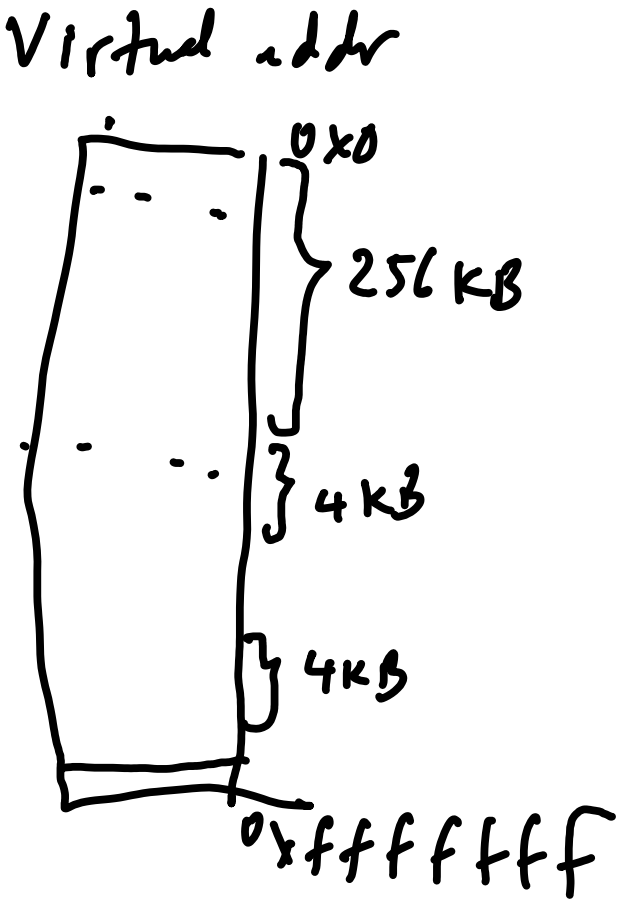
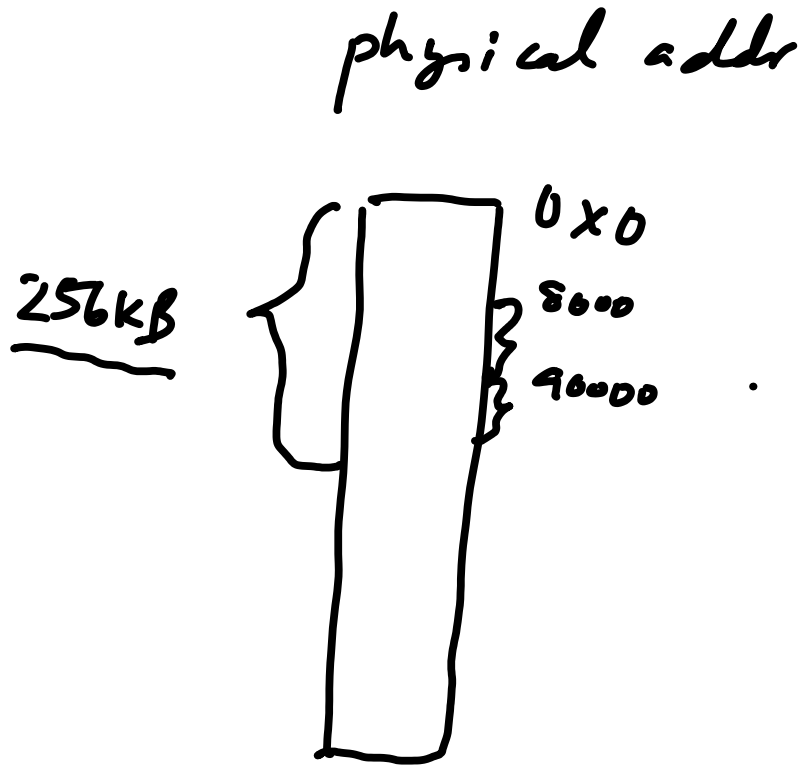

Virtual addr
0x0
256 KB
4KB
4KB
0xffffffff


physical addr
256kB
0x0
8000
90000

Multi core version: setting up the run-time environment using the MMU

- Set up the stack and frame pointers for each core.
- Set the processor state register (PSR) in each core, to enable interrupts.
- Set the window invalid mask register in each core, to reserve one window for the trap handler.
- Write a VMAP file.
- Call the page table setup assembly subroutine and set the context table pointer.
- Enable the MMU.
- Set up locks.
- Run.

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