Ajit Processor Pipeline Properties

Ashfaque Ahammed <ashfaque@iitb.ac.in>

Instructor: Prof. Madhav P. Desai <madhav@ee.iitb.ac.in>

Description: List of Ajit processor pipeline properties to be verified.

1. Each subsequent instructions will have an increasing slot-id. In other words current instruction's slot-id = previous instruction's slot-id + 1, except previous instruction have slot id of 255, that case current instruction count will be 0.

2. The output/task of each block is valid only when all of its inputs is applied/available of corresponding of same slot-id.

   - If a floating point load/store instruction the address is calculated by i-unit, so the load/store unit shoud have value of same slot-id on it's both data inputs(from fp-unit and i-unit).
   - The iretire unit should have all of it's input with same slot-id

3. If an instruction causes an exception, subsequent instructions on that thread make no effect (no changes) while passing through the pipeline (not allowed to write back) and carry the reason for the exception to iretire unit so that it will give control back to CCU.

4. Data hazards to be taken care. For example,

   ```
   add %l0 , %l1 , %o1
   sub %o0 , %l2 , %o2
   mul %o1 , %o2 , %o3
   ```

   Here the result of add instruction will be valid only after write-back state of add, which means after two pipeline-states, but sub, and mul need to wait till the output of add is valid.

5. Control hazards. If a branch is taken the PC value will be updated only in wb stage, so the subsequent instructions should not affect the state of the pipeline (annuled).

6. If a floating point exception occurred and the corresponding trap type is stored in FSR.ftt. FSR.ftt will hold that value until STFSR or other FPop is executed. LDFSR instruction does not affect ftt. When STFSR is executed it should explicitly zeroes ftt.

7. LSDFSR waits all FPop instruction that have not finished execution to complete before it loads, FSR.

8. If the delay-slot instruction is also a control transfer instruction,

9. Flush all i-buffers when instruction flush executes

10.

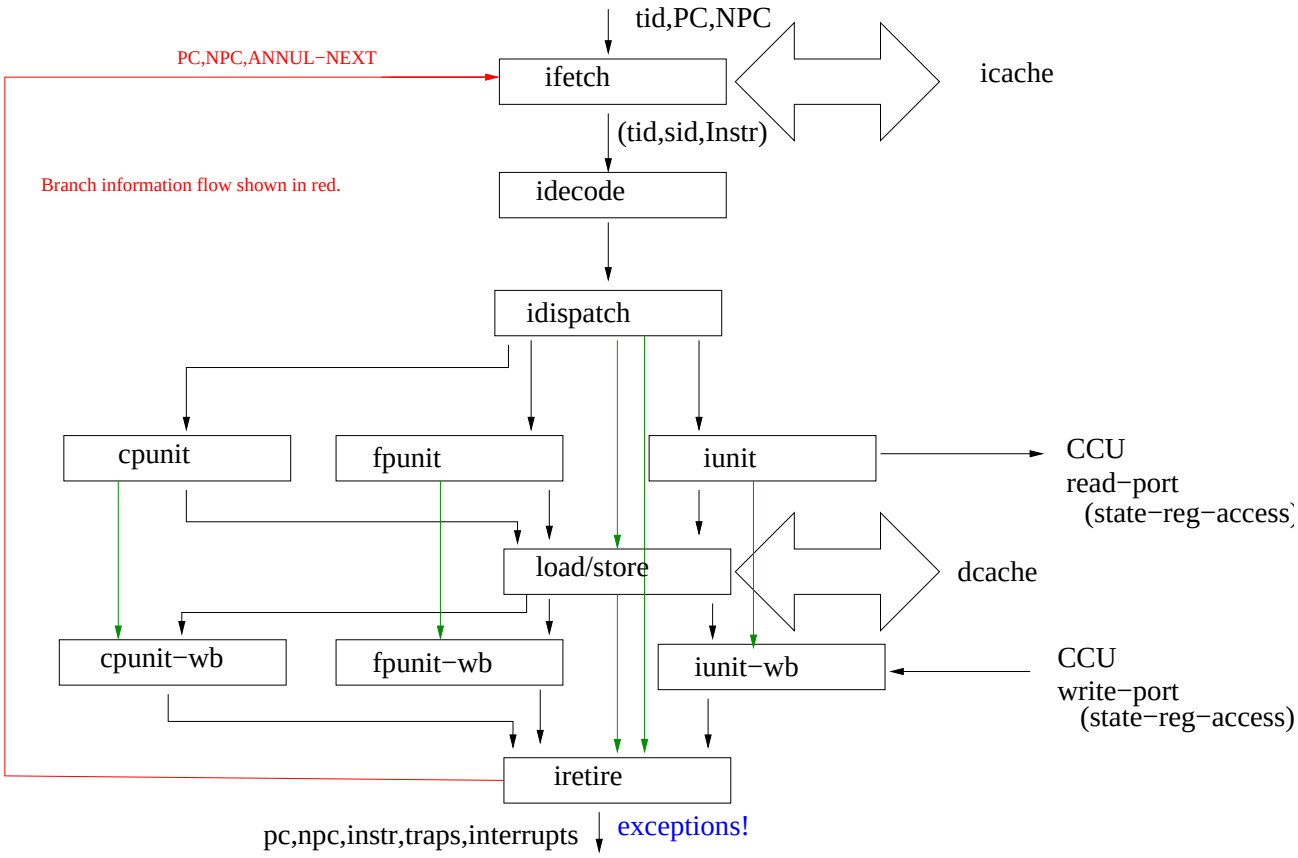

Figure 1: Ajit processor Thread Execution Unit block diagram (taken form Ajit_repo/documents)