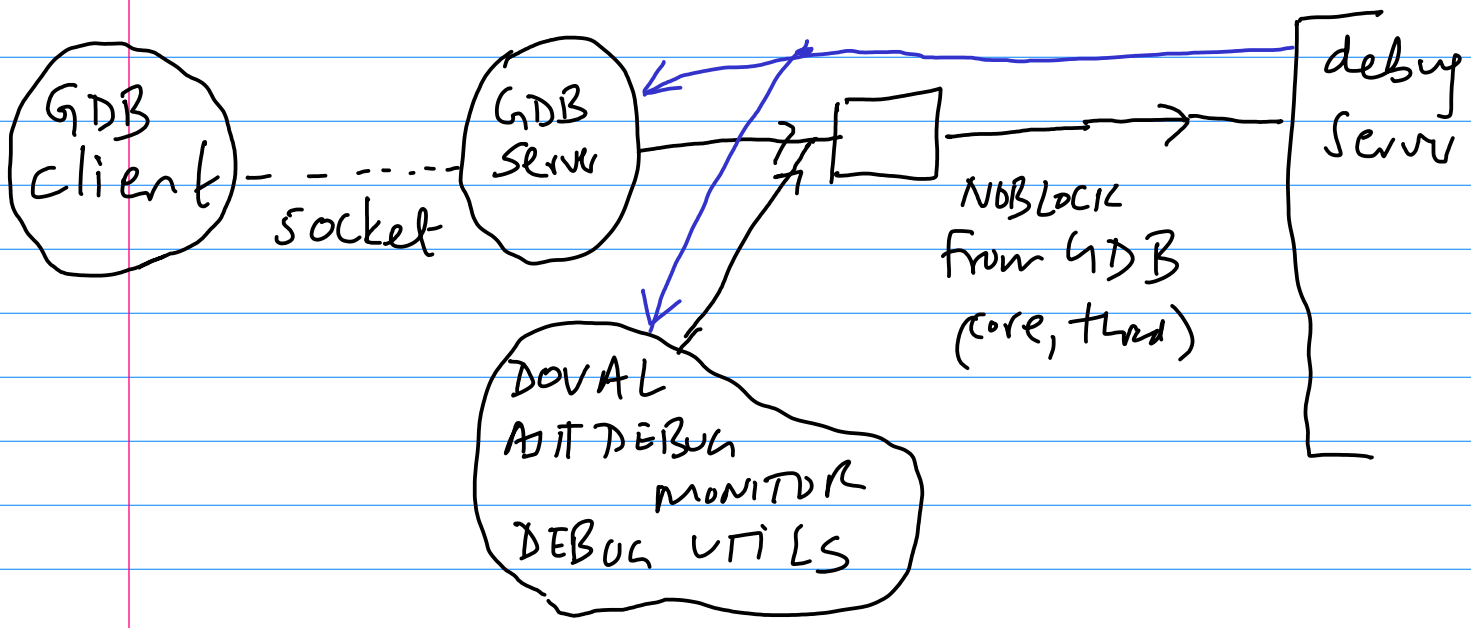
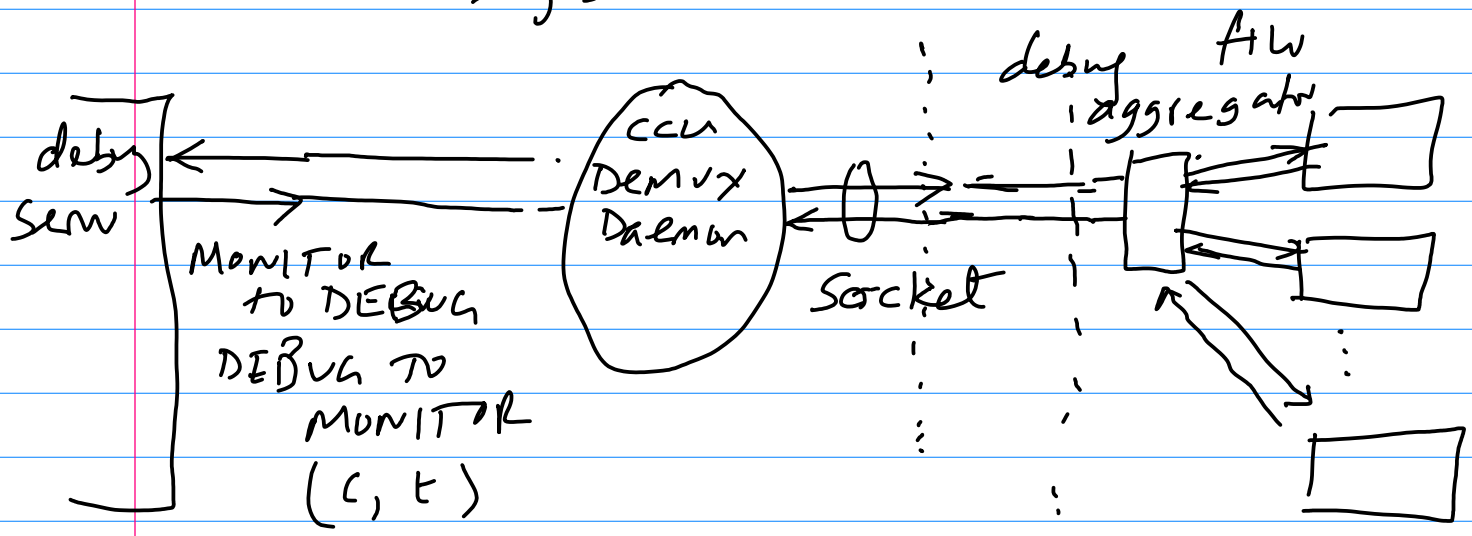
Information flow to the debug server from the "testbench" side



Information flow between debug server and "dut"



VHDL sim case