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TIMER DEVICE

1. Addresses of Timer Control Register (32b) : 0x3100

2. Timer Control Word :

31:1	0
Timer_max_count	Timer_en

3. Timer Period : The period of the timer (delay between enabling a timer and the assrtion of the interrupt) is given by :

Timer period = Timer_max_count/TIMER_TICK_REAL_FREQUENCY

The parameters TIMER_TICK_REAL_FREQUENCY, and TIMER_TICK_VIRTUAL_FREQUENCY are defined in Ajit_Hardware_Configuration.h.

4. Timer State Transitions :

The timer operates only in one-shot mode. It can be in one of following states:

- **TIMER_DISABLED** :The timer is in disabled state upon reset, and its interrupt output value is 0. When the cpu writes a control word with bit[0]=1, the count value is cleared and the timer moves to TIMER_ENABLED state.
- **TIMER_ENABLED** : When enabled, the timer keeps counting the number of ticks produced by a periodic tick source. The interrupt output is 0. When the count reaches "max_count", interrupt output is asserted , count is cleared and the timer moves to TIMER_INTERRUPTING state.
- **TIMER_INTERRUPTING** : The timer stops counting, and the interrupt output remains high, until the cpu explicitly disables the timer by writing bit[0]=0 into the control word register.