IITB RISC

Multi-cycle Implementation

Project-1

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Microprocessors

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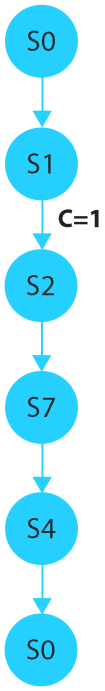
Contents

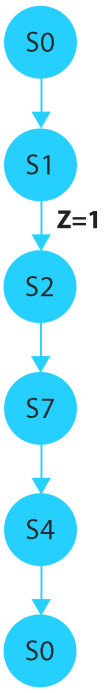
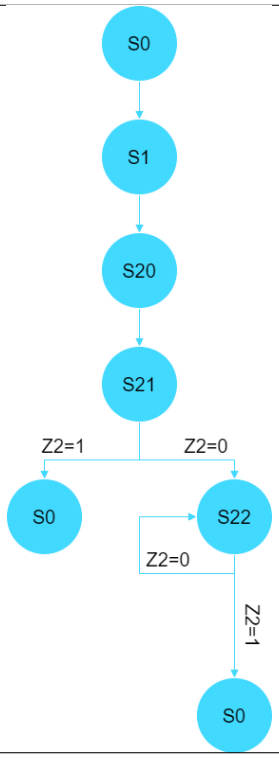
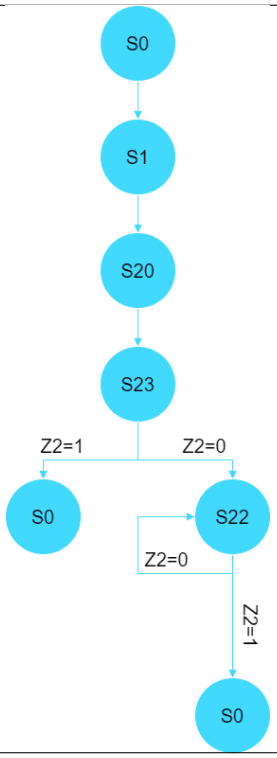
MICROPROCESSOR DESIGN

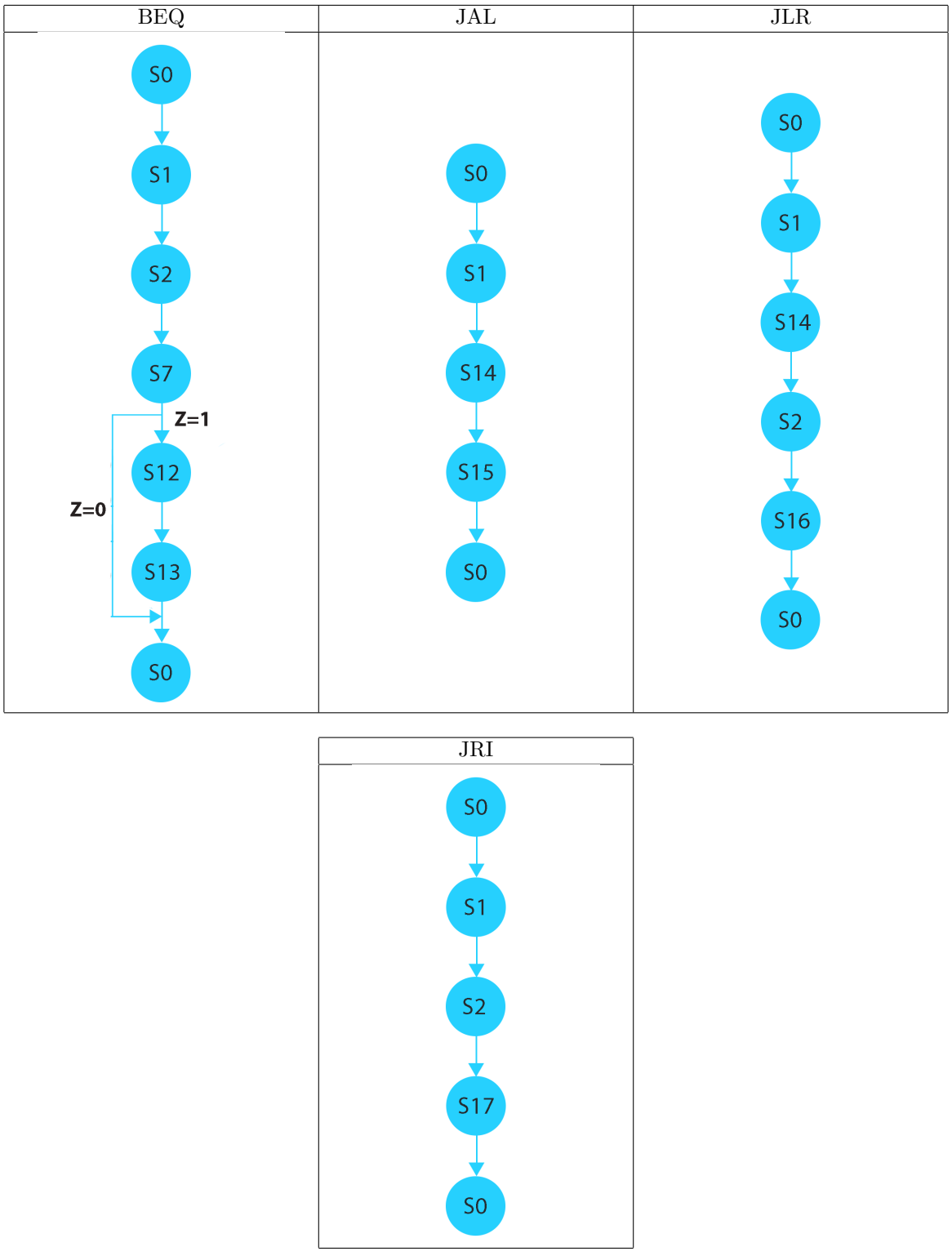
STATE ELABORATION

S1	$R_7 \longrightarrow MEM\_A, ALU\_A$ $+1 \longrightarrow ALU\_B$ $MEM\_D \longrightarrow IR$ $ALU\_out \longrightarrow R_7$
S2	$IR_{9-11} \longrightarrow RF\_A_1$ $IR_{6-8} \longrightarrow RF\_A_2$ $RF\_D_1 \longrightarrow T_1$ $RF\_D_2 \longrightarrow T_2$
S3	$T_1/(T_1 \rightarrow LS_1) \rightarrow ALU\_A$ $T_2 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_3$
S4	$IR_{3-5} \longrightarrow RF\_A_3$ $T_3 \longrightarrow RF\_D_3$
S5	$T_3 \longrightarrow RF\_D_3$ $IR_{6-8} \longrightarrow RF\_A_3$
S6	$IR_{0-5} \longrightarrow SE_{6-15} \longrightarrow T_2$ $IR_{9-11} \longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S7	$T_1 \longrightarrow ALU\_A$ $T_2 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_3$
S8	$IR_{0-8} \rightarrow SE_{9-15} \rightarrow LS_7 \rightarrow RF\_D_3$ $IR_{9-11} \longrightarrow RF\_A_3$
S9	$IR_{6-8} \longrightarrow RF\_A_2$ $RF\_D_2 \longrightarrow T_1$ $IR_{0-5} \longrightarrow SE_{9-16} \longrightarrow T_2$
S10	$T_3 \longrightarrow MEM\_A$ $MEM\_D \longrightarrow DR$
S11	$T_1 \longrightarrow ALU\_A$ $T_2 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_3$ $IR_{9-11} \longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S12	$IR_{0-5} \longrightarrow SE_{6-15} \longrightarrow ALU\_B$ $R_7 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S13	$+1 \longrightarrow ALU\_B$ $R_7 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S14	$R_7 \longrightarrow ALU\_A, RF\_D_3$ $+1 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow R_7$ $IR_{9-11} \longrightarrow RF\_A_3$
S15	$IR_{0-8} \longrightarrow SE_{9-15} \longrightarrow ALU\_B$ $R_7 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S16	$T_2 \longrightarrow R_7$
S17	$T_1 \longrightarrow ALU\_A$ $IR_{0-8} \longrightarrow SE_{9-15} \longrightarrow ALU\_B$ $ALU\_out \longrightarrow R_7$
S18	$DR \longrightarrow RF\_D_3$ $IR_{9-11} \longrightarrow RF\_A_3$
S19	$T_2 \longrightarrow MEM\_D$ $T_3 \longrightarrow MEM\_A$
S20	$IR_{0-7} \longrightarrow T_4$ $IR_{9-11} \longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_5$
S21	$T_4 \longrightarrow PE$ $PO_1 \longrightarrow T_6$ $PO_2 \longrightarrow T_4$ $T_5 \longrightarrow MEM\_A, ALU\_A$ $+1 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_5$ $MEM\_D \longrightarrow DR$
S22	$DR \longrightarrow RF\_D_3,$ $T_6 \longrightarrow RF\_A_3$ $T_4 \longrightarrow PE$ $PO_1 \longrightarrow T_6$ $PO_2 \longrightarrow T_4$ $T_5 \longrightarrow MEM\_A, ALU\_A$ $+1 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_5$ $MEM\_D \longrightarrow DR$
S23	$T_4 \longrightarrow PE$ $PO_1 \longrightarrow RF\_A_1$ $PO_2 \longrightarrow T_4$ $RF\_D_1 \longrightarrow T_1$
S24	$T_1 \longrightarrow MEM\_D$ $T_5 \longrightarrow MEM\_A, ALU\_A$ $+1 \longrightarrow ALU\_B$ $ALU\_out \longrightarrow T_5$ $T_4 \longrightarrow PE$ $PO_1 \longrightarrow RF\_A_1$ $PO_2 \longrightarrow T_4$ $RF\_D_1 \longrightarrow T_1$

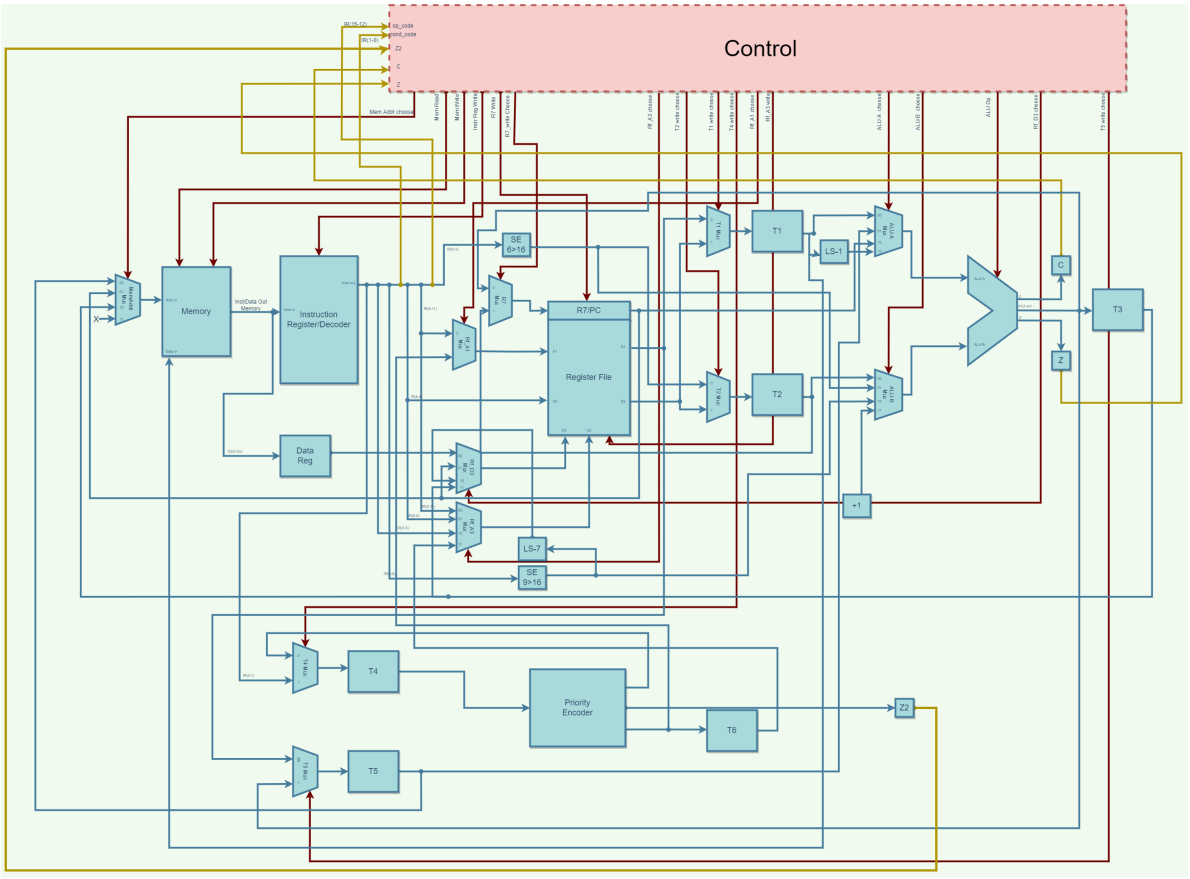
STATE FLOW DIAGRAM

ADD/ADL	ADC	ADZ
		
ADI	**NDU**	**NDC**
		

NDZ	LHI	LW
		
SW	**LM**	**SM**
		


BEQ
S0
S1
S2
S7
Z=1
S12
Z=0
S13
S0
JAL
S0
S1
S14
S15
S0
JLR
S0
S1
S14
S2
S16
S0
JRI
S0
S1
S2
S17
S0

DATAPATH


Control
Memory
Instruction Register/Decoder
Register File
R7/PC
Data Reg
T1
T2
T3
T4
T5
T6
LS-1
LS-7
SE 6>16
SE 9>16
+1
C
Z
Z2
Priority Encoder

CONTROL WORD

There are 25 control inputs needeed for the microprocessor.

Bit No.	Name	Use
24	MR	Enables Memory Read Operation
23	MW	Enables Memory Write Operation
22	IR EN	Enables write into Instruction register
21	PC EN	Enables Write into PC
20	PC MUX	Choose input to PC
19	RF EN	Enables Write into Register
18	PC MUX	Choose input to PC
17	T1 MUX	Decides input to T1
16	T2 MUX	Decides input to T2
15	T4 MUX	Decides input to T4(PE Inp reg)
14	T5 MUX	Decides input to T5(LM/SM Addr Reg)
13	T5 EN	Enables write into T5(LM/SM Addr Reg)
12	RF_A1 MUX	Decides input to RF_A1
11,10	MEM Addr MUX	Decides input to Address port of Memory
9,8	ALU A MUX	Decides input to ALU_A
7,6	ALU B MUX	Decides input to ALU_B
5,4	ALU_Op	Decides ALU Operation
3,2	RF_A3 MUX	Decides input to RF_A3
1,0	RF_D3 MUX	Decides input to RF_D3