IITB RISC

Multi-cycle Implementation

Project-1

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Microprocessors

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Contents

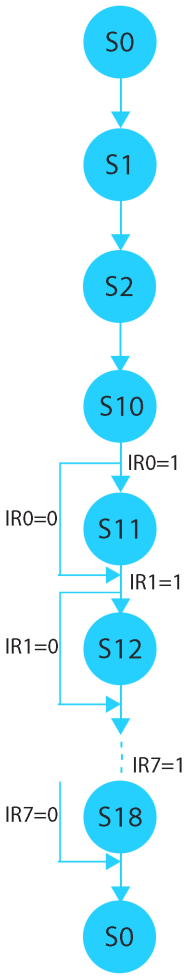
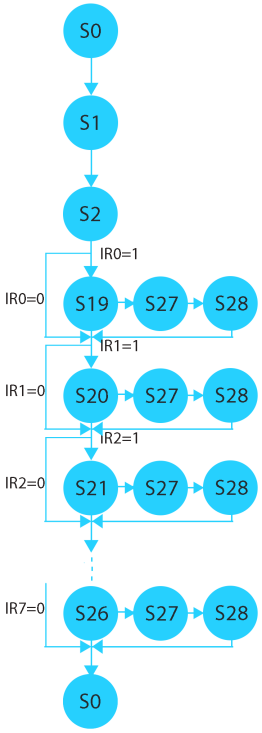
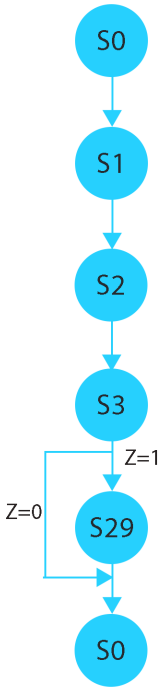
MICROPROCESSOR DESIGN

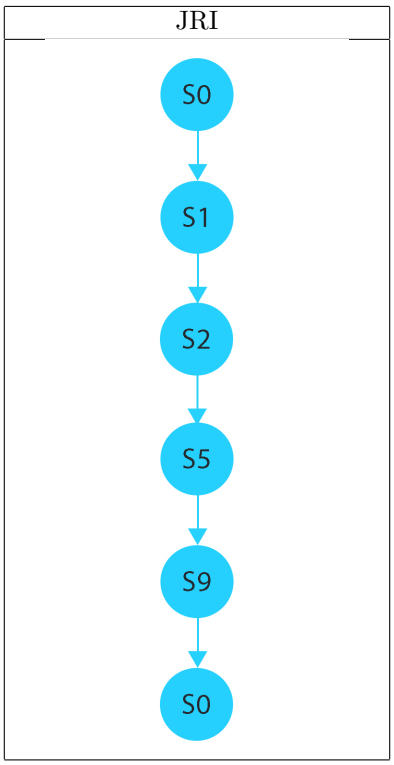
STATE ELABORATION

S1	$R_7 \longrightarrow MEM\_A, ALU\_B$ $MEM\_D \longrightarrow IR$ $+1 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S2	$IR_{6-8} \longrightarrow RF\_A_1$ $IR_{9-11} \longrightarrow RF\_A_2$ $RF\_D_1 \longrightarrow T_1$ $RF\_D_2 \longrightarrow T_2$
S3	$T_1/(T_1 \rightarrow LS_1) \rightarrow ALU\_A, ALU\_B$ $MEM\_D \longrightarrow IR$ $ALU\_out \longrightarrow R_7$
S4	$T_3 \longrightarrow RF\_D_3$ $IR_{3-5}/IR_{6-8} \longrightarrow RF\_A_3$
S5	$T_2 \longrightarrow ALU\_B$ $IR_{0-5} \longrightarrow SE_{6-16} \longrightarrow ALU\_A$ $ALU\_out \longrightarrow T_3$
S6	$IR_{0-8} \rightarrow SE_{9-16} \rightarrow LS_7 \rightarrow RF\_D_3$ $IR_{9-11} \longrightarrow RF\_A_3$
S7	$T_3 \longrightarrow MEM\_A$ $MEM\_D \longrightarrow T_3$
S8	$T_3 \longrightarrow RF\_D_3$ $IR_{9-11} \longrightarrow RF\_A_3$
S9	$T_3 \longrightarrow MEM\_A$ $T_1 \longrightarrow MEM\_D(I)$
S10	$T_2 \longrightarrow MEM\_A$ $MEM\_D \longrightarrow T_2$
S11	“000” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S12	“001” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S13	“010” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S14	“011” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S15	“100” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S16	“101” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S17	“110” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S18	“111” $\longrightarrow RF\_A_3$ $T_2 \longrightarrow RF\_D_3$
S19	“000” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S20	“001” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S21	“010” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S22	“011” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S23	“100” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S24	“101” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S25	“110” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S26	“111” $\longrightarrow RF\_A_1$ $RF\_D_1 \longrightarrow T_1$
S27	$T_2 \longrightarrow MEM\_D(I)$ $T_1 \longrightarrow MEM\_D$
S28	$T_2 \longrightarrow ALU\_B$ $+1 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow T_2$
S29	$R_7 \longrightarrow ALU\_B$ $IR_{0-5}/IR_{0-8} \rightarrow SE_{6-16}/SE_{9-16} \rightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S30	$R_7 \longrightarrow ALU\_B$ $+1 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow T_3$
S31	$T_3 \longrightarrow RF\_D_3$ $IR_{9-11} \longrightarrow RF\_A_3$
S32	$IR_{6-8} \longrightarrow RF\_A_2$ $RF\_D_2 \longrightarrow T_2$
S33	$T_2 \longrightarrow ALU\_B$ $+0 \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$
S34	$R_7 \longrightarrow MEM\_A$ $MEM\_D \longrightarrow IR$
S35	$T_2 \longrightarrow ALU\_B$ $IR_{0-8} \longrightarrow SE_{9-16} \longrightarrow ALU\_A$ $ALU\_out \longrightarrow R_7$

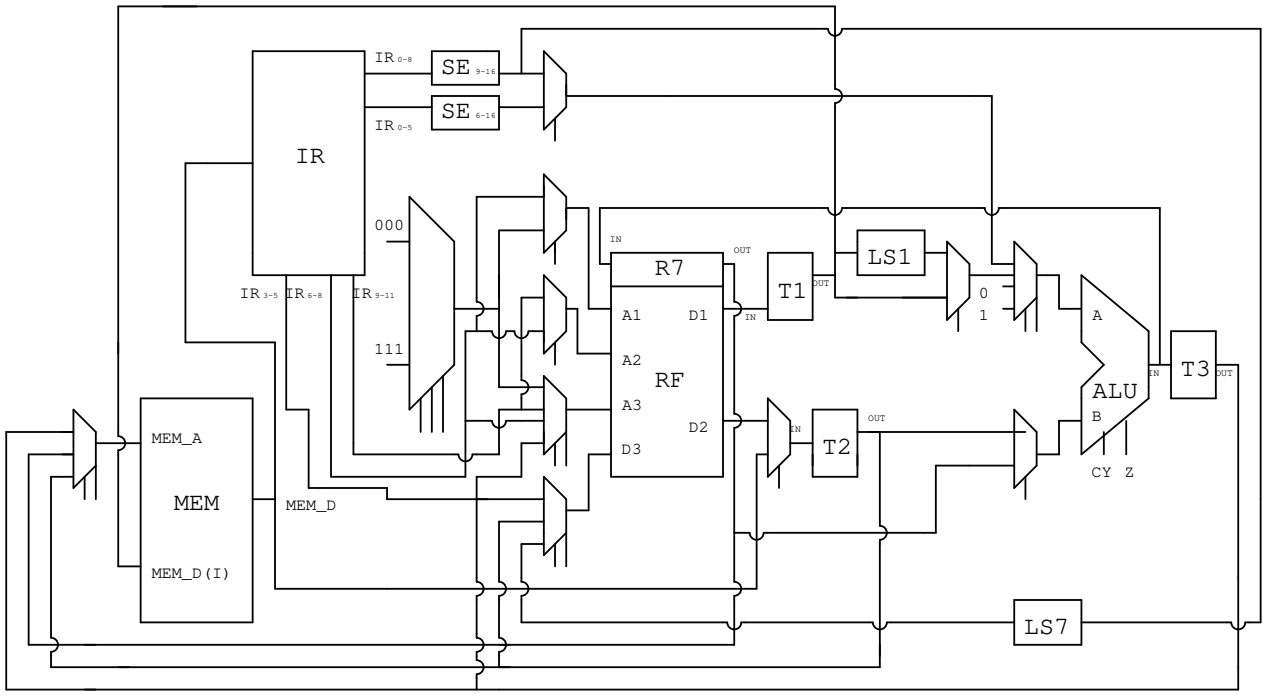
STATE FLOW DIAGRAM

ADD/ADL/NDU	ADC/NDC	ADZ/NDZ
		
ADI	**LHI**	**LW**
		

SW	LM	SM
		
BEQ	**JAL**	**JLR**
		


JRI
S0
S1
S2
S5
S9
S0

DATAPATH


IR
IR 0-8
IR 0-5
SE 9-16
SE 6-16
000
111
IR 3-5
IR 6-8
IR 9-11
R7
RF
A1
A2
A3
D1
D2
D3
IN
OUT
T1
T2
T3
LS1
LS7
0
1
A
B
ALU
CY
Z
MEM_A
MEM
MEM_D
MEM_D(I)

CONTROL WORD

There are 28 control inputs needeed for the microprocessor.

Bit No.	Name	Use
27	PC EN	Enables R7 direct transfer
26	IR EN	Enables IR storage and read
25	MW	Enables data input to memory
24	MR	Enables data output from memory
23	ALU EN	Enables ALU
22	RW EN	Enables Register write
21	T3 EN	Enables T3 read/write
20	T2 EN	Enables T2 read/write
19	T1 EN	Enables T1 read/write
18,17	ALU OP	Tells ALU, operation to do
16	LS1	Decides on whether to shift T1 o/p
15,14	A	Decides input to ALU_A
13	B	Decides input to ALU_B
12	T2	Decides input to T2
11	D3	Decides input to RF_D3
10,9	A3	Decides input to RF_A3
8	A2	Decides input to RFA2
7	A1	Decides input to RF_A1
6,5	IR	Decides input to IR
4,3,2	NUM	Chooses a 3-bit number for LM/SM operation to A3/A2
1,0	MEM	Decides input to memory address

VHDL IMPLEMENTATION

The VHDL Code and Implementation can be found in this Github Repo