IC fabrication process and characterization

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***Abstract*— In this project we study the various steps of the DIMES-01 process in the fabrication of a bipolar transistor. The project is divided in three parts. First the simulation is done which includes process and device simulations. Next the processing steps of the fabrication of bipolar transistor are done. Finally the measurements of the fabricated bipolar transistor are made to determine the performance of the transistor.**

I. Technology Assignments

1. *Assignment*

The oxidation rate of silicon can be calculated using the Deal-Grove model, which implies a first order, homogenous, separable, nonlinear differential equation for the oxide thickness.

$$\frac{dx}{dt} = \frac{B}{2x + A} \tag{1}$$

Let us assume the following initial value and boundary conditions.

$$x(t = t_0) = x_0;\ t_0 = 0 \tag{2}$$

Since $A, B > 0;\ x, x_0 \geq 0$, we can rewrite the equation in the following form:

$$(2x + A)\frac{dx}{dt} = B \tag{3}$$

$$\frac{d}{dt}(x^2 + Ax) = B \tag{4}$$

Integrating both sides gives

$$[x^2 + Ax]_0^t = [B]_0^t \tag{5}$$

$$x^2 - x_0^2 + A(x - x_0) = Bt \tag{6}$$

$$\frac{x^2 - x_0^2 + A(x - x_0)}{B} = t \tag{7}$$

a. *First oxidation thickness*

The task is to find the function which satisfies $x = h(x_0, t)$.

$$x^2 + Ax = x_0^2 + Ax_0 + Bt \tag{8}$$

$$f(x) = g(x_0, t);\ x = h(x_0, t) = f^{-1}g(x_0, t) \tag{9}$$

$$dom(f) = [0, \infty]; ran(f) = [0, \infty] \Longrightarrow$$

$$f^{-1}(y) = \frac{-A + \sqrt{A^2 + 4y}}{2}, (y > 0) \tag{10}$$

$$x = h(x_0, t) = \frac{-A + \sqrt{A^2 + 4\left(x_0^2 + Ax_0 + Bt\right)}}{2} \tag{11}$$

In the first step, the initial oxide thickness can be assumed to be zero. This is not true, since there is always a thin oxide layer on the surface of a silicon wafer. The oxide is, however, only a few nanometres thin.

We are going to use the $\{hr, \mu m\}$ unit system. The values of the parameters A and B and the elapsed time are the following:

$$B = 0.553;\ A = \frac{B}{3.1695} = 0.174;\ \Delta t = 0.641 \tag{12}$$

If we assume $10\ nm$ initial oxide thickness, the following values can be calculated:

$$x_0^2 = 10^{-4};\ Ax_0 = 1.74 \cdot 10^{-3};\ B\Delta t = 0.354 \tag{13}$$

The calculations show that we are in the 1% error range if we assume that no oxide is present in the beginning. The oxide thickness after the first oxidation then is

$$x_1 = h(0, \Delta t) = \frac{-A + \sqrt{A^2 + 4B\Delta t}}{2} \tag{14}$$

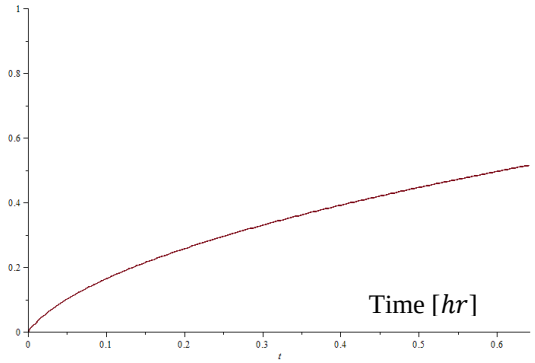


Fig 1. Oxide thickness versus time of oxidation

The calculated value for x after the first oxidation:

$$x_1 = 0.514\mu m \quad (15)$$

b. Second oxidation thickness

The second oxidation can be calculated with zero initial thickness and $2\Delta t$ time, or x_1 initial thickness and Δt time. The former is simpler, and we arrive at the value of

$$x_2 = 0.759\mu m \quad (16)$$

c. Step depth

The first oxidation process does not contribute to the step as it leaves the wafer flat. The second oxidation contributes with the consumed silicon:

$$\boldsymbol{h} = 0.455(x_2 - x_1) = 0.111\mu m \quad (17)$$

2. Assignment 2

a. Dirt barrier

Ion implantation is a low temperature process for the introduction of dopants into the semiconductor. A beam of dopant ions is accelerated to a high energy and is directed at the surface of the semiconductor. As the ions enter the silicon, they collide with the silicon atoms, lose their energy and come to rest at some depth within the crystal. Depending on the crystal orientation, there are channels in the silicon wafer where no Si atoms are present. The Si atoms in these directions below the surface are lined up exactly behind the ones at the surface. Due to these channels the incoming ions experience less scattering and they will penetrate much deeper than expected. In figure 2-a the ions A) do not collide with the lattice, will have less scattering and travel through the channel much deeper in the lattice whereas the ions in B) and C) will experience scattering in the crystal lattice of the silicon and stop at a certain, smaller depth.

It becomes difficult to model the channelled ion distribution with the channelling depth, also called as the 'channeling tail' being more than that of the expected depth of the ions implanted as shown in figure 2-b. Hence channelling must be prevented to make sure the implantation profile is similar to that of an isotropic material.

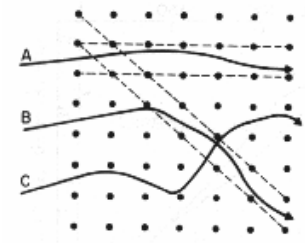


Fig 2-a.Scattering of ions and channeling

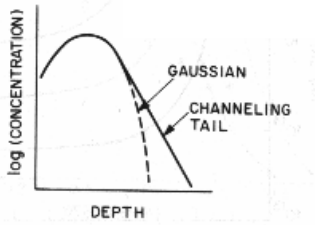


Fig 2-b.Influence on doping profile

One of the ways of minimizing the channelling effect is by deposition of a thin film screen oxide which is amorphous e.g. SiO_2 as shown in figure 2-c. This causes some randomization of incident beam by scattering the ions before they enter the crystal. This layer is called 'Dirt barrier'.

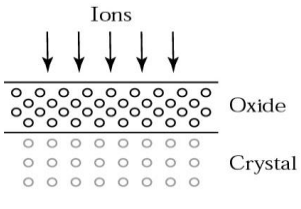


Fig 2-c Thin film of amorphous film SiO_2

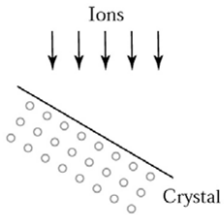


Fig 2-d.Typical tilt on wafer

In the DIMES01 process, before the ion implantation steps a thin layer of silicon oxide of about 21nm (BN step) is made by briefly oxidizing the silicon in the open windows formed after the removal of photo-resist.

b. Channeling prevention

The methods to minimize the channeling in the Ion implantation step are described below.

1. Changing the angle of ion implantation

In this method the wafer is tilted by an angle of 7˚ relative to the incoming ion beam to give the appearance of a random target. This tilted wafer is then rotated by 22˚ along the vertical axis with respect to the standard position (usually found by aligning the 'flat' of the wafer). Figure 2-d and 2-e shows the typical tilted wafer and the crystal orientation to the incoming ion beam. With this arrangement, the incoming ion beam sees the material as amorphous, resulting in better collision with the lattice, preventing channeling and achieving the desired dopant profile as per the calculated ion implantation.

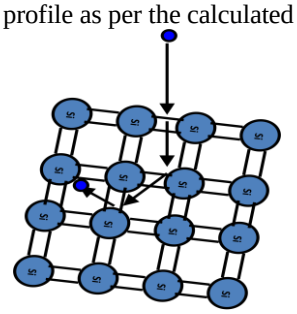


Fig 2-d.Effect of tilt wafer

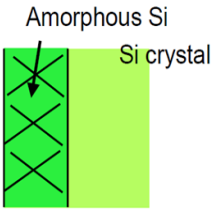


Fig 2-e. Amorphous Silicon on wafer

2. Amorphizing the Silicon surface

In this method, before the ion implantation process, the surface of the silicon is converted into amorphous silicon by implanting high dose of larger ions such as Si+. The amorphous nature of the surface of the silicon minimizes the channeling as there is no crystalline structure when compared to the silicon crystal underneath. Figure 2-e shows the deposition of amorphous Si layer above the silicon crystal and the direction of the ion implantation.

3. Deposition of thin layer of amorphous Silicon

In this method, a thin layer of amorphous film of SiO_2 will be deposited to form a dirt barrier to scatter the ions before they enter the crystal as described in figure 2-c assignment 2a.

The general distribution of dopant ions implanted in silicon is shown in the below for the dopants Antimony, Arsenic, Phosphorus and Boron.

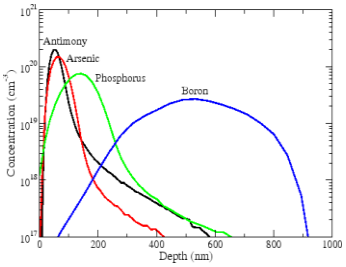


Fig 2-f Dopant distribution

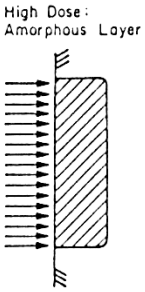


Fig 2-g Amorphizing by high ion-dose

Heavy ions like Antimony, Arsenic do not travel as deep in the crystal as the boron ions. If different ions are implanted with the same energy, the heavy ions stop at smaller depth but boron would have a large penetration depth. If the channeling is not prevented, boron would have a very large effect on the projected and real depth profile. Hence prevention of channeling becomes most critical in case of boron ions.

c. Amorphous implantation in SN step.

In the Emitter implantation step (SN) we need a high doped n-type region in the windows for emitter after the photo resist mask is patterned. Hence in this step a high dose of Arsenic with $5x10^{15}$ ions/cm^2 at 150keV is implanted using ion implantation process. Due to such heavy dose the implant damages the crystal structure and turns the silicon from crystalline into amorphous. Thus an amorphous layer is formed at the surface of the implantation as shown in Figure 2-g .This layer also prevents the effect of channeling during ion implantation.

3. *Assignment 3*

The three ways to incorporate dopant atoms into silicon are discussed below.

a. Diffusion

Diffusion is a thermal process that is used extensively in IC fabrication process. Diffusion is the process by which specific types of dopant or impurity atoms can be introduced into the silicon material. This doping process changes the conductivity type of the silicon so that p-n junctions can be formed. The selection of the areas in the substrate where the dopants need to be diffused is done using photolithography and etching. After this, the silicon wafers are placed in a high temperature furnace of about 1100˚C temperature and the dopant such as boron or phosphorus are added. The dopant atoms gradually diffuse or move into the silicon due to a density gradient. Since diffusion process requires gradient in the concentration of atoms, the distribtuion of diffused atoms is nonlinear. When the wafer is removed from the furnace the wafer temperature returns to room temperature and the diffusion coefficient of the dopant atoms is nearly zero so that the dopant atoms are fixed in the silicon material. There are two common situations in diffusion namely

a). Limited source diffusion in which a fixed number of dopants is supplied to the silicon that results in Gaussian distribution given by equation (**Error! Reference source not found.**).

$$C(x,t) = \frac{Qo}{\sqrt{\pi Dt}} * e^{\frac{x2}{4Dt}} \quad (18)$$

As the Dt product increases, the diffusion front moves more deeply into the wafer and the surface concentration decreases. The dopant profile in limited source diffusion is shown in figure 3-a

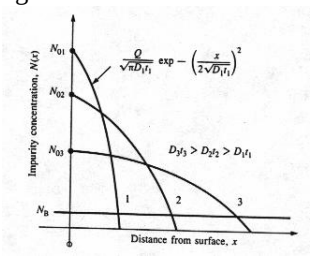


Fig 3-a Limited source diffusion profile.

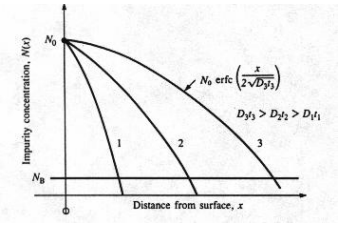


Fig 3-b Constant source diffusion profile

b). Constant-source diffusion or constant surface concentration is done by applying the dopant to the silicon through a dopant oxide. An oxide full of dopants is deposited on the surface and it diffuses through the silicon with time. The diffusion follow as per the equation **Error! Reference source not found.**.The surface concentration Cs remains constant and the diffusion moves deeper into the silicon wafer as Dt product increases. Dt can change as a result of increasing diffusion time, increasing diffusion temperature, or a combination of both.

$$C(x,t) = Cs * erfc(\frac{x}{\sqrt{\pi Dt}}) \quad (19)$$

The diffusion coefficient is temperature dependent. It increases with temperature. For the standard dopants in silicon such as boron, antimony, arsenic and phosphorus, the diffusion co-efficient is practically zero for temperatures below 600˚C.

b. Ion Implantation

A fabrication process that is an alternative to high temperature diffusion and is dominant in modern IC technologies is ion implantation. The setup of the ion implantation process is shown in Fig 3-c

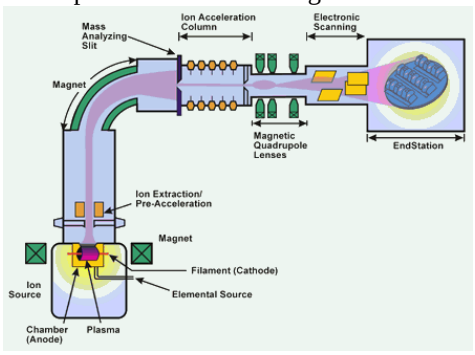


Fig 3-c Operating set up of Ion Implantation process

A beam of dopant ions such as As, P, Sb (n-type) or B (p-type) is accelerated to a high energy in an electric field. These are led through a magnetic field to get mass and charge separation. These pure beams of ions are further accelerated and will bombard the silicon surface. As the ions enter the substrate, they collide with the silicon atoms, lose energy and finally come to rest at some depth of penetration of the dopant ions.

The dopant distribution in the silicon depends on the amount of ions that hit the wafer and the energy of the ions. The advantages of ion implantation over diffusion is that the ion implantation process is a low temperature process and also very well defined doping layers can be achieved, compared to diffusion process. Photo resist layers or layers of oxide can be used to block the penetration of dopant atoms so that ion implantation can occur in the selected regions of the silicon only. The disadvantage of ion implantation is that the silicon crystal is damaged by the penetrating dopant atoms because of collisions between the incident dopant and host silicon atoms. Because of this, the wafer needs to be heated up as an extra step to regain its crystal structure. The effect of channeling as described in assignment -2a is one of the disadvantages of ion implantation.

c. Doping using alloy or Solid source Diffusion

In solid-source diffusion or doping using alloy, the Si surface is first coated with a thin film (of a SiGe alloy, for example) .The semiconductor substrate is then heated to diffuse at least some of the dopant from the silicon-germanium alloy into the semiconductor substrate to form a doped region at the face of the semiconductor substrate. The doped silicon-germanium alloy acts as a diffusion source for the dopant, so shallow-doped regions may be formed at the face of the semiconductor substrate without ion implantation. The SiGe film can be removed by wet etching.

4. Assignment 4

In the standard, integrated, vertical BJT structure, the principle current flow for normal operation is through the sink, buried layer and up through the vertical npn structure. The current across the emitter base junction and the collector base junction flows in the direction normal to the base surface. The cross section of the vertical bipolar transistor fabricated is shown in figure 4-a.

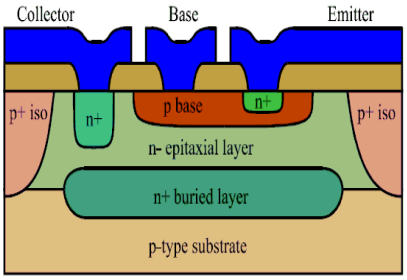


Fig 4-a Vertical fabricated Bipolar transistor

In lateral bipolar transistor structure the current flow across the base is in the direction parallel to the wafer surface. The base diffusions placed in a common tank. One of the diffusion serves as the emitter while the other diffusion serves as the collector as shown in figure 4-b. The lateral transistor has slower switching speed and current gain (beta) than the vertical transistor. The actual base width is difficult to determine because it depends on the two-dimensional current flow. The emitter injection efficiency suffers from the use of relatively lightly doped base diffusion as the emitter. Only the base width and collector efficiency can be controlled by the designer. The standard bipolar lateral device suffers from elevated recombination rates due to the use of (111) silicon structure. Hence lateral devices have lesser performance than the vertical fabricated devices.

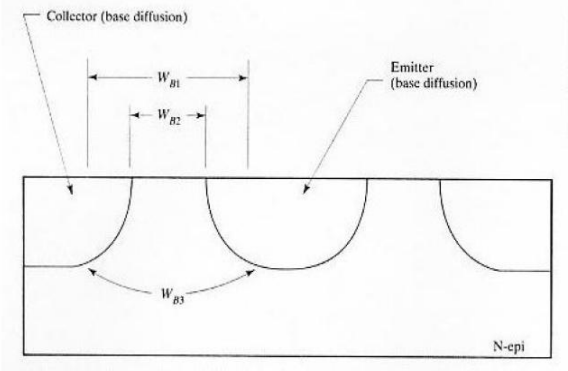


Fig 4-b Lateral fabricated Bipolar transistor

5. Assignment 5

Given in the below figure 5-a are the masks used in the DIMES fabrication process.

(Images to be scanned)

The order of the processing are described below -

1. Mask 5 – (Isolation diffusion) DP is the first mask which is used to isolate the transistor from the neighbouring transistor. A p-type region completely surrounding the transistor and in contact with the p-substrate is fabricated.
2. Mask 2 – (Collector plug) DN is the second mask. The buried layer is needed to make contact with the actual collector of the transistor. A deep N-type diffusion is performed using the DN mask.
3. Mask 4 – (Intrinsic base implantation) BS, BI, CI is the next mask. The p-type intrinsic base region is created by implantation with boron at 150keV.

4. Mask 3 – (Contact openings) CO is the next mask to be used. This mask is used to give information about the positions where the contact has to be made to the structure.
5. Mask 1 – (Aluminum etching) IC is the next mask to be used. This mask is used to give information about the positions where the contact has to be made to the structure.

6. Assignment 6

Given in the below figure 6-a are the doping profile in the DIMES01 fabrication process steps.
(Images to be scanned)

There are two regions on the graph. The one on the right hand side is a low p doping, and a large n doping (n++). The p doping is uniform throughout all the substrate. The n doping is made for the buried layer. Then an n-type epitaxy of Si follows over the substrate. The buried layer is necessary in order to decrease the collector resistance, but it is not possible to make high doping in that depth using a single wafer, since that would make further p-type doping of the base impossible.That is the reason why epitaxy is needed. The doping profile reflects the state of the wafer when collector plug has been opened (DN).

II. SIMULATION

a. Process Simulation

The process simulation determines the doping profile in the wafer as a function of the next process steps such as ion implantation and diffusion. The process simulations done are one dimensional as they calculate the doping profile in the vertical direction. The process simulations are done using the software TSUPREM-4. A one-dimensional grid is constructed and at each node the dopant material concentration is calculated.

The process simulation steps and results are described as follows

1. Implantation

In this step the three implants, arsenic, antimony and boron are chosen with the same dose but different energies. The figure 7.1 shows the dopant distribution of As, B and Sb.

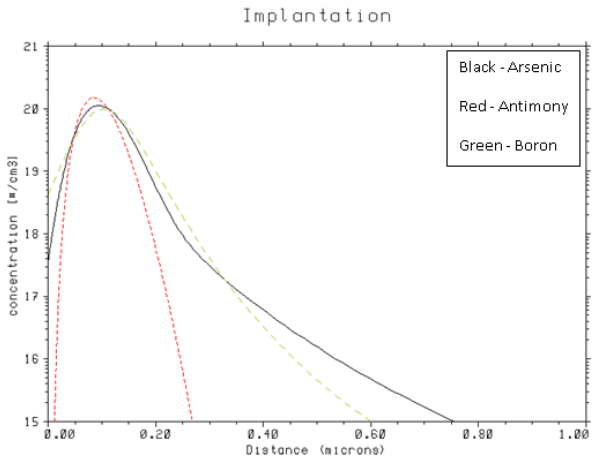


Fig.7.1 Dopant distribution of As, B, Sb in Silicon

Question 3.

In the above graph the dopant concentration is the same in all cases but the energies are chosen differently, in such a way that the projected range of penetration is the same. Ideally, the distribution of the dopant atoms in the silicon is in first order Gaussian-shaped. In our case we see some channeling tails for Arsenic and Boron, which make them not perfect Gaussian-shaped. Antimony, on the other hand is the one that resembles the Gaussian-shaped distribution the most. The order of the dopants in terms of width (straggle) in a descending row is as follows: Arsenic > Boron > Antimony. Arsenic has the largest straggle in the profile due to its ion-steering effect. The incoming beam is not parallel to the channels of the silicon lattice, but the Arsenic ions are guided towards channeling directions and thus they propagate further in Silicon. In the case of other ion types, the channeling effects make their presence stronger in lighter ions. Boron is lighter than Antimony; therefore, the width of its tail is greater.

Question 4.

If we want to implant Phosphorus to the same depth then we should find the energy needed first. By observing Fig.7.1 and knowing the atomic masses of the four ions, we can easily understand that the depth of Phosphorus will be among that of Boron and Antimony and a graph is shown in Fig 7.2 that represents the energies of the dopant ions with respect to their atomic masses:

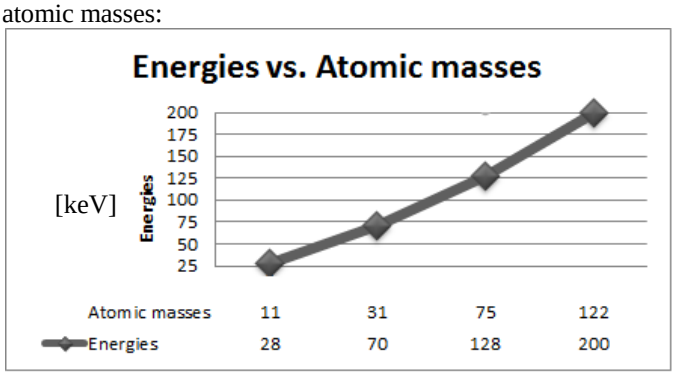


Fig.7.2 Energies vs. Atomic masses

70kEV is a very suitable for value for Phosphorus's energy as we can see from the graph above. Furthermore, by adding an implant for Phosphorus in Fig.7.3 we get the following graph:

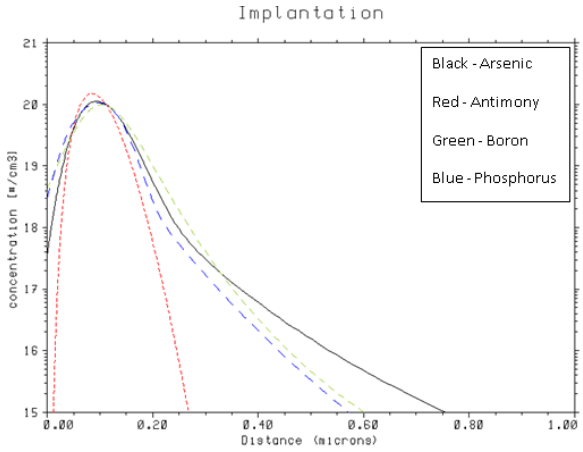


Fig.7.3 Dopant Distribution with phosphorus

In this figure we can see that our prediction was right about the depth of the Phosphorus, which lies among Antimony and Boron. Its distribution also shows channeling tail, which deviates from the Gaussian-shape.

Question 5.

Next we run a Monte Carlo simulation for amorphous Silicon and we get the following plot in the figure 7.4 for the distribution of the dopant atoms:

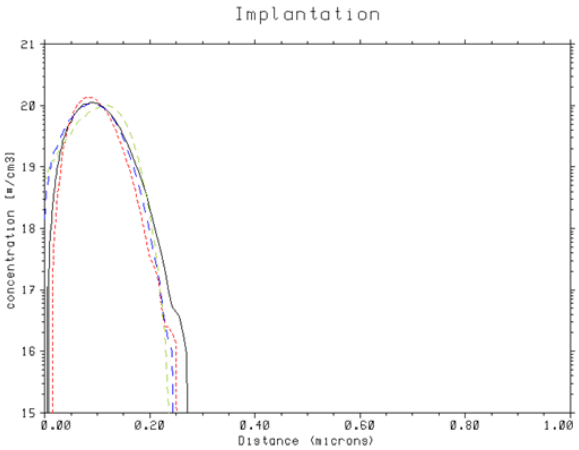


Fig.7.4 Distributions in a-Si

As we can see, the implantation profiles of all the dopants are almost Gaussian this time. The reason for this is that the amorphous Silicon has no crystal structure and therefore there are no channels formed to creating channeling tales. The channeling effect is not present. The result of this is that there is no straggle in the profiles and their shape is almost perfectly Gaussian.

Question 6.

Now, we run channelPh1.sup, channelPh2.sup and channelPh3.sup where in the following graphs the effect of channeling is shown:

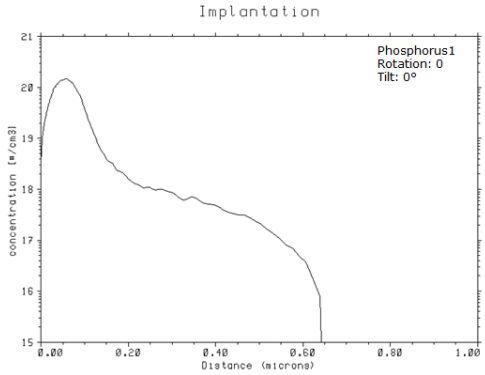


Fig.7.5 Ph1

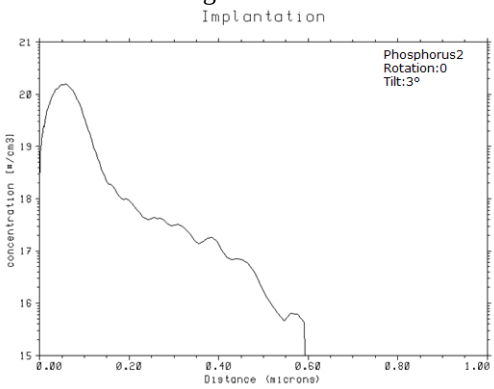


Fig.7.6 Ph2

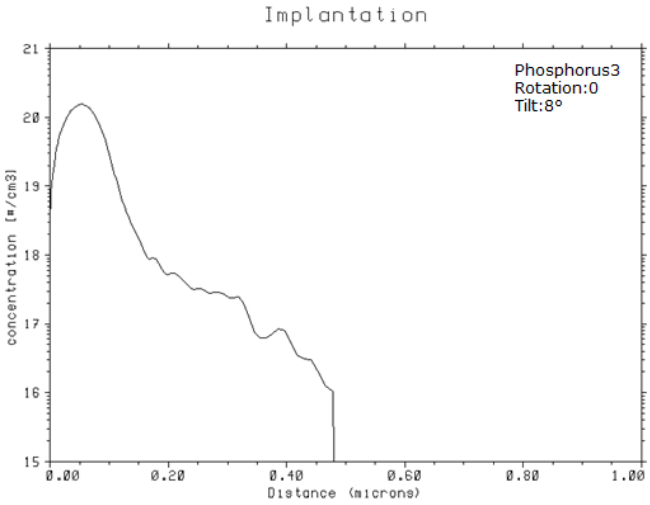


Fig.7.7 Ph3

Question 7.

Figures 7.5, 7.6 and 7.7 show how tilting the wafer modifies the doping profile. It is visible that the more the angle deviates from 90 degrees, the less channels can be used by the dopant atoms for channeling, and the tail decreases. This one method described in Assignment 2b for reducing channeling. Therefore, we can control the width of the dopant atoms by changing the tilting angle and the change in the width is inversely proportional to the tilting angle.

Question 8.

The following graph shows the implantation in amorphous silicon at 1000°C for 5 hours:

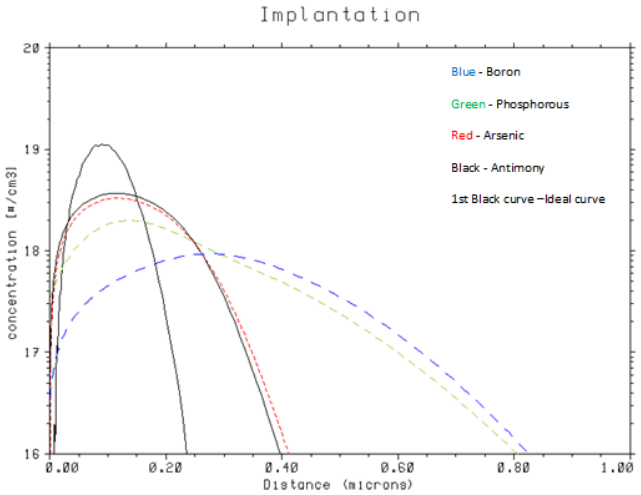


Fig.7.8 Implantation & Diffusion for 5 hours

The dopants in a descending order of diffusion profile widths are given as follows:
Boron > **Phosphorus** > **Arsenic** > **Antimony**. The misfit factor gives the effective radius of the dopant atoms in the Silicon lattice and the formula defining it is the following,

$$\boldsymbol{Reffective} = \frac{R_{dopant} - R_{silicon}}{R_{silicon}} \qquad (19)$$

As we can see from the table in page 7 in the course manual, the smaller the misfit factor of a dopant, the bigger the width the dopant achieves inside Silicon and the bigger the diffusion tail also. The order of the dopants regarding their misfit factors, therefore, is the same as the one we wrote before about their diffusion profiles.

Question 9.
In the next two graphs (Fig.7.9, Fig.7.10) we see an implantation and a diffusion of 60 minutes at 1000°C. In the second case, we have lowered the dose by a factor of 10.

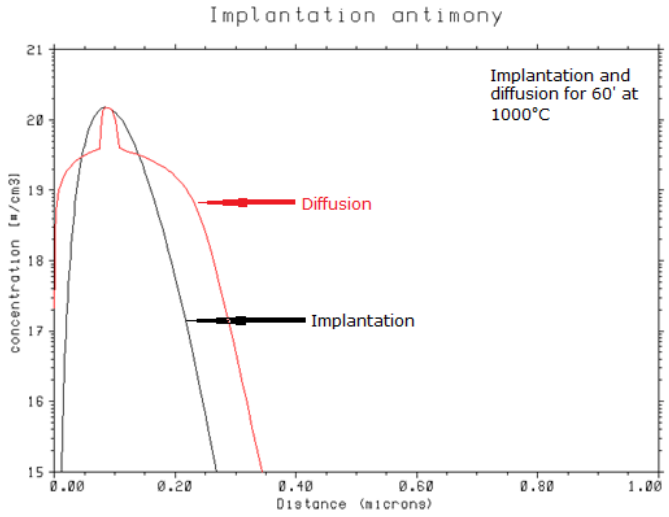


Fig.7.9

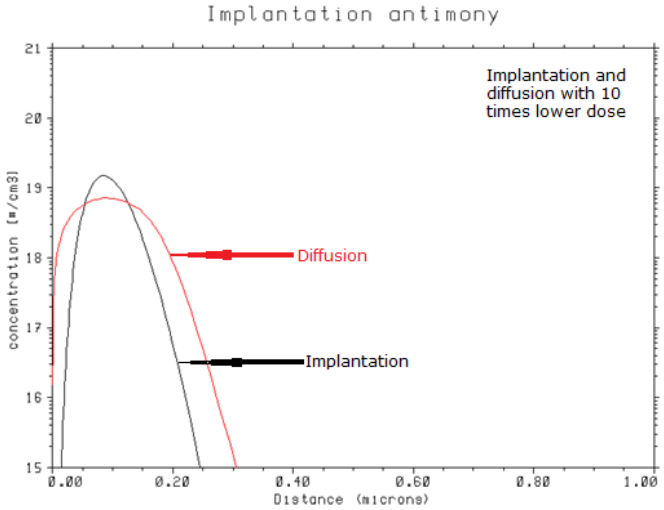


Fig.7.10

In the first case, we see that the implantation profile reaches a higher peak than that in the second case. Therefore, by lowering the dose concentration the peak of the implantation profile also gets lowered. As for the diffusion, in the first case we observe approximately in the same depth as the peak of the implantation. This can be explained in terms of the solid solubility. Since the maximum value has been reached, the excess atoms form clusters inside the lattice, or even driven out of it and give this peak. When we lower the dose, we don't observe this extra peak anymore, because with the given number of dopant atoms the maximum solid solubility is not yet reached and therefore, no excess atoms exist to form the cluster. It results in a smoother shape.

Question 10.

From the experiments preformed, we have observed the following values:

Dopant	Implant Straggle	Diffusion tail	Solid Solubility
Sb	4 (shortest)	4	1 (least)
As	1	3	4
P	3	2	3
B	2	1 (deepest)	2

Table 1.1

Question 11

For an emitter we need a high concentration and a rather sharp profile. High concentration means that the material should have high solubility. Furthermore, it should be n-type as it is the emitter of an npn transistor, and the sharp profile means a rather small diffusion tail. The material that is best fulfills the needs of these requirements is ***Arsenic,*** chosen based on the data of the table above. In the second case, we need to contact a buried layer (n-type) with a long tail and a high concentration material. Therefore, by the same arguments as before, we can easily understand that the best material for the job is ***Phosphorus***.

Question 12

Now, we will do implantation through various masking layers and judge their ability of masking the underlying Silicon against the implantation. The following picture is rather self-explanatory and shows implantation through a photo resist pattern with $0.4\mu m$ thickness.

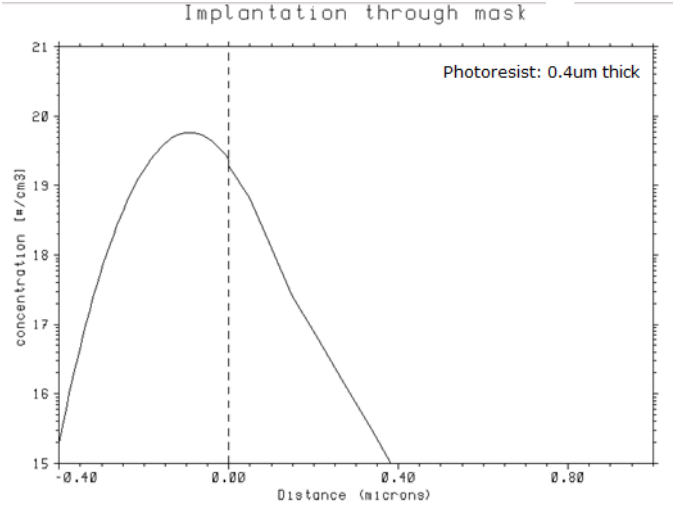


Fig.7.11 Implantation & Masking, photo resist 0.4um

Generally, a mask is considered good when only few ions pass through the mask to the material, in order not to cause damage to the structure that needs no doping. For the photo resist pattern of $0.4\mu m$ we can see that almost half of the dopant atoms pass through and damage the structure, therefore it is not considered a good mask. Furthermore, it cannot stand very high temperatures, which also creates a problem.

Question 13

In this case we make the photo resist $1\mu m$ thick instead of $0.4\mu m$ to enhance its ability to prevent dopant atoms from passing through and the graph below shows the implantation through this mask:

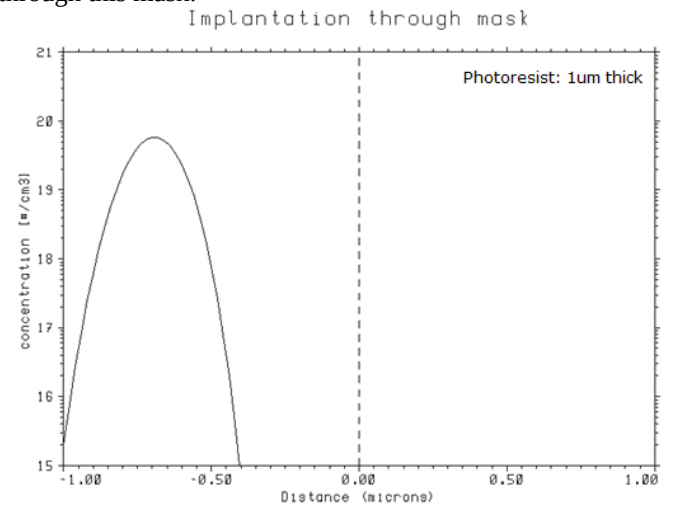


Fig.7.12 Implantation & Masking, photoresist 1um

We see that now no implanted atoms pass through the mask to the material. This makes it a good mask, but practically, again, the problem with the very high temperatures that the resist cannot stand makes its use limited as a mask.

Question 14

Next, we put silicon oxide and nitride as masks and the graphs below show their masking abilities respectively:

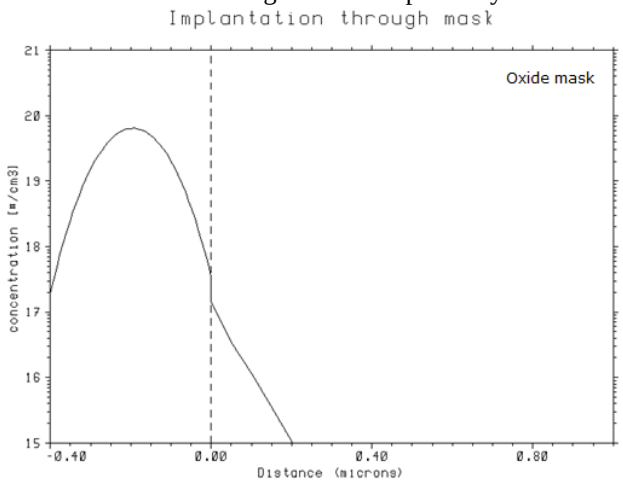


Fig.7.13 Implantation & Masking, oxide

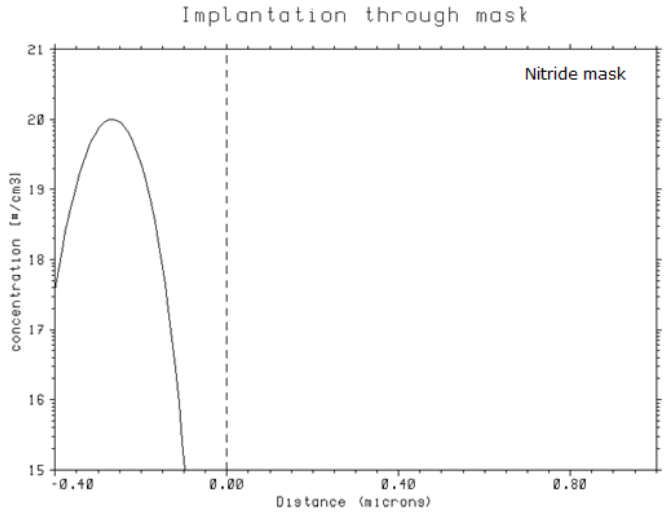


Fig.7.14 Implantation & Masking, Nitride

We observe that with the silicon oxide some dopant atoms pass through the mask to the material, but less than with the photoresist of $0.4\mu m$. Still, this is not considered as the best mask either. Another reason for the oxide's poor masking abilities is that we need high temperature to make it, which may influence the diffusion of the dopants in the Silicon. The nitride, on the other hand, makes a good mask, because no ions at all pass through it. This material is almost never used in standard processing though, because it cannot be removed easily. In order to remove it, hot phosphoric acid is used in a wet bath. Care has to be taken in order not to create many changes to the etch rate, which is very sensitive to changes in the concentration and the temperature of the acid.

Question 16

The relation between the DC current gain (β) and the dopant concentration in the base is given below:

$$\beta_F = \frac{I_C}{I_B} = \frac{J_C}{J_B} \approx \left(\frac{D_e^B L_h^E}{D_h^E w}\right)\left(\frac{N_D^E}{N_A^B}\right)$$

where N_A^B is the acceptor concentration in the base of an npn BJT. It is pretty straightforward that the gain is inversely proportional to the base concentration, therefore when the base concentration goes down, the current gain will go up. When the base concentration goes down, the base material becomes less p-type, the quasi-neutral base width becomes smaller and therefore more current can diffuse from the emitter to the collector through the base (I_C) resulting in a bigger current gain factor.

Question 17

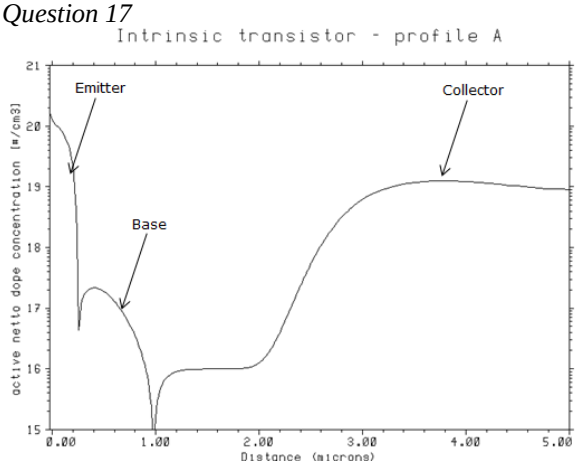


Fig.7.15 npn net doping profile

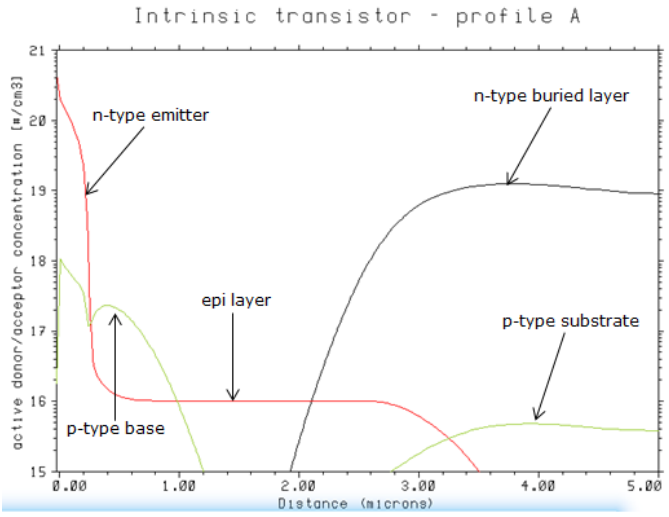


Fig.7.16 npn individual doping profile

Question 18

Figure 7.15 shows the combined doping profiles of the whole process, while Figure 7.16 shows the profiles of each individual step. As also annotated on the graphs, the substrate is represented by the green line on the right side of the second graph. The first step is the implantation of the buried layer. It is represented by the black line from the right of the graph. In the beginning, we implant the material and then we place it in high temperature in order to help the diffusion go deeper. Second, the epitaxial layer is grown, which is annotated in the second graph by the flat part of the red curve. Next, the emitter layer is implanted and is shown in the graph above as the vertical part of the red curve to the left of the schematic. The last part of the procedure is the implantation of the base, which is annotated as the green line on the left of the graph.

Question 19

As is also shown in Fig.7.16, the n-type dopants are distinguished from the p-type ones. The p-type dopants consist of the base and the substrate, whereas the emitter and the collector are the n-type dopants.

Question 20

In Fig.7.15 the emitter, base and collector are annotated and clearly shown

Question 21

From its definition, a junction is formed where the n-type dopant concentration is equal to the p-type dopant concentration. Therefore the junctions in Fig.7.15 are shown in the figure below:

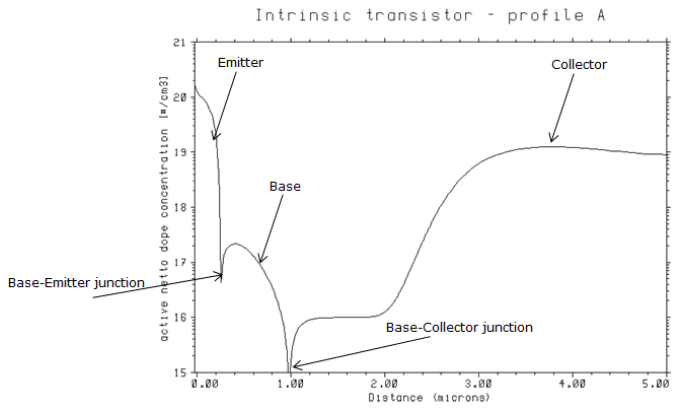


Fig.7.17 Annotation of Junctions

Question 22

As it is also annotated in Fig 7.16, the epitaxial layer is the flat red line. Originally, its depth is $4\mu m$. After its deposition, an extra p-type region is added in order to isolate the transistor from the neighboring transistors in the die. A constant source doping technique is used. The wafer is thermally oxidized and patterned with a mask. During the thermal oxidation process, part of the epitaxial layer is consumed by the oxidation. When SiO_2 is grown, part of the silicon is used to create it. Therefore, this is the reason why the epitaxial layer is seen smaller than its original depth.

Question 23

In Fig.7.15 we saw the so called net doping. This term is used to distinguish between the doping profile of each implantation process and the full doping profile after the whole procedure. The net doping profile gives us a cross section of the total doping profile after the whole doping process. In the x-axis we see the depth for which the concentrations are computed, where the zero corresponds to

the surface of the wafer. On the y-axis, the overall donor/acceptor concentrations are presented.

Question 24

Last, we run the A2.sup simulation, where we have increased the base dopant concentration to $4.5 \cdot 10^{13}/cm^3$. The graphs of the net doping profile and the individual doping profile are shown respectively below. The annotations in Fig.7.19 are the same as in Fig.7.16:

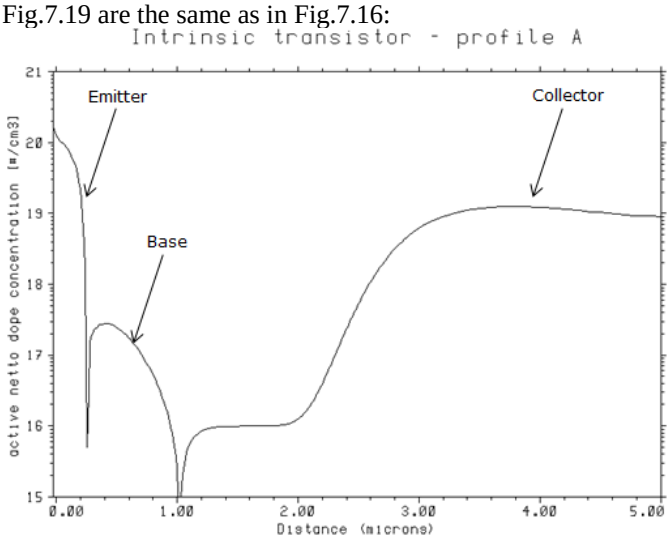


Fig.7.18 npn net doping profile, high base doping

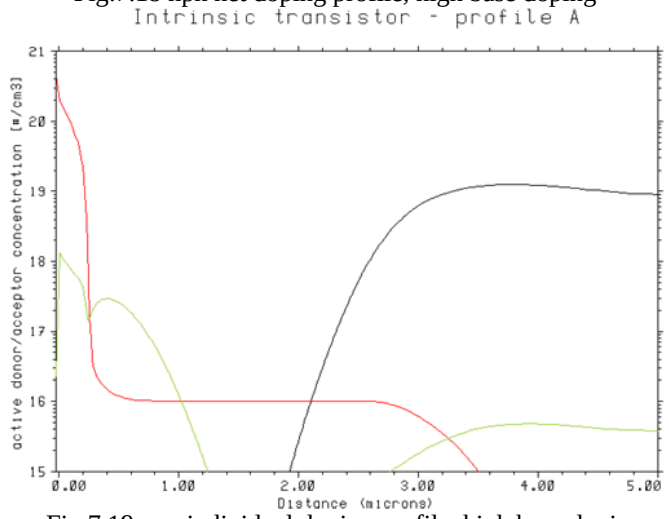


Fig.7.19 npn individual doping profile, high base doping

By a similar argument as in assignment 16, we understand that a higher dose in base would decrease the DC current gain. As we can see, though, there are some differences in the graphs obtained with the A1.sup simulation and the A2.sup simulation which support our previous argument. Theoretically, we would expect a bigger change, because the DC current gain changes significantly.

b. Device Simulation

Using the results of process simulation, it is possible to calculate the electrical characteristics of the BJT device to be fabricated. The program MEDICI was used.

Question 1

The grid generation is the first step in simulating the electrical properties of the device. The parameters like the electron or hole concentration and the electrical potential assigned to each point of the grid can then be used to solve the device equations numerically, with the finite element method. The output is the electric field and the current densities of the charge carriers.
The grids are generated automatically by the program. Their spacing is not uniform – in certain domains where the accuracy of the numerical method is critical, the grids are placed closer to one another, as it is visible in Figure 7.20.

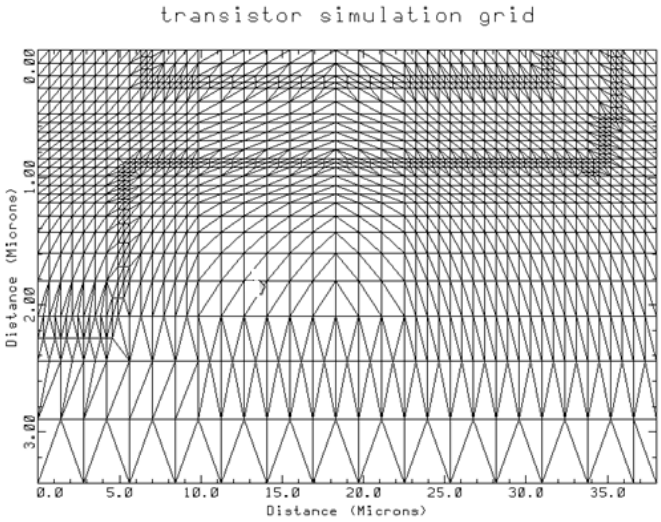


Fig. 7.20 Grid generation

It is visible that the corners of the – in contrast to the previous section, this time three-dimensional - doping profiles are much better covered by grid cells than the large planar parts. This is because the physical quantities change rapidly in these areas and accidentally overstepping the corners would introduce large errors. If the same would happen in a low-gradient area, the error would be within the limit.

Question 2

The Gummel plot of the device can be generated by applying the numerical solver on the grid.

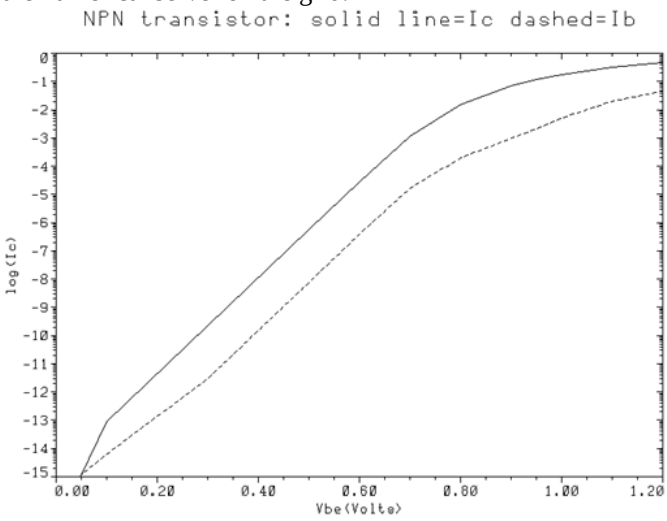


Fig. 7.21 Gummel plot

Question 3

The Gummel plot (Fig. 7.21) shows the collector and the base current versus the base-emitter voltage. It is linear in the x-axis, the voltage, and logarithmic in the y-axis, the currents. This is because there is an exponential relationship between them – that way, the graph ideally is linear. AT high currents, however, the collector and the base resistance limit the collector and the base current, respectfully. There the Gummel plot becomes linear. For low currents, the exponential relationship between base-emitter voltage and collector current is lost in the parasitic currents – namely, the recombination current. Thus, the relationship is no longer exponential for low currents as well.

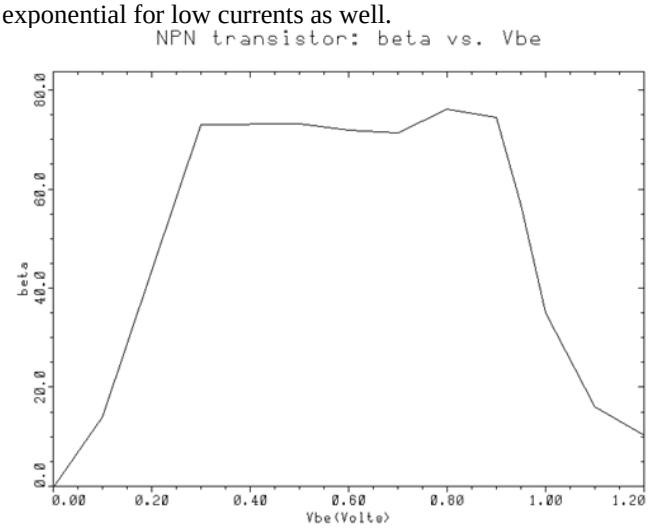


Fig. 7.22 Beta plot

The current gain, the ratio between the collector current and the base current is ideally constant, but also rapidly starts to change once the edge of the exponential region is reached, visible on the Fig. 7.22.

Question 4

The linear part has the following equation:

$$I_C = I_{s0}\left(e^{\frac{V_{BE}}{V_t}} - 1\right)$$

$$\frac{\log_{10}\frac{I_C}{I_{s0}}}{V_{BE}} \cong \frac{\log_{10} e}{V_t} = 16.76\ \frac{dec}{V}$$

$$\frac{1}{16.76\ \frac{dec}{V}} = 59.66\ \frac{mV}{dec}$$

Question 5

The gain can be read from the plot in Fig. 7.22. The exponential region has a gain of 73.

Question 6

The obtained plots can be seen at Fig 7.23. and 7.24.

Question 7

At Fig 7.23, the electron current is visibly flowing in the n-type collector and emitter, as the majority charge carriers are electrons in n-type materials. The collector current is an electron current. At Fig. 7.24, the hole current is the primary current in the base, injected from the base contact of the device. They flow along the base and partly recombine with the electrons injected from the emitter.

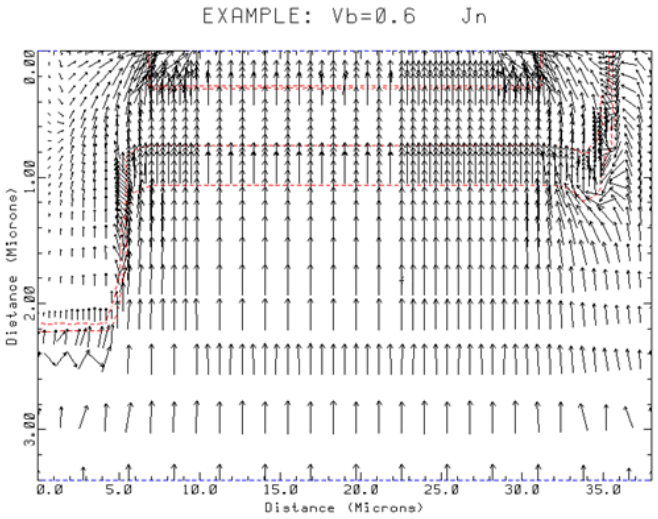


Fig. 7.23 Electron current density

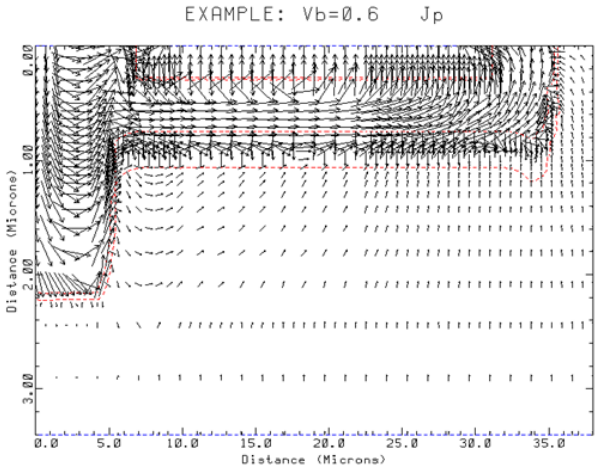


Fig. 7.24 Hole current density

Question 8

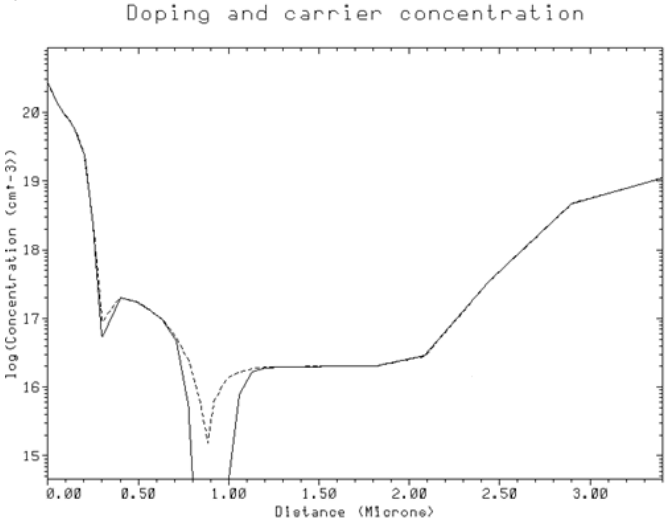


Fig. 7.25 Dopant and carrier concentration

At Fig. 7.25, the dotted line marks the dopant concentration, while the solid line shows the actual carrier concentration. The major difference is that at the base-collector junction, the concentration drops to zero as the BC junction is in reverse bias, and a depletion layer is present.

Question 9

Fig 7.26 shows the equipotential lines of the device. The denser the lines are, the larger the gradient in the electric field, and higher the voltage is. The BE junction has smaller amount of lines than the BC junction. The former has less lines, which corresponds to a smaller voltage. Indeed, the base-emitter voltage is usually below 0.7-0.8 Volts. The base-collector junction, however, contains plenty of lines which means high voltage drop. Also, they are spread over a wide area – that area represents the space charge or depletion region of the BC junction. The collector-base voltage is usually much higher than the base-emitter voltage.

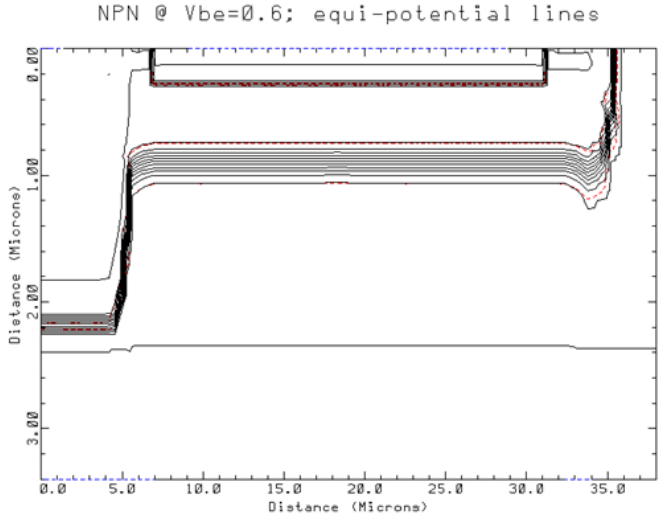


Fig. 7.26 Equipotential curves

Question 10

The second device has increased base doping, and the prediction of ours was that this decreases the gain of the transistor.

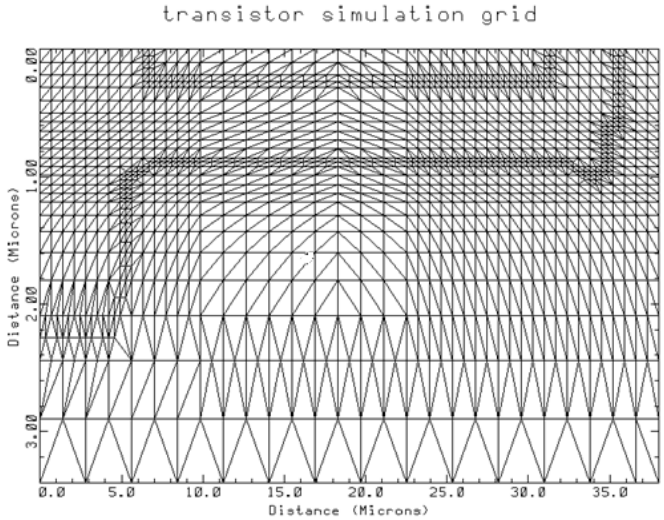


Fig. 7.27 Grid generation

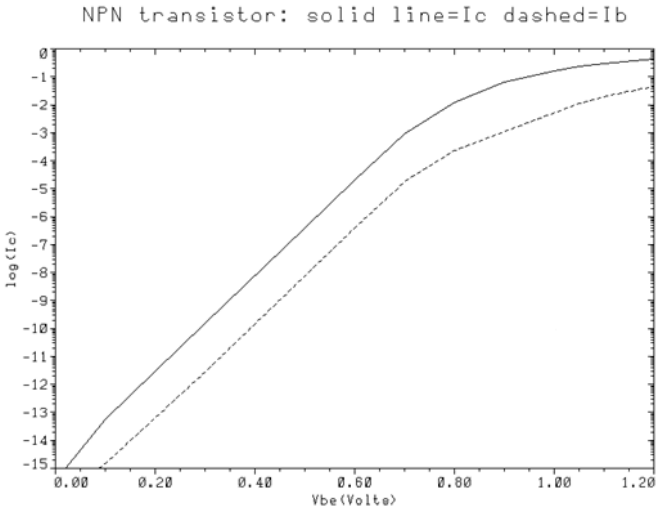


Fig. 7.28 Gummel plot

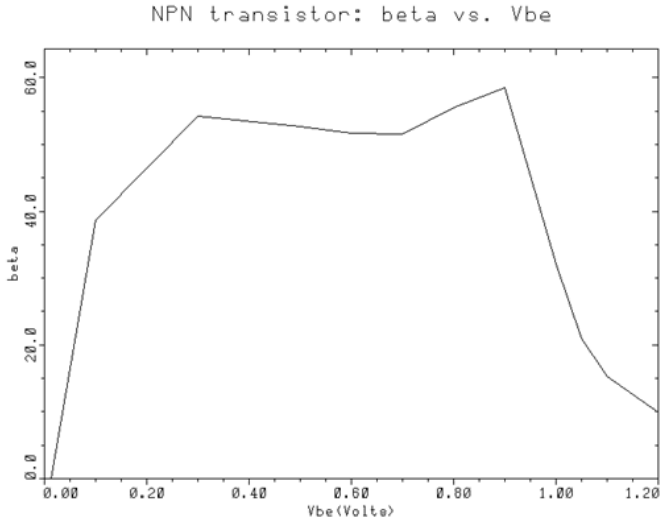


Fig. 7.29 Beta plot

Indeed, as it was expected, the current gain has decreased from 73 to the value of about 53, visible on Fig. 7.29. Our prediction was correct.

III. Processing

The wafer obtained is a processed wafer done up to the aluminium layer as per the DIMES process steps. The processing is done in a Class 100 Clean room. In the experiments nine processing steps are performed and the results are noted down. The steps are described as follows.

1. Cleaning

The start wafer in the experiment is first cleaned in 100% nitric acid (HNO3) for ten minutes. This is then rinsed in demineralised water. The resistivity of the bath gives the measure of cleanliness. In our experiment the cleaning was done in a water bath having resistivity of about 5MΩ for five minutes. The wafer is then dried on a high speed drying chamber at 3000rpm for about one minute. The objective of

this cleaning process is to remove all the organic matter present on the wafer.

2. HMDS treatment and Coating of photo resist on EVG120

The wafer after cleaning is placed a HMDS (hexa-methyl-disilazane) vapour to make it hydrophobic. After rinsing with de-mineralised water OH groups formed at the wafer surface makes it polar and thus hydrophilic. This improves better adhesion for the photo resist. The following reactions take place during exposure to HMDS.

$2SiOH + [(CH_3)_3Si]_2NH_2 \rightarrow 2SiOSi(CH_3)_3 + NH_3 \uparrow$ (20)

Silicon HMDS

The steps include wafer in HMDS vapour at 130˚C proximity, then it is cooled done to room temperature and taken to the next step that will be to apply the photo resist. The coating of the photo resist step is done in the 'yellow room' in the clean room since the photo resist layer is light and UV-light sensitive and hence it has to be filtered out. A positive photo resist is applied on the wafer by placing it in a vacuum chamber and applying liquid in the centre of the wafer. The lab conditions and the set up for the photo resist on EVG 120 is noted down as per the below table.

Method	Coat and Bake on EVG120
Temperature	21.2 ˚ C
Relative Humidity(RH)	0.462
Photo resist thickness	1.4 um
Program	CO_Edge_3012_1.4um
Baking time	90 - 95 s

A photo resist of 1.4um thickness is obtained after the coating process. After the coating the solvent is evaporated by a pre-bake at 95˚C proximity.

3. Mask IC Alignment and Exposure

The alignment and exposure of the wafer is done in two ways: with a contact aligner or a wafer stepper (PAS5500/80 ASML Stepper). In our experiment manually operated contact aligner was used. A mask with full wafer pattern of all the 52 dies is used. Each side of the wafer has alignment marks that are also present on the mask. This has to be aligned very accurately since any mis-alignment will cause the photo resist to be removed and the process has to be repeated. The mask is pressed on the wafer and exposed to a mercury based UV light having the wavelength less than 500nm. The mask is exposed to UV light for about 25 seconds. The exposed part of the photo resist will be changed chemically and will become slightly acidic.

4. Development on EVG120

The wafer is immersed in a solution of TMAOH in the EVG120 machine. The exposed part of the photo resist film will dissolve. The wafer is then cleaned by rinsing process.
The program and time used for development is shown below

Program	SP (Single Puddle)
Time	57 s

A Post exposure bake is performed for 1 minute at 115˚C to harden the photo resist and provide good adhesion to the surface. The wafer is cooled down to room temperature.

5. Visual Inspection on Microscope

A visual inspection is done on high resolution microscope to check the alignment by looking at the contact openings at the various devices.

6. Measurement

In the measurement steps we will be first measuring the oxide thickness using SP reflectometer. The oxide thickness is first measured before etching and then later measured after dry and wet etching. In the reflectometer, when the wafer is exposed to light, the light will reflect from the surface but it also partly goes through the oxide layer and reflects from the silicon- silicon oxide interface. The two reflecting beams will interfere and will have a destructive interference depending on the wavelength of light and the thickness of the oxide film.
The thickness is given by,

$$d = \frac{\lambda 1 * \lambda 2}{2 * (\lambda 1 - \lambda 2)} \quad (21)$$

First the oxide thickness is measured without etching. Then the wafer is placed for two types of etching – Wet etching and dry etching. The results of the measurement experiment are shown in below table.

Question 5.

Oxide thickness before etching	**Oxide thickness after dry etching**	**Oxide thickness after wet etching**
dox = 270.6 nm	dox = 260.74 nm	dox = 270.02 nm

From the above table it is seen that the oxide thickness remains almost same before etching and after etching in the case of wet etching process around 270nm. But after dry etching process (plasma etching) it is seen that the oxide thickness before and after etching is reducing to 260nm. About 10nm of oxide is also being etched after plasma etching process.

7. Etching process

After the photo resist pattern is formed, the remaining photo resist can be used as a mask so that the material is not covered by the photo resist can be etched. The two types of etching are dry etching or plasma etching and wet etching.

a. Dry etching or plasma etching

In plasma etching an etch gas such as chlorofluorocarbons are injected into a low pressure chamber. Plasma is created by applying radio-frequency voltage between the anode and cathode terminals. The silicon wafer is placed on the cathode. Positively charged ions in the plasma are accelerated toward the cathode and bombard the wafer normal to the surface. The net result is that the silicon is etched anisotrophically in much selected regions of the wafer. If a photo resist is applied on the

surface of silicon di-oxide, then the silicon di-oxide can also be etched away. In this process there is almost no under-etching and aluminium lines will be similar as the mask. In our experiment plasma etching was done on Trikon Omega plasma etcher. The etching is done for Aluminium with 1% silicon.

Program	Al06_350
Temperature	25 ˚ C
Inspection	Good

Question 6, 8, and 9,10.

For the measurement of the line width we consider the width of the letter 'I' in the DIMES logo in the wafer. The inspection and results of the line width of plasma etching is described below,

Before Dry Etching			After Dry Etching		
X1(um)	**X2(um)**	**Width (um)**	**X1 (um)**	**X2 (um)**	**Width (um)**
76.463	76.432	0.031	83.867	83.837	0.030

The width before and after dry etching is almost constant of about 0.030um.

b. Wet Etching

Wet Etching is an etching process that utilizes liquid chemicals or etchants to remove materials from the wafer, usually in specific patterns defined by photo resist masks on the wafer. Materials not covered by these masks are 'etched away' by the chemicals while those covered by the masks are left almost intact. A simple wet etching process may just consist of dissolution of the material to be removed in a liquid solvent, without changing the chemical nature of the dissolved material. In our experiment the wafer is immersed for one minute in a demi-water with soap solution to lower the surface tension in order to improve the etching. The wafer is immersed in phosphoric acid solution at 35˚C.After sometime the bare aluminium is completely etched visible by the colour change from shiny to gray. The wafer is then cleaned in demi-water and inspected in the microscope. We observe that due to the presence of 1% silicon on aluminium, there are small grains of silicon on the surface even after rinsing. These will be removed in a HNO3-HF solution for duration of 30 seconds. This is called as Poly silicon dip etching. Wet etching is isotropic process.

Question 6, 7,9,10.

Program	Al Etch_35˚
Temperature	35 ˚ C
Time	5 minutes 32 seconds
Inspection	Not Good Silicon participates

In the above process, grains of silicon are observed on the surface of Aluminum. To remove this, the next processing step called Poly-silicon dip etching is performed.

Program	Poly Silicon Etching
Time	30s
Inspection	Good - No Silicon participates

After the above step, the grains of silicon on the aluminum surface are not seen.

The measurement of the line width is done similar to the plasma etching by considering the letter width of the letter I in the DIMES logo in the wafer. The inspection and results of the line width of plasma etching is described below,

Before Wet Etching			After Wet Etching		
X1(um)	**X2(um)**	**Width (um)**	**X1 (um)**	**X2 (um)**	**Width (um)**
95.598	95.576	0.022	86.045	86.015	0.030

The width of the letter I in the DIMES logo before and after wet etching is not constant. It is seen that the width has increased to **8nm**. This is because wet etching is isotropic process and it etches in all directions with the same speed .Due to this it will etch a little underneath the resist window.

Although wet etching is cheaper it has the disadvantage of etching underneath the photo resist. This is not the case in case of plasma etching or dry etching which is anisotropic and does not cause photo resist adhesion problems.

Plasma etching process has high selectivity when compared to wet etching process.

8. Epi Doping concentration calculations

In doping concentration measurement, we calculate the sheet resistance by four point measurement, calculate the epi layer thickness using the bevel method and finally calculate the doping concentration using the Irving – curve. The measurements and results of the above methods are described below.

a. Epi surface concentration measurement.

Sheet resistivity: The sheet resistance is a measure of resistance of thin films that are nominally uniform in thickness. It is commonly used to characterise materials made from semiconductor doping. Consider a block as shown in figure 8.1 having length 'l' and width 'w'. Let the specific resistivity of this block be ρ .

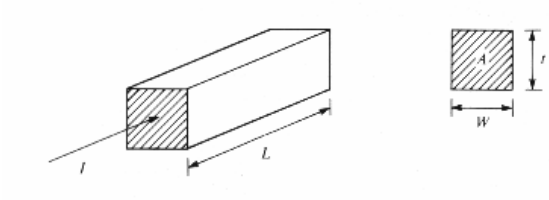


Fig.8.1 A block of material with width w and length l

The resistance of this block is given by the equation below.

$$R = \frac{\rho}{t} \cdot \frac{l}{w} = R_s . \frac{l}{w} \qquad (22)$$

In the above equation R_s is called as the sheet resistance. For an implanted or diffused layer with a given thickness a designer can make a resistor by making an area of length 'l'

and width ‘w’. The resistance ‘R’ is then the number of squares that fit in the length l. Hence the layer will have a sheet resistance of R_sΩ/square. In our experiment we use four

Method	Four point Measurement
Program	DI 01 _ Epi
Sheet Resistence R_s	1298 +/- 8 Ω/square

point probe measurement to the sheet résistance of the given sample. A four point probe is used to avoid contact resistance, which can often be the same magnitude as the sheet resistance. Typically a constant current is applied to two probes and the potential on the other two probes is measured with a high impedance voltmeter as shown in figure 8.1.

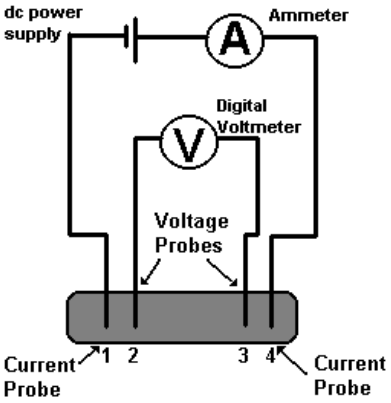


Fig.8.2 Four probe measurement set up.

Question 1.
The process and the sheet resistance obtained using the above setup is described below;

b. Epi layer junction depth calculation using Bevel method.

The junction depth (measured from the surface of the plane) in a p-n junction is the point at which concentration of acceptors is equal to concentration of the donor atoms i.e., $N_a = N_d$. In our experiment the junction depth is measured using Bevel method. In this process the wafer is subjected to mechanical abrasion to expose the junction for viewing. Here a hole is grinded by a steel ball (with radius R) in the silicon through the junction. Then with copper sulphate, the n type area is coloured under the influence of strong light. Under the microscope we measure the ring dimension and calculate the thickness. The measurement that is required for junction depth calculation is shown in the figure 8.3

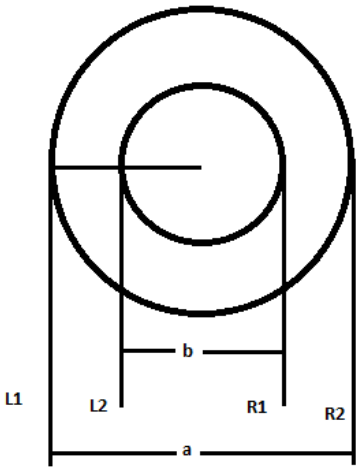


Fig.8.3 Junction depth measurement using bevel method
The measurement of a and b was obtained from the values of L1, L2, R1 and R2 using the microscope. The junction depth is calculated using the below formula,

$$x_j = \sqrt{R^2 - \frac{b^2}{4}} - \sqrt{R^2 - \frac{a^2}{4}} \quad (23)$$

Question 2.
The values obtained from the experiment are shown below

L1 (mm)	L2(mm)	R1 (mm)	R2(mm)
77.184	77.058	75.655	75.53

The Epi layer junction depth is calculated as **3.84um**.

c. Epi Doping concentration using Irving curve.
The 4- point probe and bevel method are used to determine the sheet résistance R_s and junction depth x_j respectively. In order to find the doping concentration N_o of the dopant atoms in a layer we utilise the relation between the junction depth, sheet resistance and background concentration N_B using Irving curves. The dopant profile (erfc or half Gaussian) can be uniquely determined if one knows the concentration at two depth positions.
Question 3.
In our experiment, we use the above described method of calculation and the doping concentration
No = 9.4 x 10^15 atom /cc

Layer	N-type epitaxy layer
Doping concentration – No	9.4 x 10^15 atom /cc

IV. DEVICE CHARACTERIZATION

The aim of the following measurements was to determine the electrical properties of the manufactured devices.

A. Effect of light

Light generates electron-hole pairs, which creates recombination current along the device. This current does not contribute to the transistor’s primary operation, it is a parasitic effect. The aim of this measurement was to determine how much does light degrade the transistor effect, how much does

the Gummel plot deviate from the theoretical first order model. To determine this, the logarithmic gain was calculated to be

$$I_C = I_{s0}\left(e^{\frac{V_{BE}}{V_t}} - 1\right) \tag{20}$$

$$\frac{\log_{10}\frac{I_C}{I_{s0}}}{V_{BE}} \cong \frac{\log_{10} e}{V_t} = 16.76\ \frac{1}{V} \tag{21}$$

$$I_{s0} = \frac{eD_n n_{p0}}{L_n} + \frac{eD_p p_{n0}}{L_p} \tag{24}$$

The exponential transfer characteristic of the bipolar transistor is linearized on the logarithmic scale. The ideal transistor's logarithmic transfer curve would be a straight line on the Gummel plot. Any deviation from that can be easily detected. There are few types of deviation. At low and high voltages, secondary effects become dominant, and the Gummel plot becomes nonlinear. The slope of the primary region can also deviate from the calculated value.

The recombination current can be calculated as

$$I_R = I_{r0} e^{\frac{V_{BE}}{2V_t}} \tag{25}$$

$$\frac{\log_{10}\frac{I_R}{I_{r0}}}{V_{BE}} \cong \frac{\log_{10} e}{2V_t} = 8.38\ \frac{1}{V} \tag{26}$$

$$I_{r0} = \frac{eWn_i}{2\tau_0} \tag{27}$$

The recombination current is half as steep on the Gummel plot. The point where the recombination current becomes dominant is

$$I_R = I_C \tag{28}$$

$$I_{s0} e^{\frac{V_{BE}}{V_t}} = I_{r0} e^{\frac{V_{BE}}{2V_t}} \tag{29}$$

$$\frac{\log_{10} \mathrm{e}}{2\mathrm{V_t}} \mathrm{V_{BE}} = \frac{\log_{10} \mathrm{e}}{\mathrm{V_t}} \mathrm{V_{BE}} + \log_{10} \frac{\mathrm{I_{s0}}}{\mathrm{I_{r0}}} \tag{30}$$

$$V_{BE} = 2V_t \ln \frac{I_{r0}(V_{BE})}{I_{s0}} \tag{31}$$

This is a transcendental equation as the recombination current depends on V_{BE} through the space charge region width W.

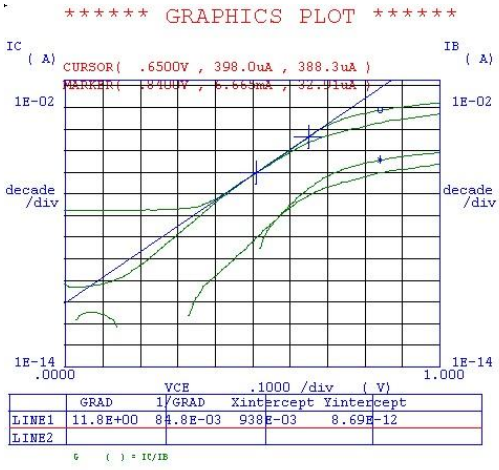


Figure I EFFECT OF LIGHT

The measured value in the presence of light was $11.8\ \frac{1}{V}$, which is lower than the theoretical value. The reason for this is that the recombination current becomes dominant for higher voltages as well than without light, which decreases the exponential current region of the transistor. For low bias voltages, the collector current is higher than without light, due to the larger recombination current. The base current visibly turns into a negative value which is marked as a discontinuation on the Gummel plot.

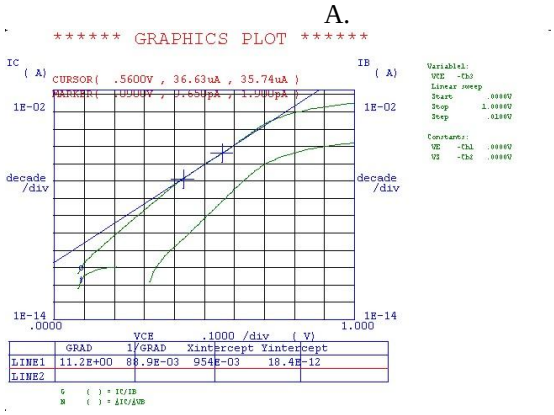
With the exclusion of light, one can read from the graph that the gain is $14.25\ \frac{1}{V}$, which is closer to the theoretical value.

B. Gain vs. Base Doping

The base doping is one factor that determines the current of a bipolar transistor via the saturation current I_{s0}. However, on a Gummel plot, it does not modify the slope of the current, since a linear multiplication is a logarithmic addition. It does modify, however, the point where the recombination current becomes dominant (equation (31)). We will see that for increased base doping, the recombination current becomes dominant for higher voltages.

1. *BS Low doping*

A.



B.

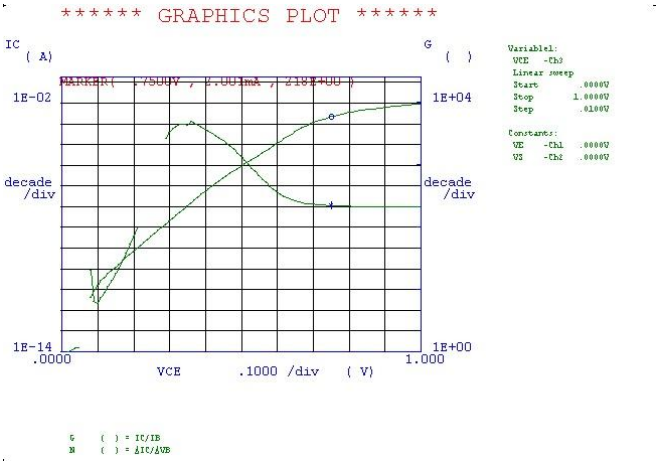
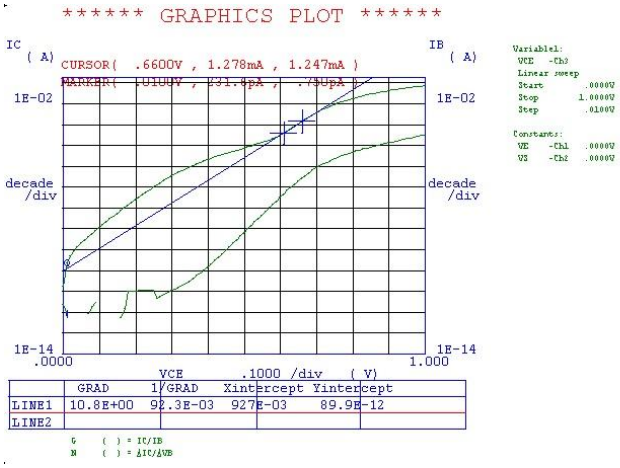


Figure II GUMMEL AND BETA PLOTS OF A LOW DOPED TRANSISTOR

As it is shown in Figure II/A, the recombination current remains low for a wide voltage range, and the Gummel plot is close to the ideal straight line. For low voltages, the current gain β increases as the base current rapidly decreases due to non-ideal effects, but otherwise remains close to a constant value (Figure II/B).

2. *BI Medium doping*

A.



B.

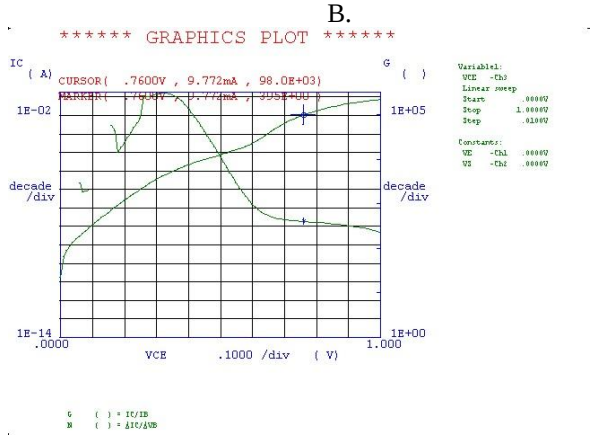


Figure III GUMMEL AND BETA PLOTS OF A MEDIUM DOPED TRANSISTOR

Due to medium base doping, the recombination current leaves a very small voltage range where the transistor is ideal. The current gain increases due to the increased recombination current.

3. *CI High doping*

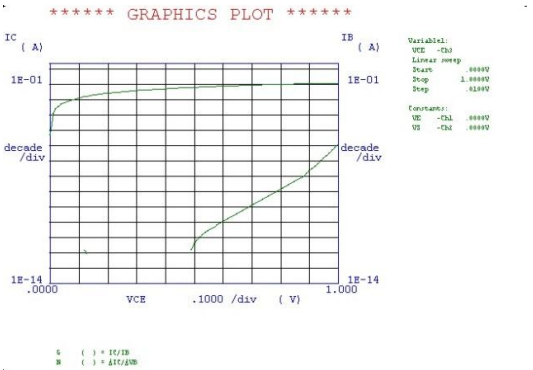


Figure IV GUMMEL AND BETA PLOTS OF A HIGHLY DOPED TRANSISTOR

At high base doping the transistor effect vanishes. The concentration of minority carriers at the base (n_{p0}) becomes very small and the electrons cannot pass the BE junction. The current gain hugely varies over the applied voltage, there is no single value which can be noted.

Table I: Transistor parameters vs. doping

	β_F	I_s	n_F
BS	218	18.4 pA	11.2
BI	305	89.9 pA	10.8
CI	–	–	1.3

4. *Effect of Series Resistance*

In the ideal model of a bipolar transistor, the finite resistances of the base and the collector were not taken into account. This is partially justified as the transistor action takes place in the relatively short base. However, the actual layout of a transistor inherently includes some considerable resistance, which is going to limit the collector current and the transfer characteristic becomes linear. To test this behaviour, one can by intention increase the base or collector resistance during manufacturing and evaluate their effect.

Normal resistance

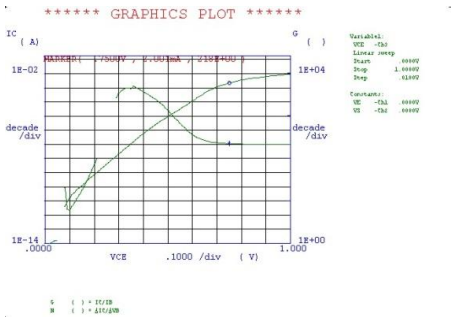


Figure V BETA PLOT OF A NORMAL RESISTANCE TRANSISTOR

5. *Rb, increased base resistance*

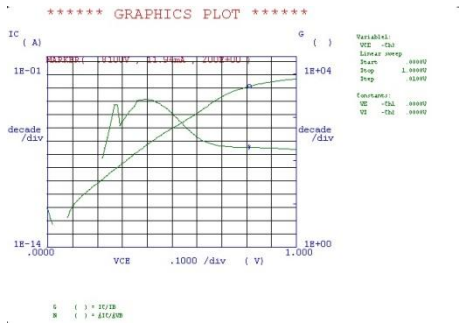


Figure VI BETA PLOT OF A LARGE BASE RESISTANCE TRANSISTOR

The increased base resistance is going to limit the base current by a negative feedback mechanism. The larger the base current becomes, the larger the voltage drop across the base resistance is going to be, decreasing the BE voltage, which in turn decreases the base current.

6. *Rc, increased collector resistance*

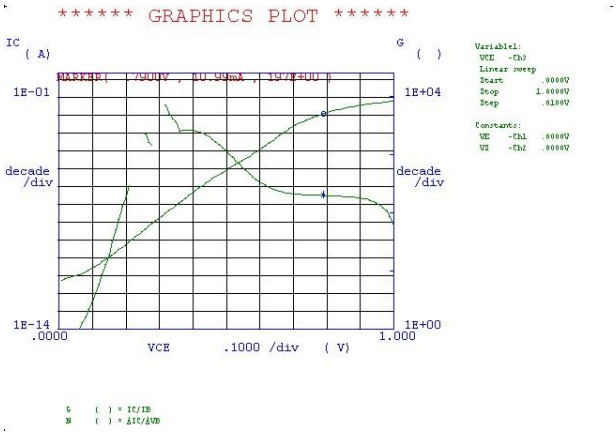


Figure VII BETA PLOT OF A LARGE COLLECTOR RESISTANCE TRANSISTOR

The increased collector resistance is going to have a similar effect. It is visible that for high voltages, the collector current is no longer exponential, and is closer to linear due to the collector resistance. The current gain factor drops heavily in that region, unlike the normal resistance transistor.

Table II: Transistor parameters vs. series resistance

	β_F	I_S	n_F
norm	218	18.4 pA	11.2
Rb	200	5.3 pA	11.7
Rc	197	10.2 pA	10.8

7. *Output characteristics*

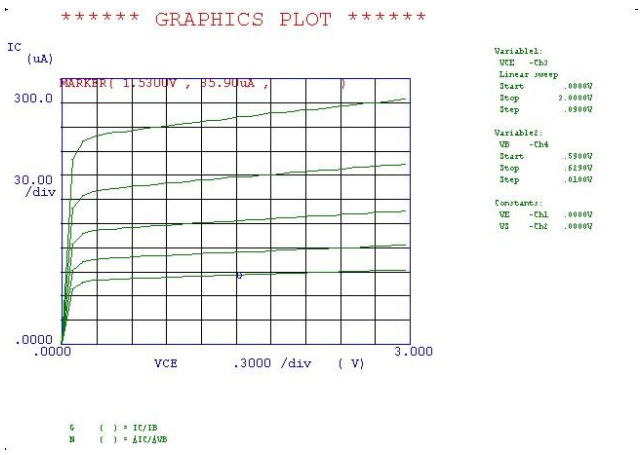
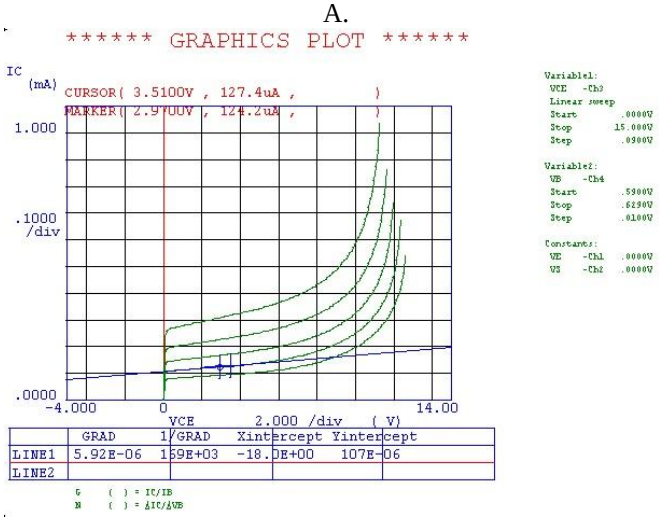


Figure VIII OUTPUT CHARACTERISITCS

8. *Early voltage*

Ideally, the output characteristic of the bipolar transistor in the forward active mode should be flat as the CE voltage does not have influence on the charge transport. However, due to the Early effect, the width of the base is not going to remain constant, but it varies with the BC voltage via the depletion region width at the BC junction. The linear interpolation of the branch of curves have a point where they meet – the voltage associated with the point is called the Early voltage. In an ideal device, the Early voltage is infinite.

A.



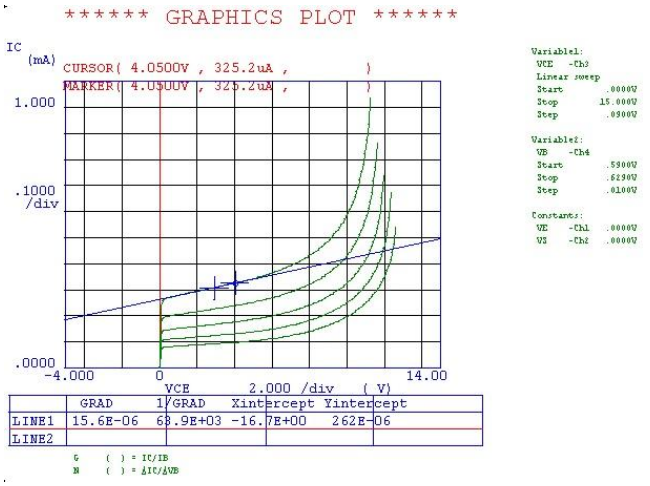


Figure IX GUMMEL AND BETA PLOTS OF A LOW DOPED TRANSISTOR

The Early voltage can be calculated from the crossing point. The curves match sufficiently and in accordance with the theory.

Table III: Early voltage from interpolation

	Upper branch	Lower branch	Average
Early Voltage	16.7 V	18 V	17.35 V

9. EC breakdown

An npn transistor has two junctions, which can be regarded as two diodes in reverse direction. The breakdown mechanism of diodes is well-known. There are two types of breakdown – avalanche breakdown and Zener breakdown. Figure X presents the avalanche breakdown of the EC junction. Avalanche breakdown occurs when large electric field accelerates electrons so that they kick out tied electrons in the substrate, which also get accelerated. This is and exponentially growing electron population multiplication.

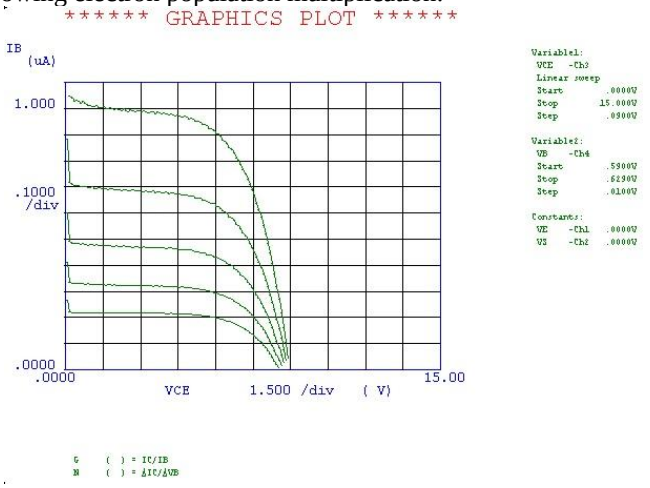


Figure X EC BREAKDOWN OF A TRANSISTOR

The measured breakdown voltage was $9V$, which is an expected value for the DIMES-01 process.

10. Van der Pauw measurement

The four-terminal resistance and the sheet resistance of a symmetric configuration can be related to each other in the following way

$$R_{\square} = \frac{\pi}{\ln 2} R_{AB,CD} \tag{32}$$

In practice, the four-terminal resistance can be easily measured through the four point probe measurement. We have measured several layers present in the DIMES-01 process, and calculated the sheet resistance.

Table IV: Four-terminal resistances of different layers

	$R_{AB,CD}[\Omega]$	$R_{\square}\ [\Omega/\square]$
BS	$1.39k$	$6.29k$
SP	5.2	23.55
SN	11	49.83
DP	1.88	8.51
DN	0.746	3.37
EPI	304	1377.12
BN	4	18.12

CALCULATION FROM SIM

Differential resistance measurement

Another way to measure the sheet resistance is the differential resistance measurement. Interpolating the data measured for different sample lengths and widths gives the value for the sheet resistance.

Table V: Differential resistances of different layers

		$SP\ [\Omega]$	$SN\ [\Omega]$
W	2 μm		
L	80 μm	746	$1.58k$
	320 μm	$3.01k$	$6.77k$
	480 μm	$4.52k$	$10.0k$
W	16 μm		
L	80 μm	119	250
	320 μm	474	$1.01k$
	480 μm	709	$1.51k$

In order to decrease the effect of lateral out diffusion, 16 μm wide samples are also measured. We will take them as reference and compare it with the 2 μm samples to determine the out diffusion.

Table VI: Resistivity of different layers

		$SP\ [\Omega/\mu m]$	$SN\ [\Omega/\mu m]$
W	16 μm		
L	80 μm	1.4875	3.125
	320 μm	1.48125	3.15625
	480 μm	1.477	3.1458
	Average	1.4823	3.14235
	$R_{\square}\ [\Omega/\square]$	23.71	50.27

The square resistances accurately match the results of the van der Pauw measurement. The lateral out diffusion can be calculated with the formula:

$$R_{2um} \cdot W = R_{16um} \cdot 16\ \mu m \tag{33}$$

$$d = \frac{1}{2}\left(\frac{R_{\square}}{R_{2um}} - 2\ \mu m\right) \tag{34}$$

Table VII: Resistivity of different layers

		$SP\ [\Omega/\mu m]$	$SN\ [\Omega/\mu m]$
W	$2\ \mu m$		
L	$80\ \mu m$	9.325	19.75
	$320\ \mu m$	9.40625	21.15
	$480\ \mu m$	9.41666	20.83
	Average	9.3826	20.5766
	d	$0.26\ \mu m$	$0.2215\ \mu m$

CONCLUSION

The Bipolar transistor fabricated from DIMES -01 process was studied. In the simulations, the process simulation was done using TSUPREM- 4 which gives us the doping profile in the wafer and the device simulation was done using MEDICI that gave us information about the performance of the device. In the processing step, we observed the difference in wet etching and dry etching. Various measurements such as thickness of the oxide, junction depth and sheet résistance of the processed wafer was reported. In the measurement step, the resistance, DC characteristic of the different structures of bipolar transistor in the wafer was measured to give us information about the device behavior.

ACKNOWLEDGMENT

We would like to thank the staff of DIMES for the guidance and giving us the opportunity to work in the DIMES clean room as part of the IC Technology course. It was a great learning experience for us to know about the process steps in fabrication of the bipolar transistor.

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