For a **UART (Universal Asynchronous Receiver/Transmitter) verification project**, interviewers expect you to think **protocol-wise, data-wise, timing-wise, and robustness-wise**. Below is a **complete, structured test-case checklist** you can directly map to **UVM sequences + assertions + coverage**.

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1. Basic Functional Test Cases

These confirm that UART works as per spec.

- **Reset behavior**
    - TX line idle (1) after reset
    - RX FSM resets correctly
    - Internal FIFOs/flags cleared
- **Basic transmit**
    - Single byte transmission
    - Back-to-back byte transmission
    - Idle line before and after transfer
- **Basic receive**
    - Correct sampling at mid-bit
    - Correct data reconstruction
    - Proper rx_done / interrupt generation

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2. Data Format Configurations

UART is highly configurable – this is critical.

- **Data length**
    - 5-bit, 6-bit, 7-bit, 8-bit data
- **Stop bits**
    - 1 stop bit
    - 1.5 stop bits

    - 2 stop bits
- **Parity**
    - No parity
    - Even parity
    - Odd parity
    - Parity bit generation & checking

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3. Baud Rate & Timing Tests

Very important for **asynchronous** protocol verification.

- **Baud rate configurations**
    - Minimum supported baud rate
    - Maximum supported baud rate
- **Baud mismatch tolerance**
    - TX slightly faster than RX
    - TX slightly slower than RX
- **Clock drift tests**
    - Gradual drift within tolerance
- **Oversampling logic**
    - Correct sampling at 8x / 16x oversampling
    - Mid-bit sampling verification

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4. Error Handling Test Cases (Must-have)

These show **verification maturity**.

- **Parity error**
    - Inject incorrect parity bit
- **Framing error**

    - Stop bit forced to 0
- **Overrun error**
    - RX FIFO full and new data arrives
- **Underrun error**
    - TX FIFO empty during transmit
- **Break condition**
    - RX held low for more than frame length

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5. Corner & Stress Test Cases

Interviewers love these.

- **Back-to-back frames with no idle gap**
- **Randomized data streams**
- **Long continuous transmission**
- **Maximum FIFO depth usage**
- **Simultaneous TX and RX**
- **Reset during active transmission**
- **Reset during reception**

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6. Interrupt & Status Tests (if applicable)

If UART has interrupts/status registers.

- **TX empty interrupt**
- **RX full interrupt**
- **Error interrupt**
- **Interrupt clear behavior**
- **Multiple interrupts simultaneously**

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7. Register-Level Test Cases (APB/AXI UART)

If UART is memory-mapped.

- **Register read/write**
- **Invalid address access**
- **Read-only / write-only enforcement**
- **Configuration changes during active transfer**
- **Register reset values**

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8. Assertions (SVA) – High-Value Checks

These strengthen your project.

- Start bit must be 0
- Stop bit must be 1
- No data change except at baud boundaries
- RX sample point at mid-bit
- No TX activity when disabled
- Error flags asserted only on valid error conditions

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9. Functional Coverage Points

Good coverage story = strong resume.

- All data widths × parity × stop-bit combinations
- All baud rate settings
- Each error type hit
- FIFO full/empty transitions
- Interrupt generation and clear paths

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10. Negative / Robustness Tests

Shows real-world thinking.

- Illegal configuration combinations
- Glitch on RX line
- Noise injection (single-cycle spike)
- Partial frame reception
- Power-on reset with RX low