MEA2100-256 User Guide

Interfaceboard Address Map (Address bits 11-0), Base Address: 0x0000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
0x000:																									0x	0e	= N	1EA	210	00-2	256
Device ID																									IF	В					
0x004:									HW	//Bo	ard \	Versi	ion				FPC	GA V	Versi	ion											
HW/FPGA																															
Version																															
0x008:																								Cy2_notCy1			CO)D I	Pins		
Configuration																															

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x010: GTP																															HS2	HS1
Status																															link	link
																															up	up
0x014:	erro	or co	unte	r HS	32												erro	or co	unte	r HS	51										•	
Error																																
counter																																
(RO)																																
0x014:	any	wri	te re	sets	the e	error	cou	nters																								
Error																																
counter																																
reset (WO)																																

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x020:																													-			Reset
Reset																																FPGA
0x024:																														HS2	HS1	IF
Power																														power	power	analog
enable																																
0x028:										HS	2 de	lay						HS	1 de	lay						IF	de	lay				•
Waveform																																
0x02c:																						LE	ED							LED E	IS 1/2 ar	nd IF
LED																						HS	S 1/	2								
																						an	d II	7								
																						reg	gist	er								
																						mo	ode									
																						en	abl	е								

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	,	6	5 4	4 3	2	1 (,
0x030: (WO)Flash Instruction Code																				<u> </u>				Fifo Reset	I	ns	truc	 ction	n Co	de		1
Register																																
0x030: (RO)Flash Status Register																						FIFO_empty	FIFO_full	Statemachine busy	F	Fla	sh S	Stat	us R	egis.	ter	
0x034: Flash Memory Address Register									Flas	sh A	ddre	SS													•							
0x038: Flash Data FIFO Register	250	6 Da	ta B	ytes	in 64	4 DV	Vord	s to/	from	Flas	sh																					
0x03c: Flash HW configuration Register	(1,	dres 2 or tes)		gth	Clo	ock E	Divid	ler R	egist	ter (N	Multi	ples	of 2	divi	ide 3	38.4	МН	Hz)														

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0f0: Lock																																Lock
other Cypress																																

Register	31 30	29	2	28 27	7 26	25	24	23	22	21	20	0 19	1	8	17	16	15	1	4 13	1	2 1	1	10	9	8	3 7	6	5 5	4	3	2	1	0
0x100: Trigger CTRL	Trigge	r upd	lat	e rate						l																						Trigger idle	Enable trigger
0x104: Trigger Configuration															Trig	ger	rise/	/fa	ıll ser	d se	epei	ate	;										
0x108: Trigger Status Config																			status ister r								_			lect	s h	eadstage	trigger
0x110: Set Trigger (Write)															Gen	erat	e tri	gg	ger ev	ent,	sel	f cl	ear	ing	; if	trig	ggeı	r ris	se/fa	all :	== '	'0'	
0x110: Trigger Event Monitor (Read)															Trig	ger	evei	nt	bits a	t ne	xt t	rigg	ger	pa	cke	et to) he	ads	stag	e			
0x114: Clear Trigger (Write)															Clea	r Tı	igge	er	status	s, or	ıly	who	en t	rig	ger	ris	se/fa	all	==	'1'			
0x114: Trigger Status Monitor (Read)															Trig	ger	statı	us	bits a	ıt ne	ext t	rig	ger	pa	cke	et to	o he	ead	stag	ge			
0x120: Trigger Armed															Arm	ed ((1 bi	it p	per tri	gge	er)												

0x124: Trigger Running		Running (1 bit per trigger)
0x140: Electrode/Segment ID Trigger 0	Segment/Trigger ID	Electrode config ID
0x141: Electrode/Segment ID Trigger 1	Segment/Trigger ID	Electrode config ID
0x142: Electrode/Segment ID Trigger 2	Segment/Trigger ID	Electrode config ID
0x143: Electrode/Segment ID Trigger 3	Segment/Trigger ID	Electrode config ID
0x144: Electrode/Segment ID Trigger 4	Segment/Trigger ID	Electrode config ID
0x145: Electrode/Segment ID Trigger 5	Segment/Trigger ID	Electrode config ID
0x146: Electrode/Segment ID Trigger 6	Segment/Trigger ID	Electrode config ID
0x147: Electrode/Segment ID Trigger 7	Segment/Trigger ID	Electrode config ID
0x148: Electrode/Segment ID Trigger 8	Segment/Trigger ID	Electrode config ID
0x149: Electrode/Segment ID Trigger 9	Segment/Trigger ID	Electrode config ID
0x14a: Electrode/Segment ID Trigger 10	Segment/Trigger ID	Electrode config ID
0x14b: Electrode/Segment ID Trigger 11	Segment/Trigger ID	Electrode config ID
0x14c: Electrode/Segment ID Trigger 12	Segment/Trigger ID	Electrode config ID
0x14d: Electrode/Segment ID Trigger 13	Segment/Trigger ID	Electrode config ID
0x14e: Electrode/Segment ID Trigger 14	Segment/Trigger ID	Electrode config ID
0x14f: Electrode/Segment ID Trigger 15	Segment/Trigger ID	Electrode config ID

0x150: Electrode/Segment ID Trigger 16	Segment/Trigger ID	Electrode config ID
0x151: Electrode/Segment ID Trigger 17	Segment/Trigger ID	Electrode config ID

Register	31 30	29	28	3 27	26	2	5 24	23	3 2	2 2	1	20	19	18	17	16	15		14 1	3	12	11	10)	9 8	3	7 6	5	5	4 3	3 2	1		0
0x200: Trigger CTRL	Trigger	upd	late	rate											l																	Trigg idle		Enable trigger
0x204: Trigger Configuration															Tr	igger	rise	e/f	all se	nd	sepe	era	te											
0x208: Trigger Status Config															1	elect t											_			efle	ets h	eadstag	ge tı	rigger
0x210: Set Trigger (Write)															Ge	enera	te tr	ig	ger e	ven	t, se	elf (clear	rin	g if	tri	ggeı	r ri	ise	/fall	==	'0'		
0x210: Trigger Event Monitor (Read)															Tr	igger	eve	ent	bits	at 1	next	tri	gger	· pa	acke	et t	o he	ad	lsta	ige				
0x214: Clear Trigger (Write)															Cl	ear T	rigg	ger	statı	1S, (only	w	hen	tri	gge	r ri	se/fa	all	==	= '1'				
0x214: Trigger Status Monitor (Read)															Tr	rigger	stat	tus	s bits	at 1	next	tri	ggeı	r pa	ack	et 1	o he	ead	lsta	age				
0x220: Trigger Armed															Aı	rmed	(1 b	oit	per t	rigg	ger)													
0x224: Trigger Running															Rı	unnin	g (1	b	it per	tri	ggei	:)												
0x240: Electrode/Segment ID Trigger 0								Se	egm	ent/T	rig	gger	ID		I												Elec	tro	ode	e co	nfig	ID		
0x241: Electrode/Segment ID Trigger 1								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	co	nfig	ID		
0x242: Electrode/Segment ID Trigger 2								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	co	nfig	ID		
0x243: Electrode/Segment ID Trigger 3								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	e co	nfig	ID		
0x244: Electrode/Segment ID Trigger 4								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	e co	nfig	ID		
0x245: Electrode/Segment ID Trigger 5								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	e co	nfig	ID		
0x246: Electrode/Segment ID Trigger 6								Se	egm	ent/T	rig	gger	ID														Elec	tro	ode	e co	nfig	ID		

0x247: Electrode/Segment ID Trigger 7	Segment/Trigger ID	Electrode config ID
0x248: Electrode/Segment ID Trigger 8	Segment/Trigger ID	Electrode config ID
0x249: Electrode/Segment ID Trigger 9	Segment/Trigger ID	Electrode config ID
0x24a: Electrode/Segment ID Trigger 10	Segment/Trigger ID	Electrode config ID
0x24b: Electrode/Segment ID Trigger 11	Segment/Trigger ID	Electrode config ID
0x24c: Electrode/Segment ID Trigger 12	Segment/Trigger ID	Electrode config ID
0x24d: Electrode/Segment ID Trigger 13	Segment/Trigger ID	Electrode config ID
0x24e: Electrode/Segment ID Trigger 14	Segment/Trigger ID	Electrode config ID
0x24f: Electrode/Segment ID Trigger 15	Segment/Trigger ID	Electrode config ID
0x250: Electrode/Segment ID Trigger 16	Segment/Trigger ID	Electrode config ID
0x251: Electrode/Segment ID Trigger 17	Segment/Trigger ID	Electrode config ID

Register	31	30	29	9 28	27	26	25	24	23 2	2 21	20) 19	18	17	16	15	14	1.	3 12	11	10	9	8	7	6	5	4	3	2	1	0
0x400: Digital single pulse	bits	can	or	nly be	set l	nere,	and v	will	be clea	red a	fter	the ti	ne d	efine	ed in	Dig	ital s	sing	gle pı	ilse c	lurat	ion 1	4						•	·	
0x404: Digital single pulse duration 1	Dui	ratio	n c	of Dig	gital I	Oata i	n mi	ultip	le of 2	0 us i	or F	ulse I	Regis	ster b	oits 0	to 7	7														
0x408: Digital single pulse duration 2	Dui	ratio	n c	of Dig	gital I	Oata i	n mı	ultip	le of 2	0 us 1	or F	ulse I	Regis	ster b	oits 8	to 1	15														
0x40c: Digital single pulse duration 3	Dui	ratio	n c	of Dig	gital I	Oata i	n mi	ultip	le of 2	0 us 1	or F	ulse I	Regis	ster b	oits 1	6 to	23														
0x410: Digital single pulse duration 4	Dui	ratio	n c	of Dig	gital I	Oata i	n mi	ultip	le of 2	0 us i	or F	ulse I	Regis	ster b	oits 2	4 to	31														

Mode* Pulse length Pulse lengt			
generator 1 periodic pulse generator 2 periodi 0x421 Digital periodic pulse generator 2 periodi 0x422 Digital periodic pulse generator 3 periodi 0x422 Digital periodic pulse generator 4 periodic pulse generator 4 periodic pulse generator 4 periodic pulse generator 5 periodic pulse generator 4 periodic pulse generator 6 periodic pulse generator 6 periodic pulse generator 6 periodic pulse generator 7 periodic pulse generator 7 periodic pulse generator 8 periodic pulse generator 9 periodic pulse generator 9 periodic pulse generator 9 periodic pulse generator 1 periodic pulse generator 9 periodic pulse genera		Sample period	
0x42t Digital periodic pulse generator 2			
Sample period pulse generator 2 period Sample period Sam	1		
periodic pulse generator 2 period 0x422; Digital periodic pulse generator 3 period 0x424; Digital periodic pulse generator 4 periodic pulse generator 5 length 0x425; Digital periodic pulse generator 6 length 0x426; Digital periodic pulse generator 7 length 0x427; Digital periodic pulse generator 8 length 0x427; Digital periodic pulse generator 9 length 0x428; Digital periodic pulse generator 1 length 0x427; Digital periodic pulse generator 2 length 0x428; Digital periodic pulse generator 2 length 0x429; Digital periodic pulse generator 2 length 0x429; Digital periodic pulse generator 4 length 0x429; Digital periodic pulse generator 4 length 0x429; Digital periodic pulse generator 4 length 0x429; Digital periodic pulse generator 3 length 9 lengt	period		
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0x42b: Digital periodic pulse generator 4 config 0x440: Digital stimulator clear write Digital IN bit select Channel (015)			
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generator 4 config 0x440: Digital stimulator clear write channel (015)		Mode.	
config 0x440: Digital stimulator clear write channel (015)			SCICCI
0x440: Digital stimulator clear write channel (015)			
stimulator clear write (015)			
clear write			
			(015)
pointer			
	pomer		

0x444: Digital stimulator		men	nory location		channel
channel memory select (WO)					
0x448: Digital Stimulator channel data (WO)	Append data to current selected channel (selected via Digital stin	nulat	or channel memory select register	3:0)	
0x448: Digital Stimulator channel data (RO)	Read data from selected channel (selected via Digital stimulator of	chanı	nel memory select register 3:0)		
0x44c: Digital Stimulator start slope	mask		slope (0: falling, 1: rising)		
0x450: Digital Stimulator stop slope	mask		slope (0: falling, 1: rising)		
0x454: Digital Stimulator global repeat			per channel 1 bit (0: single, 1: loop	p)	
0x480: Feedback data	Feedback data				
0x4a0: Data to Data Stream					
0x4a4: Mask for 'Digital Data-Stream'					
0x4b0: AUX data OUT					AUX data
0x4b4: AUX data IN					AUX data
0x4b8: AUX data direction					0: Input, 1: Output
0x4d0: Digital OUT port (RO)	Data				·
0x4d4: Digital IN port (RO)	Data				
0x4d8: Direction of digital port	1: Input, 0: Output				
0x4dc: Digital port interrupt enable	1: Interrupt enabled, affects only inputs, 0: Interrupt disabled				

*Mode:

Register	31 30 2	9 28 27	7 26 25	5 24 2	23 22	21 2	20 19 1	18 17	16 1	5 14 1	13 12	2 11 10	9	8	7	6	5	4	3	3 2	1	0
0x500: Digital data delay					,									1		'	Numb	per of s	weeps	to delay	the digi	tal data
0x504: Delay interface board data													Digital data register	Digital out stimulato	Digital pulse r generato	DACQ is running	in	Feedb	ack	Digital OUT	Digital IN	Digital MUX
0x510: Delay HS 1 trigger								Tr	igger s	tatus (1	l bit p	er trigge	er)					1			I	
0x514: Delay HS 1 stimulation data	n							Sic	deband	data (1	1 bit p	oer sideb	and men	nory chann	el)							
0x520: Delay HS 2 trigger								Tr	igger s	tatus (1	l bit p	er trigge	er)									
0x524: Delay HS 2 stimulation data	n							Sic	deband	l data (1	1 bit p	oer sideb	and men	nory chann	el)							
0x540: Digital mux source target config	source Co	ode*		S	source	bit se	elect*		ta	nrget Co	ode**	ķ			target bi	t select**						
0x544: Digital mux source read prepare (WO)	don't care	2							ta	arget**	:				target bi	t select**						

*Source Code and bits:

source Code	Source Nur	mber of bits	source bit select
IFB			
0x00	Digital In	32	0 - 31
0x01	Digital Single Pulse	Reg 32	0 - 31
0x02	Feedback	32	0 - 31
0x03	Aux Data In	2	0 - 1
	Fix 0	1	2

	Fix 1	1	3	
	DACQ is running	4	4 - 7	
	Digital Peri. Pulse Gen.	8	8 - 15	
	Digital Out Stimul.	16	16 - 31	
0x04	Digital Data Reg.	32	0 - 31	
HS 1/2 (HS 1	: $0x40-0x7F$, HS 2: $0x80-0$	xBF)		
0x40/0x80	Trigger Status 0 - 15	32	0 - 31	
0x41/0x81	Trigger Status 16 - 17	4	0 - 3	
0x42/0x82	Sideband data 0	16	0 - 15	
0x43/0x83	Sideband data 1	16	0 - 15	
0x44/0x84	Sideband data 2	16	0 - 15	
0x45/0x85	Sideband data 3	16	0 - 15	
0x46/0x86	Sideband data 4	16	0 - 15	
0x47/0x87	Sideband data 5	16	0 - 15	
0x48/0x88	Sideband data 6	16	0 - 15	
0x49/0x89	Sideband data 7	16	0 - 15	
0x4A/0x8A	Sideband data 8	16	0 - 15	
0x4B/0x8B	Sideband data 9	16	0 - 15	
0x4C/0x8C	Sideband data 10	16	0 - 15	
0x4D/0x8D	Sideband data 11	16	0 - 15	
0x4E/0x8E	Sideband data 12	16	0 - 15	
0x4F/0x8F	Sideband data 13	16	0 - 15	
0x50/0x90	Sideband data 14	16	0 - 15	
0x51/0x91	Sideband data 15	16	0 - 15	
0x52/0x92	Sideband data 16	16	0 - 15	
0x53/0x93	Sideband data 17	16	0 - 15	
0x54-0x7F	Reserved			
0x94-0xFF	Reserved			

**Target Code and bits:

target Code	Target Nu	umber of b	oits target bit se	elect
0x0	Trigger for STGs on HS	5 1 32	0 - 31	
0x1	Trigger for STGs on HS	5 2 32	0 - 31	
0x2	Dig Out	32	0 - 31	
0x3	Digital MUX Stream S0	32	0 - 31	
0x4	Digital MUX Stream S1	32	0 - 31	
0x5	Trigger for DACQ Start	32	0 - 31	
0x6	Digital Out Stimulator	32	0 - 31	
0x7-0xFF	Reserved			

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x600:								-											digital	DSP	DAC	Analog	ADC								HS2	HS1
Data																															link	link
stream																															up	up
enable																																
0x604:																								l								
FIFO																																
control																																
0 ->																																
DACQ																																
path																																
reset																																

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
0x700: Right audio channel			•											rce (D		₹,									Ch	anr	iel	•	•		
0x704: Left audio channel														rce (D		₹,									Ch	anr	iel				
0x710: Right attenuation																											Atı	teni	atic	n	
0x714: Right attenuation																											Atı	tenı	atic	on	

*Source: Source decoding:

0: No source

1: HS0

2: HS1

3: IF

4: DSP(bits 23 - 0)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	5	4	3	2	1	0
0x800: Downsampling device 0						ı					<u> </u>	1						ı						1	P	erce	ntage	e of f	ull	dat	a rate		
0x802: Downsampling device 2																									P	erce	ntage	e of f	ull	dat	a rate		
0x804: Start devices																															Device 2		Device 0
0x808: Stop devices																															Device 2		Device 0
0x80c: Reset device 0																															<u>'</u>		Reset
0x80e: Reset device 2																																	Reset

001	Determine desire*	(Cal. Carray)(Carray to all at within data day
0x81c: Channel select	Data source device*	(Sub-Group)/Segment select within data device
device 0		
0x81e:	Data source device*	(Sub-Group)/Segment select within data device
Channel select		
device 2		
0x820:	Channel 0 to 31 for selected source and group	
Channel		
Select device		
0		
0x822:	Channel 0 to 31 for selected source and group	
Channel		
Select device		
2		
0x824:	Channel 32 to 63 for selected source and group	
Channel	8	
Select device		
0		
0x826:	Channel 32 to 63 for selected source and group	
Channel	Chainer 52 to 65 for selected source and group	
Select device		
2		
0x828:	Channel 64 to 95 for selected source and group	
Channel	Channel 64 to 93 for selected source and group	
Select device		
0		
0x82a: Channel	Channel 64 to 95 for selected source and group	
Select device		
2		
0x82c:	Channel 96 to 127 for selected source and group	
Channel		
Select device		
0x82e:	Channel 96 to 127 for selected source and group	
Channel		
Select device		
2		
0x830:	Channel 128 to 159 for selected source and group	
Channel		
Select device		
0		
0x832:	Channel 128 to 159 for selected source and group	
Channel		
Select device		
2		
0x834:	Channel 160 to 191 for selected source and group	
Channel		
Select device		
0		

0x836:	Channel 160 to 191 for selected source and group					
Channel	Chainer 100 to 191 for selected source and group					
Select device						
2						
0x838:	Channel 192 to 223 for selected source and group					
Channel						
Select device						
0						
0x83a:	Channel 192 to 223 for selected source and group					
Channel	g ·· I					
Select device						
2						
0x83c:	Channel 224 to 255 for selected source and group					
Channel						
Select device						
0						
0x83e:	Channel 224 to 255 for selected source and group					
Channel						
Select device						
2						
0x870: Data			Volta	ge range i	n Data mode	2***
format device				t mode**		
0						
0x872: Data			X7. 1.		D . 1	ate ate ate
				ge range i t mode**	n Data mode	3***
format device			10 01	подетт		
2						
0x880: Filter		send		send		send
Data Select		IFB		HS2		HS1
Register		Filtered		Filtered		Filtered
		data		data		data

*Data source:

Source:	Code:	Segment from/to:	bits:
Headstage 1	0x1	0	0 to 255 -> 256 channels per Headstage
Headstage 2	0x5	0	0 to 255 -> 256 channels per Headstage
IF	0x9	0	0 to 7 -> 8 ADC channels
Reserved for analog	0xA	0 to 1(0: HS1, 1: HS2)	0 to 11 -> 0 to 31
STG DAC Data	0xB	0 to 1(0: HS1, 1: HS2)	0 to 11 -> DAC 0 to 11
DSP	0xC	0 to 7	0 to 255 -> 256 32 bit Channels
Digital Data	0xD	0 to 4(1/2: HS1, 3/4: HS2)	0 to 11/63 -> 14 32bit Vector***
Reserved	0xE	0	

**Voltage Range:

	bit	07	06	05	04	De	sci	ription:	:			
16 bit mod	9	0	0	0	0	Bits	31	(sign)	&	14	downto	0
16 bit mode	=	0	0	0	1	Bits	31	(sign)	&	15	downto	1
16 bit mode	€	0	0	1	0	Bits	31	(sign)	&	16	downto	2
16 bit mode	€	0	0	1	1	Bits	31	(sign)	&	17	downto	3
16 bit mode	€	0	1	0	0	Bits	31	(sign)	&	18	downto	4
16 bit mode	€	0	1	0	1	Bits	31	(sign)	&	19	downto	5

```
16 bit mode
                 0
                        1
                             0
                               Bits 31 (sign) & 20 downto 6
                    1
16 bit mode
                                Bits 31 (sign) & 21 downto 7
                 0
                     1
                         1
                             1
16 bit mode
                 1
                     0
                         0
                             0
                                  Bits 31 (sign) & 22 downto 8
```

***Data mode:

*****Digital Data 32bit vector:

```
Segment 0: (IFB Dig Data)
Bits: Data Source:
0, 1
      Digital MUX Stream SO (to be used on USB Port A)
      Digital MUX Stream S1 (to be used on USB Port B)
      Digital In
4, 5
6, 7
      Digital Out
8, 9
       Feedback Register
10, 11 Digital Register
12
       Aux Input and Dig Periodig Pulse
13
       Digital Generator/Stimulator
Segment 1: (Headstage 1 Sideband Data)
Bits: Data Source:
0, 1 Sideband Vector 0
      Sideband Vector 1
4, 5
      Sideband Vector 2
6, 7
      Sideband Vector 3
8, 9
       Sideband Vector 4
10, 11 Sideband Vector 5
12, 13 Sideband Vector 6
14, 15 Sideband Vector 7
16, 17 Sideband Vector 8
18, 19 Sideband Vector 9
20, 21
       Sideband Vector 10
22, 23 Sideband Vector 11
24, 25 Sideband Vector 12
26, 27
       Sideband Vector 13
28, 29 Sideband Vector 14
30, 31 Sideband Vector 15
32, 33 Sideband Vector 16
```

```
34, 35 Sideband Vector 17
Segment 2: (Headstage 1 Trigger Status)
Bits: Data Source:
 0 Trigger 0 status
 2 Trigger 1 status
 4 Trigger 2 status
 6 Trigger 3 status
 8 Trigger 4 status
10 Trigger 5 status
12 Trigger 6 status
14 Trigger 7 status
16 Trigger 8 status
18 Trigger 9 status
20 Trigger 10 status
22 Trigger 11 status
24 Trigger 12 status
26 Trigger 13 status
28 Trigger 14 status
30 Trigger 15 status
32 Trigger 16 status
34 Trigger 17 status
Segment 3: (Headstage 2 Sideband Data)
Bits: Data Source:
 0, 1 Sideband Vector 0
 2, 3 Sideband Vector 1
 4, 5 Sideband Vector 2
 6, 7
      Sideband Vector 3
8, 9
       Sideband Vector 4
10, 11 Sideband Vector 5
12, 13 Sideband Vector 6
14, 15 Sideband Vector 7
16, 17 Sideband Vector 8
18, 19 Sideband Vector 9
20, 21 Sideband Vector 10
22, 23 Sideband Vector 11
24, 25 Sideband Vector 12
26, 27 Sideband Vector 13
28, 29 Sideband Vector 14
30, 31 Sideband Vector 15
32, 33 Sideband Vector 16
34, 35 Sideband Vector 17
Segment 4: (Headstage 2 Trigger Status)
```

Bits	: Data	So	urce:
0	Trigger	0	status
	Trigger		
4	Trigger	2	status
6	Trigger	3	status
8	Trigger	4	status
10	Trigger	5	status
12	Trigger	6	status
14	Trigger	7	status
16	Trigger	8	status
18	Trigger	9	status
20	Trigger	10	status
22	Trigger	11	status
24	Trigger	12	status
26	Trigger	13	status
28	Trigger	14	status
30	Trigger	15	status
32	Trigger	16	status
34	Trigger	17	status

Register	31 30 29 28 27 26	25 24 23 22 21	20 19 18	17	16	15 14	13 12 1	1 10	9	8	7	6	5	4	3	2	1	0
0xb00:				,				,	I	nt					•	•	Clear Fifo	Reset
DSP									I	ln							Flags(WO)	Fifo(WO)
Indata																		
CTRL																		
Register																		
0xb04:									I	nt							Clear Fifo	Reset
DSP									I	ln							Flags(WO)	Fifo(WO)
Outdata																		
CTRL																		
Register																		
0xb08:											overflow	overflow	full	progr.	progr.	empty	underflow	underflow
DSP In											occured			full	empty			occured
Fifo Status																		
Flags(RO)																		
0xb0c:											overflow	overflow	full	progr.	progr.	empty	underflow	underflow
DSP Out											occured			full	empty			occured
Fifo Status																		
Flags(RO)																		
0xb10:		Fifo full TH						F	ifo empt	/ TH								
DSP																		
Indata																		
Threshold																		
Register																		

0xb14:		Fifo full TH						Fifo emp	ty TH	(insert an	ount of tra	nsmit dat	a here)				
DSP																	
Outdata																	
Threshold																	
Register																	
Register																	
0xb18:	Configured channels, de	etected after a full sweep,	, reread i	f 0												-	
DSP		•															
Indata																	
Channel																	
Info(RO)																	
0xb20:			Bootme	ode				Reset	POR								
			Dootiii	ouc				Reset	IOK								
DSP Boot																	
conf.																	
Register																	
0xb24:									Int								
DSP									En								
Mailbox																	
CTRL																	
Register																	
0.100							T	1 4 5 5			,, ,-						
0xb28:							Last use	a Addres	ss at w	rite to Mai	ibox Mem	ory					
DSP																	
Mailbox																	
Info																	
Register																	
						T				1							1
0xb30:				Keep last	Enable				Int							Clear Fifo	Reset
DSP				Streamdata	Streaming				En							Flags(WO)	Fifo(WO)
Streamdata																	
CTRL																	
Register																	
0xb34:										overflow	overflow	full	progr.	progr.	empty	underflow	underflow
DSP										occured			full	empty			occured
Stream																	
Fifo Status																	
Flags(RO)																	
rags(RO)																	
0xb38:														•		Connect	Connect
I2C Bus																DSP I2C	DSP I2C
CTRL																Bus with	Bus with
																USB B	USB A
Register																	
																I2C BUS	I2C BUS
0xb40:								send				send				send HS1	
Filter Data								IFB				HS2				Filtered	
Select								Filtered				Filtered				data	
Register								data				data					
0xb81:																	256
Indata																	channels
																	Chaineis
Enable:																	
Headstage																	
1																	
Owker																	250
0xb85:																	256
Indata																	channels
Enable:																	
Headstage																	
2																	

0.100					
0xb89:					8
Indata					channels
Enable:					
IFB					
Analog					
0xb8b:				12 HS 2	12 HS 1
Indata				channels*	channels*
Enable:					
STG DAC					
Data					
0xb8d:	18 HS 2	18 HS 2	18 HS 1	18 HS 1	8 IFB
Indata	Trig.	SBS	Trig.	SBS	channels*
Enable:	Stat.	channels*	Stat.	channels*	
Digital	channels*		channels*		
Data					
0xb8f:					6
Indata					channels*
Enable:					
Tail Data					

*Data source details:

for more details see Data Stream Select Register Description food notes at address 0x800

Register	31	30	29	2	8 27	26	2	5 24	23	22	21	20	19	18	17	16	15	14	1	3 12	11	1	0	9	8	7	6	5	4	3	2	1	0
0xc00: HS1 Data Filter 1 coefficent b[0]	Filte	r co	peffi	ce	ent b[()] as (Q1	.16 va	lue										0	to ext	end	cc	eff	ici	ent	to	Q1	.30	ı	I			
0xc02: HS1 Data Filter 1 coefficent b[1]	Filte	r co	peffi	ce	nt b[1] as (Q1	.16 va	lue										0	to ext	end	cc	eff	ici	ent	to	Q1	.30					
0xc03: HS1 Data Filter 1 coefficent a[1]	Filte	r co	oeffi	ce	nt a[1] as (Q1	.30 va	lue (Q1.3	3 tog	gethe	er w	ith lo	wer	bits	regi	ster))														
0xc04: HS1 Data Filter 1 coefficent b[2]	Filte	r co	oeffi	ce	ent b[2	2] as (Q1	.16 va	lue										0	to ext	end	cc	eff	icie	ent	to	Q1	.30					
0xc05: HS1 Data Filter 1 coefficent a[2]	Filte	r co	oeffi	ce	ent a[2	?] as (Q1	.30 va	lue (Q1.3	3 tog	gethe	er w	ith lo	wer	bits	regi	ster)	,														

0xc06: HS1 Data Filter 1 coefficent lower bits 0xc07: HS1 Data Filter 1 control	lower bits of a[2]		lower b of a[1]	its	Enable Filter
0xc08: HS1 Data Filter 2 coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc0a: HS1 Data Filter 2 coefficent b[1]		cent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
Oxc0b: HS1 Data Filter 2 coefficent a[1]		cent a[1] as Q1.30 value (Q1.33 together with lower b	its register)		
0xc0c: HS1 Data Filter 2 coefficent b[2]		cent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
Oxc0d: HS1 Data Filter 2 coefficent a[2]	Filter coeffi	cent a[2] as Q1.30 value (Q1.33 together with lower b	its register)		
0xc0e: HS1 Data Filter 2 coefficent lower bits	lower bits of a[2]		lower b	its	
0xc0f: HS1 Data Filter 2 control					Enable Filter
0xc10: HS1 Data Filter 3 coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc12: HS1 Data Filter 3 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	

0xc13: HS1 Data Filter 3 coefficent a[1]	Filter coeffi	icent a[1] as Q1.30 value (Q1.33 toget	ther with lower bits register)		
0xc14: HS1 Data Filter 3 coefficent b[2]	Filter coeffi	icent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc15: HS1 Data Filter 3 coefficent a[2]		icent a[2] as Q1.30 value (Q1.33 toget			
0xc16: HS1 Data Filter 3 coefficent lower bits	lower bits of a[2]		lower b	its	
0xc17: HS1 Data Filter 3 control					Enable Filter
0xc18: HS1 Data Filter 4 coefficent b[0]	Filter coeffi	icent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc1a: HS1 Data Filter 4 coefficent b[1]	Filter coeffi	icent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc1b: HS1 Data Filter 4 coefficent a[1]	Filter coeffi	icent a[1] as Q1.30 value (Q1.33 toget	ther with lower bits register)		
0xc1c: HS1 Data Filter 4 coefficent b[2]	Filter coeffi	icent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc1d: HS1 Data Filter 4 coefficent a[2]	Filter coeffi	icent a[2] as Q1.30 value (Q1.33 toget	ther with lower bits register)		
0xc1e: HS1 Data Filter 4 coefficent lower bits	lower bits of a[2]		lower b of a[1]	its	

0xc1f: HS1 Data Filter 4 control								Enable Filter
0xc34: HS1 highpass filter frequency	Corner freq	uency of highpass filte	er in mHz					
0xc35: HS1 highpass filter information	filter order		band: highpass	family			1: software filter	enabled
0xc38: HS1 lowpass filter frequency	Corner freq	uency of lowpass filte	r in mHz	·				
0xc39: HS1 lowpass filter information	filter order		band: lowpass	family			1: software filter	enabled
0xc40: HS2 Data Filter 1 coefficent b[0]	Filter coeffi	icent b[0] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0xc42: HS2 Data Filter 1 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0xc43: HS2 Data Filter 1 coefficent a[1]	Filter coeffi	icent a[1] as Q1.30 val	lue (Q1.33 together with	lower bits register)			
0xc44: HS2 Data Filter 1 coefficent b[2]	Filter coeffi	icent b[2] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0xc45: HS2 Data Filter 1 coefficent a[2]	Filter coeffi	icent a[2] as Q1.30 val	lue (Q1.33 together with	lower bits register				
0xc46: HS2 Data Filter 1 coefficent lower bits	lower bits of a[2]			lower of a[1]				

0xc47: HS2 Data Filter 1 control				Enable Filter
0xc48: HS2 Data Filter 2 coefficent b[0]	Filter coefficent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	1
0xc4a: HS2 Data Filter 2 coefficent b[1]	Filter coefficent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc4b: HS2 Data Filter 2 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together	with lower bits register)		
0xc4c: HS2 Data Filter 2 coefficent b[2]	Filter coefficent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc4d: HS2 Data Filter 2 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together	with lower bits register)		
0xc4e: HS2 Data Filter 2 coefficent lower bits	lower bits of a[2]	lower b	its	
0xc4f: HS2 Data Filter 2 control				Enable Filter
0xc50: HS2 Data Filter 3 coefficent b[0]	Filter coefficent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc52: HS2 Data Filter 3 coefficent b[1]	Filter coefficent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc53: HS2 Data Filter 3 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together	with lower bits register)		

Oxc54: HS2 Data Filter 3 coefficent b[2] Oxc55: HS2 Data Filter 3 coefficent a[2] Oxc56:		cent b[2] as Q1.16 value cent a[2] as Q1.30 value (Q1.33 together with lower bits	register)		
HS2 Data Filter 3 coefficent lower bits	of a[2]		of a[1]		
0xc57: HS2 Data Filter 3 control					Enable Filter
0xc58: HS2 Data Filter 4 coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc5a: HS2 Data Filter 4 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc5b: HS2 Data Filter 4 coefficent a[1]	Filter coeffi	cent a[1] as Q1.30 value (Q1.33 together with lower bits	register)		
0xc5c: HS2 Data Filter 4 coefficent b[2]	Filter coeffi	cent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc5d: HS2 Data Filter 4 coefficent a[2]	Filter coeffi	cent a[2] as Q1.30 value (Q1.33 together with lower bits	register)		
0xc5e: HS2 Data Filter 4 coefficent lower bits	lower bits of a[2]		lower b of a[1]	its	
0xc5f: HS2 Data Filter 4 control					Enable Filter

0xc74: HS2 highpass filter frequency	Corner frequency of highpass filt	er in mHz							
0xc75: HS2 highpass filter information	filter order	band: highpass	family			1: software filter	enabled		
0xc78: HS2 lowpass filter frequency	Corner frequency of lowpass filter								
0xc79: HS2 lowpass filter information	filter order	band: lowpass	family			1: software filter	enabled		
0xc80: IFB Data Filter 1 coefficent b[0]	Filter coefficent b[0] as Q1.16 value 0 to extend coefficient to Q1.30								
0xc82: IFB Data Filter 1 coefficent b[1]	Filter coefficent b[1] as Q1.16 va	lue		0 to extend coefficient	to Q1.30				
0xc83: IFB Data Filter 1 coefficent a[1]	Filter coefficent a[1] as Q1.30 va	lue (Q1.33 together with lower bits	register)						
0xc84: IFB Data Filter 1 coefficent b[2]	Filter coefficent b[2] as Q1.16 va	lue		0 to extend coefficient	to Q1.30				
0xc85: IFB Data Filter 1 coefficent a[2]	t								
0xc86: IFB Data Filter 1 coefficent lower bits	lower bits of a[2]		lower b of a[1]	its					
0xc87: IFB Data Filter 1 control	•						Enable Filter		

	1				
0xc88: IFB Data Filter 2 coefficent b[0]	Filter coeffi	icent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc8a: IFB Data Filter 2 coefficent b[1]	Filter coeffi	icent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc8b: IFB Data Filter 2 coefficent a[1]	Filter coeffi	icent a[1] as Q1.30 value (Q1.33 together	with lower bits register		
Oxc8c: IFB Data Filter 2 coefficent b[2]	Filter coeffi	icent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc8d: IFB Data Filter 2 coefficent a[2]		icent a[2] as Q1.30 value (Q1.33 together	with lower bits register		
Oxc8e: IFB Data Filter 2 coefficent lower bits	lower bits of a[2]		lower to of a[1]	pits	
0xc8f: IFB Data Filter 2 control			·		Enable Filter
0xc90: IFB Data Filter 3 coefficent b[0]	Filter coeffi	icent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc92: IFB Data Filter 3 coefficent b[1]	Filter coeffi	icent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc93: IFB Data Filter 3 coefficent a[1]	Filter coeffi	icent a[1] as Q1.30 value (Q1.33 together	with lower bits register)	
0xc94: IFB Data Filter 3 coefficent b[2]	Filter coeffi	icent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	

0xc95: IFB Data Filter 3 coefficent a[2]		cent a[2] as Q1.30 value (Q1.33 together with lower bits			
0xc96: IFB Data Filter 3 coefficent lower bits	lower bits of a[2]		lower bi of a[1]	ts	
0xc97: IFB Data Filter 3 control					Enable Filter
0xc98: IFB Data Filter 4 coefficent b[0]	Filter coeffic	cent b[0] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc9a: IFB Data Filter 4 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc9b: IFB Data Filter 4 coefficent a[1]	Filter coeffi	cent a[1] as Q1.30 value (Q1.33 together with lower bits	s register)		
0xc9c: IFB Data Filter 4 coefficent b[2]		cent b[2] as Q1.16 value		0 to extend coefficient to Q1.30	
0xc9d: IFB Data Filter 4 coefficent a[2]	Filter coeffi	cent a[2] as Q1.30 value (Q1.33 together with lower bits	s register)		
0xc9e: IFB Data Filter 4 coefficent lower bits	lower bits of a[2]		lower bi of a[1]	its	
0xc9f: IFB Data Filter 4 control					Enable Filter
0xcb4: IFB highpass filter frequency	Corner frequ	uency of highpass filter in mHz			

0xcb5: IFB highpass filter information	filter order	band: highpass	family	1: software filter	enabled
0xcb8: IFB lowpass filter frequency	Corner frequency of lowpass filter	r in mHz			
0xcb9: IFB lowpass filter information	filter order	band: lowpass	family	1: software filter	enabled

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xe00:			•			•																									DMA	DMA
DMA																															active	start
control																																
0xe04:																	Star	t ad	dres	s												
DMA																																
start																																
address																																
0xe08:																						Co	unte	er								
DMA																																
counter																																

Mini DMA command overview:

Command	Bit 31 to 24	Bit 23 to 0	Description
SDTA	0x01	register address	Store next data to register address
DATA	Data	Data	Data expected after SDTA command
STP	0xFF	(anything)	Stop DMA

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 6 5 4 3 2 1 0
0xf00:																								Fifo Reset	Instruction Code
(WO)EEPROM																									
Instruction																									
Code Register																									
0xf00:																						FIFO_empty	FIFO_full	Statemachine	Flash Status Register
(RO)EEPROM																								busy	
Status																									
Register																									
0xf04:									Flas	sh A	ddre	ss													L
EEPROM																									
Memory																									
Address																									
Register																									

0xf08:	256 Data Bytes in 64 DWords to/from Flash
EEPROM	
Data FIFO	
Register	
0xf0c:	Address length Clock Divider Register (Multiples of 2 divide 38.4 MHz)
EEPROM HW	(1, 2 or 3
configuration	Bytes)
Register	
0xf10:	Offset for reads and writes to the EEprom
EEPROM	
Offset	
Register	
0xf14:	Size of the EEprom Block available for this Image
EEPROM	
Size Register	

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	1	13 1	2 11	1	10	9	8	3 7	7	6 5	; [4 3	3	2 1		0
0xf80: FPGA																	GE	NEF	R.A	AL 2 (lata													
GENERAL 2																																		
0xf84: FPGA																	GE	NEF	R.A	AL 5	lata													
GENERAL 5																																		
0xf90: direct																																1 1	pre	
connection to																																	mb	er
FPGA SPI																																(0		
Flash																																no	ne)	
0xf94: Config																	bas	e ad	ldı	ess o	con	ıfiş	g ee	pro	om	ı								
EEprom Base																																		
0xf98:																	Fir	nwa	are	Vers	ion (of	FX	3 E	300	otst	rap	со	de	this	s U	SB P	ort	
FX3-USB																																		
Bootstrap																																		
Firmware																																		
0xf9c:																	Fir	nwa	are	Vers	ion (of	FΧ	3 E	300	otst	rap	со	de	on	oth	er US	SB I	Port
FX3-USB																																		
Bootstrap																																		
Firmware other																																		
port																																		
0xfb0:	Av	vrite	wil	l cau	ise a	n int	errup	ot on	the o	other	Cyl	oress	, wit	har	ead	you	can	chec	ck	is it i	s rea	d a	alre	ady	y									
Message to																																		
other Cypress																																		
0xfb4: Read	Eac	ch bi	t wh	nich i	is se	t wil	l be 1	eset	on re	ead																								
Only: Message																																		
from other																																		
Cypress																																		

Mailbox Register Address Map (Address bits 11-0) Base Address: 0x1000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000 - 0xFFC: Mailbox Registers	wri	te w	ill ge	enera	ate a	n Int	erruj	pt on	GP	6 Li	ne																					

Headstage Address Map (Address bits 11-0), Base Address HS1: 0x8000, HS2: 0xC000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
0x000: Device ID																									0x	0f =	MI	EA21	00-	256	5
																									H	3					
0x001: Serial	lowe	er 3	2 bit	t of h	eads	stage	seri	al nı	ımbe	r, rea	ıd as	4 A	SCII	byte	s																
number low																															
0x002: Serial	high	er 3	32 bi	it of	head	stag	e ser	ial n	umb	er, re	ad as	s 4 A	SCI	I byt	es																
number high																															
0x004: Version									Ass	embl	ly		PC:	B Re	visi	on	FP	GA	Vers	ion											
									Ver	sion																					
0x008:																									A	lapte	er T	ype			
Configuration																															
0x00c: Limits	Lim	its																													

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x010: Port																			•			•								•		Link
Status																																Up
0x014: Error Count																	CR	C Eı	rror (Cour	nt, re	set o	n v	vrite	e							

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x020: Reset																																Reset

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 6 5 4 3 2 1 0
0x030:				•		•			•	•											•			Fifo Reset	Instruction Code
(WO)Flash																									
Instruction																									
Code																									
Register																									
0x030:																						FIFO_empty	FIFO_full	Statemachine	Flash Status Register
(RO)Flash																								busy	
Status																									
Register																									

0x034:			Flash Address
Flash			
Memory			
Address			
Register			
0x038:	256 Data Bytes	in 64 DWords to/	from Flash
Flash Data			
FIFO			
Register			
0x03c:	Address length	Clock Divider R	egister (Multiples of 2 divide 38.4 MHz)
Flash HW	(1, 2 or 3		
configuration	Bytes)		
Register			

Register	31	1 30) 2	29	28	27	26	5 2	5 2	4	23	22	21	20	19	1	8	17	16	15	14	13	1	2 1	11	10	9	8	7	' 6	5 5	5 4	1 3	2	1	0
0x040:							1							I							1						<u> </u>	Fifo Reset	I	nst	ruc	tio	ı Co	ode		_
(WO)EEPROM																																				
Instruction																																				
Code Register																																				
0x040:																										FIFO_empty	FIFO_full	Statemachine	F	las	h S	Stat	us I	Reg	istei	
(RO)EEPROM																												busy								
Status																																				
Register																																				
0x044:											Flas	h A	ddre	ss														•								
EEPROM																																				
Memory																																				
Address																																				
Register																																				
0x048:	25	56 D	ata	Ву	tes	in 6	64 D	Wo	rds t	io/fi	rom	Fla	sh																							
EEPROM																																				
Data FIFO																																				
Register																																				
0x04c:	A	ddre	ss	leng	gth	Cl	ock	Div	ider	Re	gist	er (l	Mult	iple	s of	2 d	ivic	le 3	8.4	МН	z)															_
EEPROM HW	(1	, 2 o	r 3	,																																
configuration	В	ytes))																																	
Register																																				

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x050:																					•										DMA	DMA
DMA																															active	start
control																																
0x054:																	Sta	rt ad	dres	s												•
DMA																																
start																																
address																																
0x058:																						Co	unt	er								
DMA																																
counter																																

Mini DMA command overview:

Command	Bit 31 to 24	Bit 23 to 0	Description
SDTA	0x01	register address	Store next data to register address
DATA	Data	Data	Data expected after SDTA command
STP	0xFF	(anything)	Stop DMA

Register	31	30	29	9 28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 6	5	4	3 2	1	0
0x100: Number of detection electrodes	256	Ele	ectr	odes			·	'													•			•	•					
0x110: ADC Range	AD	C ra	ınge	ge (0x0	023	1860 =	: 23	00 r	nV)																					
0x114: ADC Resolution	AD	C R	eso	olution	(0x	80000	112	2 = 2	274 n	V/b	it)																			
0x118: DAC Resolution	AD	C R	eso	olution	in b	oits (0	:00	0000)18 =	24	bit)																			
0x11c: Gain	Gai	n of	the	e DAC	Q S	ystem	(0)	800	00271	0 =	gaiı	n 10	.0)																	
0x120: Limitations	Lin	nitai	ons	s of thi	s Sy	stem	an	be v	vritte	n he	ere																			
0x130: Max Sampling Frequency	Ma	ximı	um	Frequ	enzy	y that	s al	llow	ed to	be	set a	at co	nfigu	ıratio	on fo	or the	e use	er (0:	x000	0C3	50 =	501	кНz)						

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 6	5	4	3	2	2	-	1	0	
0x400: Enable blanking	Electi	rode	32	to 1				'			'								•			•						'						
0x401: Enable blanking	Electi	rode	e 64	to 3	3																													
0x402: Enable blanking	Electr	rode	96	to 6	55																													
0x403: Enable blanking	Electi	rode	128	3 to	97																													
0x404: Enable blanking	Electi	rode	e 160) to	129																													
0x405: Enable blanking	Electi	rode	192	2 to	161																													
0x406: Enable blanking	Electr	rode	224	l to	193																													
0x407: Enable blanking	Electi	rode	256	ó to	225																													

0x480: Blanking control for stimulus channels	Force data keep			Enable data keep on stimulation channels, post filter	Enable data keep on stimulation channels, mid filter	Enable data keep on stimulation channels, pre filter
0x484: Stimulus data keep pre filter		onset delay	offset delay	,		
0x488: Stimulus data keep mid filter		onset delay	offset delay	,		
0x48c: Stimulus data keep post filter		onset delay	offset delay	,		
0x4a0: Blanking control for non-stimulus channels	Force data keep			Enable data keep on measurement channels, post filter	Enable data keep on measurement channels, mid filter	Enable data keep on measurement channels, pre filter
0x4a4: Non-stimulus data keep pre filter		onset delay	offset delay	,		
0x4a8: Non-stimulus data keep mid filter		onset delay	offset delay	,		
0x4ac: Non-stimulus data keep post filter		onset delay	offset delay	,		
0x4c0: Highpass Filterreset						Reset filter
0x4c4: Highpass reset duration			D	Duration in 20u	s units	

Register	31 30	29	28	27	26	25	5 24	1 2.	3	22	21	20	19	9 1	8	17	16	15	1	4	13	12	2 1	1	10	9	8	7	6	5 4	1 3	3 2		1	0	
0x600: Filter 1 coefficent b[0]	Filter co	oeffi	cent b	p[0]	as (Q1.	16 va	alue	;												0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0						
0x602: Filter 1 coefficent b[1]	Filter co	oeffi	cent b	[1]	as Ç	Q1.	16 va	alue													0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0						
0x603: Filter 1 coefficent a[1]	Filter co	oeffi	cent a	[1]	as Ç	Q1	30 va	alue	(Q	1.33	tog	gethe	er v	with	lo	wer	bit	s reg	iste	er)																
0x604: Filter 1 coefficent b[2]	Filter co	oeffi	cent b	[2]	as (Q1.	16 va	alue	;												0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0						
0x605: Filter 1 coefficent a[2]	Filter co	oeffi	cent a	[2]	as Ç	Q1	30 va	alue	(Q	1.33	tog	gethe	er v	with	lo	wer	· bit	s reg	iste	er)																
0x606: Filter 1 coefficent lower bits	lower b of a[2]	its																	wer a[1	bit	ts															
0x607: Filter 1 control																																		nabl lank	Enal Filte	
0x608: Filter 2 coefficent b[0]	Filter co	oeffi	cent b	[0]	as (Q1.	16 va	alue	;												0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0			•			
0x60a: Filter 2 coefficent b[1]	Filter co	oeffi	cent b	[1]	as (Q1.	16 va	alue	;												0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0						
0x60b: Filter 2 coefficent a[1]	Filter co	oeffi	cent a	[1]	as Ç	Q1	30 va	alue	(Q	1.33	tog	gethe	er v	with	lo	wer	bits	s reg	iste	er)																
0x60c: Filter 2 coefficent b[2]	Filter co	oeffi	cent b	p[2]	as (Q1.	16 va	alue	;												0 t	o e	xten	nd c	oef	fici	ent	to (Q1.3	0						
0x60d: Filter 2 coefficent a[2]	Filter co	oeffi	cent a	[2]	as Ç	Q1	30 va	alue	(Q	1.33	tog	gethe	er v	with	lo	wer	bit	s reg	iste	er)																
0x60e: Filter 2 coefficent lower bits	lower b of a[2]	its																- 1	wer a[1	bit	ts															

0x60f: Filter 2 control						Enable Blanking	Enable Filter
0x610: Filter 3 coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 value		0	to extend coefficient to Q1.30	·	
0x612: Filter 3 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 value		0	to extend coefficient to Q1.30		
0x613: Filter 3 coefficent a[1]	Filter coeffi	cent a[1] as Q1.30 value (Q1.33 together	with lower bits reg	ister)			
0x614: Filter 3 coefficent b[2]	Filter coeffi	cent b[2] as Q1.16 value		0	to extend coefficient to Q1.30		
0x615: Filter 3 coefficent a[2]	Filter coeffi	cent a[2] as Q1.30 value (Q1.33 together	with lower bits reg	ister)			
0x616: Filter 3 coefficent lower bits	lower bits of a[2]			wer bits			
0x617: Filter 3 control			1			Enable Blanking	Enable Filter
0x618: Filter 4 coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 value		0	to extend coefficient to Q1.30		
0x61a: Filter 4 coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 value		0	to extend coefficient to Q1.30		
0x61b: Filter 4 coefficent a[1]	Filter coeffi	cent a[1] as Q1.30 value (Q1.33 together	with lower bits reg	rister)			
0x61c: Filter 4 coefficent b[2]	Filter coeffi	cent b[2] as Q1.16 value		0	to extend coefficient to Q1.30		
0x61d: Filter 4 coefficent a[2]	Filter coeffic	cent a[2] as Q1.30 value (Q1.33 together	with lower bits reg	rister)			

0x61e: Filter 4 coefficent lower bits 0x61f: Filter 4 control	lower bits of a[2]			lower b	pits		Enable Blanking	Enable Filter
0x620: Filter 2b coefficent b[0]	Filter coeffi	cent b[0] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0x622: Filter 2b coefficent b[1]	Filter coeffi	cent b[1] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0x623: Filter 2b coefficent a[1]	Filter coeffi	cent a[1] as Q1.30 val	ue for one clock after blank (Q1.3	3 togethe	r with lower bits registe	r)		
0x624: Filter 2b coefficent b[2]	Filter coeffi	cent b[2] as Q1.16 va	lue		0 to extend coefficient	to Q1.30		
0x625: Filter 2b coefficent a[2]	Filter coeffi	cent a[2] as Q1.30 val	ue for one clock after blank (Q1.3	3 togethe	r with lower bits registe	r)		
0x626: Filter 2b coefficent lower bits	lower bits of a[2]			lower b of a[1]	oits			
0x630: hardware filter frequency	Corner frequ	uency of hardware filt	er in mHz					
0x631: hardware filter information	filter order		band: lowpass	family			0: hardware filter	enabled
0x634: highpass filter frequency	Corner frequency	uency of highpass filte	er in mHz					
0x635: highpass filter information	filter order		band: highpass	family			1: software filter	enabled
0x638: lowpass filter frequency	Corner frequency	uency of lowpass filte	r in mHz					

0x639:	filter order	band: lowpass	family	1:	enabled
lowpass				software	
filter				filter	
information					

Headstage Stimulation Address Map (Address bits 11-0), Base Address HS1: 0x9000, HS2: 0xD000

Register	31	30	29	28	27	26	25	24	2	23 22	21	2	20 19	18	17	16	15	14	1	13	12	11	10	9)	8	7	6	5	4	3	2	1 (0
0x100: Voltage Range	Vo	ltag	e ran	ge ((0x00	00 2	710 :	= 100	00	00 mV)		· ·																					_
0x104: Voltage Resolution	Vo	ltag	e reso	oluti	on (()x80	000 0	1F4 :	= :	500 u'	V)																							
0x108: Current Range	Cui	rren	t rang	ge (0)x00	0 00	3E8 :	= 100	00) uA)																								
0x10c: Current Resolution	Cui	rren	t reso	olutio	on (C	x00	00 00)32 =	= 5	50 nA))																							
0x120: Trigger																	Νι	ımb	er	of t	rigg	er (1	(8)											
0x130: Stimulation Memory																	Νι	ımb	er	of r	nem	nory	cha	nne	els	(36	5)							
0x140: DAC Properties	Nu	mbe	er of l	DAC	C Ch	anne	els (3	6)									Nu	ımb	er	of I	OAC	C me	mo	ry c	ha	nne	els	(18	3)					
0x144: DAC Resolution																	Re	solı	utio	n i	n bi	ts (1	6)											
0x150: Sideband Properties	Nu	mbe	er of	sidel	oand	s (30	5)										Νι	ımb	er	of s	idel	oand	me	emo	ry	cha	anı	nels	s (1	8)				
0x160: Number of Stimulation Electrodes																	Sti	mu	lati	on	Elec	etroc	les	(250	6)									
0x170: Memory Configuration	Me	moi	ry siz	e pe	r cha	inne	1 in 3	2 bit	t e	ntries	(0x0	002	20 0000) = 2	М	entr	ies)																	
0x174: Total Memory Size	Me	moi	ry siz	e in	32 b	it er	itries	(0x0)4(00 000	00 =	64	4 M ent	ires)	1																			

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	0
0x200: Memory				•									•									•		•	Se	egn	ent	Se	lect	or*	
Control Register for																															
DAC in Memory																															
Group 0																															
0x201: Start Pointer for DAC in Memory Group 0	Sta	rt M	emo	ory Po	ointe	er																			ı						
0x202: End Pointer	Enc	d Me	mo	ry Po	inte	r																									
for DAC in Memory																															
Group 0																															

0x203: Write Pointer for DAC in Memory Group 0	Write Memory Pointer, write will clear Channel	
0x208: Memory Control Register for SBS in Memory Group 0		Segment Selector*
0x209: Start Pointer for SBS in Memory Group 0	Start Memory Pointer	
0x20a: End Pointer for SBS in Memory Group 0	End Memory Pointer	
0x20b: Write Pointer for SBS in Memory Group 0	Write Memory Pointer, write will clear Channel	
0x210: Memory Control Register for DAC in Memory Group 1		Segment Selector*
0x211: Start Pointer for DAC in Memory Group 1	Start Memory Pointer	
0x212: End Pointer for DAC in Memory Group 1	End Memory Pointer	
0x213: Write Pointer for DAC in Memory Group 1	Write Memory Pointer, write will clear Channel	
0x218: Memory Control Register for SBS in Memory Group 1		Segment Selector*
0x219: Start Pointer for SBS in Memory Group 1	Start Memory Pointer	
0x21a: End Pointer for SBS in Memory Group 1	End Memory Pointer	
0x21b: Write Pointer for SBS in Memory Group 1	Write Memory Pointer, write will clear Channel	
0x220: Memory Control Register for DAC in Memory Group 2		Segment Selector*
0x221: Start Pointer for DAC in Memory Group 2	Start Memory Pointer	

0x222: End Pointer for DAC in Memory Group 2	End Memory Pointer	
0x223: Write Pointer for DAC in Memory Group 2	Write Memory Pointer, write will clear Channel	
0x228: Memory Control Register for SBS in Memory Group 2		Segment Selector*
0x229: Start Pointer for SBS in Memory Group 2	Start Memory Pointer	
0x22a: End Pointer for SBS in Memory Group 2	End Memory Pointer	
0x22b: Write Pointer for SBS in Memory Group 2	Write Memory Pointer, write will clear Channel	
0x230: Memory Control Register for DAC in Memory Group 3		Segment Selector*
0x231: Start Pointer for DAC in Memory Group 3	Start Memory Pointer	
0x232: End Pointer for DAC in Memory Group 3	End Memory Pointer	
0x233: Write Pointer for DAC in Memory Group 3	Write Memory Pointer, write will clear Channel	
0x238: Memory Control Register for SBS in Memory Group 3		Segment Selector*
0x239: Start Pointer for SBS in Memory Group 3	Start Memory Pointer	
0x23a: End Pointer for SBS in Memory Group 3	End Memory Pointer	
0x23b: Write Pointer for SBS in Memory Group 3	Write Memory Pointer, write will clear Channel	
0x240: Memory Control Register for DAC in Memory Group 4		Segment Selector*

0x241: Start Pointer for DAC in Memory Group 4	Start Memory Pointer	
0x242: End Pointer for DAC in Memory Group 4	End Memory Pointer	
0x243: Write Pointer for DAC in Memory Group 4	Write Memory Pointer, write will clear Channel	
0x248: Memory Control Register for SBS in Memory Group 4		Segment Selector*
0x249: Start Pointer for SBS in Memory Group 4	Start Memory Pointer	
0x24a: End Pointer for SBS in Memory Group 4	End Memory Pointer	
0x24b: Write Pointer for SBS in Memory Group 4	Write Memory Pointer, write will clear Channel	
0x250: Memory Control Register for DAC in Memory Group 5		Segment Selector*
0x251: Start Pointer for DAC in Memory Group 5	Start Memory Pointer	
0x252: End Pointer for DAC in Memory Group 5	End Memory Pointer	
0x253: Write Pointer for DAC in Memory Group 5	Write Memory Pointer, write will clear Channel	
0x258: Memory Control Register for SBS in Memory Group 5		Segment Selector*
0x259: Start Pointer for SBS in Memory Group 5	Start Memory Pointer	
0x25a: End Pointer for SBS in Memory Group 5	End Memory Pointer	
0x25b: Write Pointer for SBS in Memory Group 5	Write Memory Pointer, write will clear Channel	

0.260.16		G . G 1 . *
0x260: Memory		Segment Selector*
Control Register for DAC in Memory		
Group 6		
Group o		
0x261: Start Pointer	Start Memory Pointer	
for DAC in Memory		
Group 6		
0x262: End Pointer	End Memory Pointer	
for DAC in Memory	End Memory Forner	
Group 6		
Group o		
0x263: Write Pointer	Write Memory Pointer, write will clear Channel	
for DAC in Memory		
Group 6		
0x268: Memory		Segment Selector*
Control Register for		Segment Selector
SBS in Memory		
Group 6		
Group o		
0x269: Start Pointer	Start Memory Pointer	
for SBS in Memory		
Group 6		
0x26a: End Pointer	End Memory Pointer	
for SBS in Memory	End Memory Former	
Group 6		
Стоир о		
0x26b: Write Pointer	Write Memory Pointer, write will clear Channel	
for SBS in Memory		
Group 6		
0x270: Memory		Segment Selector*
Control Register for		C
DAC in Memory		
Group 7		
0x271: Start Pointer	Start Memory Pointer	
for DAC in Memory		
Group 7		
0x272: End Pointer	End Memory Pointer	
for DAC in Memory		
Group 7		
0x273: Write Pointer	Write Memory Pointer, write will clear Channel	
for DAC in Memory	with Memory Former, with win crear Channel	
1		
Group 7		
0x278: Memory		Segment Selector*
Control Register for		
SBS in Memory		
Group 7		
0x279: Start Pointer	Start Memory Pointer	
for SBS in Memory		
Group 7		
0x27a: End Pointer	End Memory Pointer	
for SBS in Memory		
Group 7		

0x27b: Write Pointer	Write Memory Pointer, write will clear Channel	
for SBS in Memory Group 7		
0x280: Memory		Segment Selector*
Control Register for		
DAC in Memory		
Group 8		
0x281: Start Pointer	Start Memory Pointer	
for DAC in Memory		
Group 8		
0x282: End Pointer	End Memory Pointer	
for DAC in Memory		
Group 8		
0x283: Write Pointer	Write Memory Pointer, write will clear Channel	
for DAC in Memory	white Memory Foliner, write will clear Channel	
Group 8		
		<u> </u>
0x288: Memory		Segment Selector*
Control Register for		
SBS in Memory		
Group 8		
0x289: Start Pointer	Start Memory Pointer	
for SBS in Memory		
Group 8		
0x28a: End Pointer	End Memory Pointer	
for SBS in Memory		
Group 8		
0x28b: Write Pointer	Write Memory Pointer, write will clear Channel	
for SBS in Memory	The Herioty Foliation, while the Chamber	
Group 8		
		0 (01 (*
0x290: Memory Control Register for		Segment Selector*
DAC in Memory		
Group 9		
0x291: Start Pointer	Start Memory Pointer	
for DAC in Memory Group 9		
Group 9		
0x292: End Pointer	End Memory Pointer	
for DAC in Memory		
Group 9		
0x293: Write Pointer	Write Memory Pointer, write will clear Channel	
for DAC in Memory		
Group 9		
0x298: Memory		Segment Selector*
Control Register for		Segment Selector
SBS in Memory		
Group 9		
	Chart Manager Delates	
0x299: Start Pointer for SBS in Memory	Start Memory Pointer	
Group 9		
Group /		

0x29a: End Pointer for SBS in Memory Group 9	End Memory Pointer	
0x29b: Write Pointer for SBS in Memory Group 9	Write Memory Pointer, write will clear Channel	
0x2a0: Memory Control Register for DAC in Memory Group 10		Segment Selector*
0x2a1: Start Pointer for DAC in Memory Group 10	Start Memory Pointer	
0x2a2: End Pointer for DAC in Memory Group 10	End Memory Pointer	
0x2a3: Write Pointer for DAC in Memory Group 10	Write Memory Pointer, write will clear Channel	
0x2a8: Memory Control Register for SBS in Memory Group 10		Segment Selector*
0x2a9: Start Pointer for SBS in Memory Group 10	Start Memory Pointer	
0x2aa: End Pointer for SBS in Memory Group 10	End Memory Pointer	
0x2ab: Write Pointer for SBS in Memory Group 10	Write Memory Pointer, write will clear Channel	
0x2b0: Memory Control Register for DAC in Memory Group 11		Segment Selector*
0x2b1: Start Pointer for DAC in Memory Group 11	Start Memory Pointer	
0x2b2: End Pointer for DAC in Memory Group 11	End Memory Pointer	
0x2b3: Write Pointer for DAC in Memory Group 11	Write Memory Pointer, write will clear Channel	
0x2b8: Memory Control Register for SBS in Memory Group 11		Segment Selector*

0x2b9: Start Pointer for SBS in Memory Group 11	Start Memory Pointer	
0x2ba: End Pointer for SBS in Memory Group 11	End Memory Pointer	
0x2bb: Write Pointer for SBS in Memory Group 11	Write Memory Pointer, write will clear Channel	
0x2c0: Memory Control Register for DAC in Memory Group 12		Segment Selector*
0x2c1: Start Pointer for DAC in Memory Group 12	Start Memory Pointer	
0x2c2: End Pointer for DAC in Memory Group 12	End Memory Pointer	
0x2c3: Write Pointer for DAC in Memory Group 12	Write Memory Pointer, write will clear Channel	
0x2c8: Memory Control Register for SBS in Memory Group 12		Segment Selector*
0x2c9: Start Pointer for SBS in Memory Group 12	Start Memory Pointer	
0x2ca: End Pointer for SBS in Memory Group 12	End Memory Pointer	
0x2cb: Write Pointer for SBS in Memory Group 12	Write Memory Pointer, write will clear Channel	
0x2d0: Memory Control Register for DAC in Memory Group 13		Segment Selector*
0x2d1: Start Pointer for DAC in Memory Group 13	Start Memory Pointer	
0x2d2: End Pointer for DAC in Memory Group 13	End Memory Pointer	
0x2d3: Write Pointer for DAC in Memory Group 13	Write Memory Pointer, write will clear Channel	

Control Register for SBS in Memory Group 13 Ox.269: Start Pointer for SBS in Memory Fointer for	0x2d8: Memory Control Register for		Segment Selector*
SBS in Memory Group 13 Ox.249: Start Pointer for SBS in Memory Group 13 Ox.249: Start Pointer for SBS in Memory Group 13 Ox.240: Memory Group 13 Ox.240: Memory Group 13 Ox.240: Memory Control Register for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for DAC in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 14 Ox.240: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15 Ox.241: Start Pointer for SBS in Memory Group 15			
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0x.2da: End Pointer for SBS in Memory foroup 13 0x.2db: Write Pointer for SBS in Memory Control Register for DAC in Memory Control Register for DAC in Memory Group 14 0x.2e2: End Pointer for DAC in Memory Group 14 0x.2e3: Write Pointer for DAC in Memory Group 14 0x.2e3: Write Pointer for DAC in Memory Group 14 0x.2e4: Memory Control Register for DAC in Memory Group 14 0x.2e5: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Control Register for SBS in Memory Group 14 0x.2e8: Memory Group 15 Sagment Selector** Segment Selector*	-		
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Onzel Memory Control Register for DAC in Memory Group 14 Onzel : Start Memory Pointer for DAC in Memory Group 14 Onzel : Start Memory Pointer for DAC in Memory Group 14 Onzel : Start Memory Pointer for DAC in Memory Group 14 Onzel : Memory Group 14 Onzel : Write Pointer for DAC in Memory Group 14 Onzel : Write Memory Pointer, write will clear Channel for DAC in Memory Group 14 Onzel : Memory Group 14 Onzel : Memory Group 14 Onzel : Start Memory Group 14 Onzel : Memory Group 14 Onzel : Bart Memory Group 14 Onzel : Bart Memory Group 14 Onzel : Memory Group 15		Write Memory Pointer, write will clear Channel	
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0x2e8: Memory Control Register for SBS in Memory Group 14 0x2e9: Start Pointer for SBS in Memory Group 14 0x2ea: End Pointer for SBS in Memory Group 14 0x2ea: End Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 15 Segment Selector*	for DAC in Memory		
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Group 14 0x2e9: Start Pointer for SBS in Memory Group 14 0x2ea: End Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15 Start Memory Pointer Start Memory Pointer Start Memory Pointer	Control Register for		
Ox2e9: Start Pointer for SBS in Memory Group 14 Ox2ea: End Pointer for SBS in Memory Group 14 Ox2eb: Write Pointer for SBS in Memory Group 14 Ox2eb: Write Pointer for SBS in Memory Group 14 Ox2eb: Write Pointer for SBS in Memory Group 15 Segment Selector* Segment Selector* Start Memory Pointer Segment Selector* Segment Selector*	SBS in Memory		
for SBS in Memory Group 14 0x2ea: End Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	Group 14		
Group 14 0x2ea: End Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	0x2e9: Start Pointer	Start Memory Pointer	
Ox2ea: End Pointer for SBS in Memory Group 14 Ox2eb: Write Pointer for SBS in Memory Group 14 Ox2f0: Memory Control Register for DAC in Memory Group 15 Ox2f1: Start Pointer for DAC in Memory Group 15	for SBS in Memory	·	
for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	Group 14		
for SBS in Memory Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	0x2ea: End Pointer	End Memory Pointer	
Group 14 0x2eb: Write Pointer for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	for SBS in Memory		
for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	Group 14		
for SBS in Memory Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	0x2eb: Write Pointer	Write Memory Pointer write will clear Channel	
Group 14 0x2f0: Memory Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15	for SBS in Memory		
Ox2f0: Memory Control Register for DAC in Memory Group 15 Ox2f1: Start Pointer for DAC in Memory Group 15	Group 14		
Control Register for DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15			Segment Selector*
DAC in Memory Group 15 0x2f1: Start Pointer for DAC in Memory Group 15 Start Memory Pointer			Segment Selector
Group 15 0x2f1: Start Pointer for DAC in Memory Group 15 Start Memory Pointer			
0x2f1: Start Pointer for DAC in Memory Group 15	Group 15		
for DAC in Memory Group 15		Start Memory Pointer	
Group 15		Start Memory 1 Office	
UXZ1Z; EDIO PODICE EDIO IMEMOTY PODICE		End Mamouri Pointon	
	for DAC in Memory	End Memory Pointer	
	Group 15		

0x2f3: Write Pointer for DAC in Memory Group 15	Write Memory Pointer, write will clear Channel	
0x2f8: Memory Control Register for SBS in Memory Group 15		Segment Selector*
0x2f9: Start Pointer for SBS in Memory Group 15	Start Memory Pointer	
0x2fa: End Pointer for SBS in Memory Group 15	End Memory Pointer	
0x2fb: Write Pointer for SBS in Memory Group 15	Write Memory Pointer, write will clear Channel	
0x300: Memory Control Register for DAC in Memory Group 16		Segment Selector*
0x301: Start Pointer for DAC in Memory Group 16	Start Memory Pointer	
0x302: End Pointer for DAC in Memory Group 16	End Memory Pointer	
0x303: Write Pointer for DAC in Memory Group 16	Write Memory Pointer, write will clear Channel	
0x308: Memory Control Register for SBS in Memory Group 16		Segment Selector*
0x309: Start Pointer for SBS in Memory Group 16	Start Memory Pointer	
0x30a: End Pointer for SBS in Memory Group 16	End Memory Pointer	
0x30b: Write Pointer for SBS in Memory Group 16	Write Memory Pointer, write will clear Channel	
0x310: Memory Control Register for DAC in Memory Group 17		Segment Selector*
0x311: Start Pointer for DAC in Memory Group 17	Start Memory Pointer	

0x312: End Pointer for DAC in Memory Group 17	End Memory Pointer	
0x313: Write Pointer for DAC in Memory Group 17	Write Memory Pointer, write will clear Channel	
0x318: Memory Control Register for SBS in Memory Group 17		Segment Selector*
0x319: Start Pointer for SBS in Memory Group 17	Start Memory Pointer	
0x31a: End Pointer for SBS in Memory Group 17	End Memory Pointer	
0x31b: Write Pointer for SBS in Memory Group 17	Write Memory Pointer, write will clear Channel	

*Segment Selector:

Segment 0 to 255 reflect the Segment ID 0 to 255 from Trigger CTRL logic.

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	1	9	8	7	6 5	4	3 2	1 0
0x600: Trigger 0 Control Register			ı			ı	l				ı	ı	1							1	1				Tri	gger	conf	igura	ntion*
0x601: Trigger 1 Control Register																									Tri	gger	conf	igura	ntion*
0x602: Trigger 2 Control Register																									Tri	gger	conf	igura	ntion*
0x603: Trigger 3 Control Register																									Tri	gger	conf	igura	ntion*
0x604: Trigger 4 Control Register																									Tri	gger	conf	igura	ntion*
0x605: Trigger 5 Control Register																									Tri	gger	conf	igura	ntion*
0x606: Trigger 6 Control Register																									Tri	gger	conf	igura	ntion*
0x607: Trigger 7 Control Register																									Tri	gger	conf	igura	ntion*
0x608: Trigger 8 Control Register																									Tri	gger	conf	igura	ntion*
0x609: Trigger 9 Control Register																									Tri	gger	conf	igura	ntion*
0x60a: Trigger 10 Control Register																									Tri	gger	conf	igura	ntion*
0x60b: Trigger 11 Control Register																									Tri	gger	conf	igura	ntion*

0x60c: Trigger 12 Control Register				Trigger configuration*
0x60d: Trigger 13 Control Register				Trigger configuration*
0x60e: Trigger 14 Control Register				Trigger configuration*
0x60f: Trigger 15 Control Register				Trigger configuration*
0x610: Trigger 16 Control Register				Trigger configuration*
0x611: Trigger 17 Control Register				Trigger configuration*
0x640: Stop Trigger		Trigger	17 to 0, 1 bit per trigger	
0x644: Trigger Speed Monitor			Trigger speed**	
0x680: Trigger 0 event limit	Stop trigger after this number of events			
0x681: Trigger 1 event limit	Stop trigger after this number of events			
0x682: Trigger 2 event limit	Stop trigger after this number of events			
0x683: Trigger 3 event limit	Stop trigger after this number of events			
0x684: Trigger 4 event limit	Stop trigger after this number of events			
0x685: Trigger 5 event limit	Stop trigger after this number of events			
0x686: Trigger 6 event limit	Stop trigger after this number of events			
0x687: Trigger 7 event limit	Stop trigger after this number of events			
0x688: Trigger 8 event limit	Stop trigger after this number of events			
0x689: Trigger 9 event limit	Stop trigger after this number of events			
0x68a: Trigger 10 event limit	Stop trigger after this number of events			
0x68b: Trigger 11 event limit	Stop trigger after this number of events			
0x68c: Trigger 12 event limit	Stop trigger after this number of events			
0x68d: Trigger 13 event limit	Stop trigger after this number of events			
0x68e: Trigger 14 event limit	Stop trigger after this number of events			
0x68f: Trigger 15 event limit	Stop trigger after this number of events			

0x690: Trigger 16 event limit	Stop trigger after this number of events
0x691: Trigger 17 event limit	Stop trigger after this number of events
0x6c0: Trigger 0 event counter	current trigger events
0x6c1: Trigger 1 event counter	current trigger events
0x6c2: Trigger 2 event counter	current trigger events
0x6c3: Trigger 3 event counter	current trigger events
0x6c4: Trigger 4 event counter	current trigger events
0x6c5: Trigger 5 event counter	current trigger events
0x6c6: Trigger 6 event counter	current trigger events
0x6c7: Trigger 7 event counter	current trigger events
0x6c8: Trigger 8 event counter	current trigger events
0x6c9: Trigger 9 event counter	current trigger events
0x6ca: Trigger 10 event counter	current trigger events
0x6cb: Trigger 11 event counter	current trigger events
0x6cc: Trigger 12 event counter	current trigger events
0x6cd: Trigger 13 event counter	current trigger events
0x6ce: Trigger 14 event counter	current trigger events
0x6cf: Trigger 15 event counter	current trigger events
0x6d0: Trigger 16 event counter	current trigger events
0x6d1: Trigger 17 event counter	current trigger events
0x700: Trigger 0 repeat limit	number of times to reapeat a trigger
0x701: Trigger 1 repeat limit	number of times to reapeat a trigger
0x702: Trigger 2 repeat limit	number of times to reapeat a trigger

0x703: Trigger 3 repeat limit	number of times to reapeat a trigger
0x704: Trigger 4 repeat limit	number of times to reapeat a trigger
0x705: Trigger 5 repeat limit	number of times to reapeat a trigger
0x706: Trigger 6 repeat limit	number of times to reapeat a trigger
0x707: Trigger 7 repeat limit	number of times to reapeat a trigger
0x708: Trigger 8 repeat limit	number of times to reapeat a trigger
0x709: Trigger 9 repeat limit	number of times to reapeat a trigger
0x70a: Trigger 10 repeat limit	number of times to reapeat a trigger
0x70b: Trigger 11 repeat limit	number of times to reapeat a trigger
0x70c: Trigger 12 repeat limit	number of times to reapeat a trigger
0x70d: Trigger 13 repeat limit	number of times to reapeat a trigger
0x70e: Trigger 14 repeat limit	number of times to reapeat a trigger
0x70f: Trigger 15 repeat limit	number of times to reapeat a trigger
0x710: Trigger 16 repeat limit	number of times to reapeat a trigger
0x711: Trigger 17 repeat limit	number of times to reapeat a trigger
0x740: Trigger 0 repeat counter	current trigger repeats
0x741: Trigger 1 repeat counter	current trigger repeats
0x742: Trigger 2 repeat counter	current trigger repeats
0x743: Trigger 3 repeat counter	current trigger repeats
0x744: Trigger 4 repeat counter	current trigger repeats
0x745: Trigger 5 repeat counter	current trigger repeats
0x746: Trigger 6 repeat counter	current trigger repeats
0x747: Trigger 7 repeat counter	current trigger repeats

0x748: Trigger 8 repeat counter	current trigger repeats
0x749: Trigger 9 repeat counter	current trigger repeats
0x74a: Trigger 10 repeat counter	current trigger repeats
0x74b: Trigger 11 repeat counter	current trigger repeats
0x74c: Trigger 12 repeat counter	current trigger repeats
0x74d: Trigger 13 repeat counter	current trigger repeats
0x74e: Trigger 14 repeat counter	current trigger repeats
0x74f: Trigger 15 repeat counter	current trigger repeats
0x750: Trigger 16 repeat counter	current trigger repeats
0x751: Trigger 17 repeat counter	current trigger repeats
0x780: Trigger 0 segment ID	current segment ID
0x781: Trigger 1 segment ID	current segment ID
0x782: Trigger 2 segment ID	current segment ID
0x783: Trigger 3 segment ID	current segment ID
0x784: Trigger 4 segment ID	current segment ID
0x785: Trigger 5 segment ID	current segment ID
0x786: Trigger 6 segment ID	current segment ID
0x787: Trigger 7 segment ID	current segment ID
0x788: Trigger 8 segment ID	current segment ID
0x789: Trigger 9 segment ID	current segment ID
0x78a: Trigger 10 segment ID	current segment ID
0x78b: Trigger 11 segment ID	current segment ID
0x78c: Trigger 12 segment ID	current segment ID

0x78d: Trigger 13 segment ID	current segment ID
0x78e: Trigger 14 segment ID	current segment ID
0x78f: Trigger 15 segment ID	current segment ID
0x790: Trigger 16 segment ID	current segment ID
0x791: Trigger 17 segment ID	current segment ID

*Trigger configuration:

```
Bit 0: Enable Trigger: not Armed -> Armed

Bit 3:1:

0: Stop stimulus sequence at recuring of same trigger event

1: Restart stimulus sequence at recuring of same trigger event

2: Ignore same trigger and continue processing

3: Gate stimulus sequence at trigger event

Bit 5:4:

0: Stop stimulus sequence at occuring of other trigger event

1: Restart stimulus sequence at occuring of other trigger event

2: Ignore other trigger and continue processing

bit 7-6: Status of Trigger statemachine (00: not Armed, 01: Armed, 10: Triggerd (running), 11: Reserved)
```

**Trigger speed:

Value	STG speed
0x00	12.5 kHz
0x01	25 kHz
0x02	50 kHz (default)
0x03	100 kHz
0x04	200 kHz
0x05	400 kHz

Register	31	3	0 29	28	27	26	25	24	23	22	21	20	19	1	18	17	16	15	14	13	12	11	10	9	8	7	6	5 5	4	3	2	1 0
0x800:													-				used for						1	Data	a	Т	rig	ger	nu	mbe	r us	ed
Memory																	DAC							Sou	rce	* to	st	art	this	s cha	nne	:1
Group 0																	Data(RO)															
DAC Data																																
Read																																
Configuration																																
0x801:																	used for							Data	a	Т	rig	ger	nu	mbe	r us	ed
Memory																	DAC							Sou	rce	* to	st	art	this	s cha	nne	1
Group 0																	Data(RO)															
SBS Data																																
Read																																
Configuration																																

0x802:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 1	Data(RO)		
DAC Data			
Read			
Configuration			
0x803:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 1	Data(RO)	Source	to start tins channel
SBS Data	Data(NO)		
Read			
Configuration			
0x804:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 2	Data(RO)		
DAC Data			
Read			
Configuration			
0x805:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 2	Data(RO)		
SBS Data			
Read			
Configuration			
0x806:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 3	Data(RO)		
DAC Data			
Read			
Configuration			
0x807:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 3	Data(RO)	Source	
SBS Data	2(110)		
Read			
Configuration			
	1.0	D.	Triange
0x808:	used for DAC	Data Source*	Trigger number used to start this channel
Memory Group 4		Source*	to start this channel
Group 4 DAC Data	Data(RO)		
Read Read			
Configuration			
0x809:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 4	Data(RO)		
SBS Data			
Read			
Configuration			
0x80a:	used for	Data	Trigger number used
Memory	DAC	Source*	to start this channel
Group 5	Data(RO)		
DAC Data			
Read			
Configuration			

0x80b:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 5	Data(RO)	
SBS Data		
Read		
Configuration		
0x80c:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 6	Data(RO)	
DAC Data		
Read		
Configuration		
0x80d:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 6	Data(RO)	Source to start this channel
SBS Data	Data(NO)	
Read		
Configuration		
	10	D
0x80e:	used for	Data Trigger number used
Memory	DAC Data(DO)	Source* to start this channel
Group 7	Data(RO)	
DAC Data Read		
Configuration		
0x80f:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 7	Data(RO)	
SBS Data		
Read		
Configuration		
0x810:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 8	Data(RO)	
DAC Data		
Read		
Configuration		
0x811:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 8	Data(RO)	
SBS Data		
Read		
Configuration		
0x812:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 9	Data(RO)	Source to start time charmer
DAC Data	(****)	
Read		
Configuration		
0x813:	used for	Data Trigger number used
Memory	DAC	Source* to start this channel
Group 9	Data(RO)	to start this chailler
SBS Data	Data(NO)	
Read		
Configuration		
- Constitution		

0x814:	used for	Data Trigger number u	used
Memory	DAC	Source* to start this chann	
Group 10	Data(RO)		
DAC Data			
Read			
Configuration			
0x815:	used for	Data Trigger number u	used
Memory	DAC	Source* to start this chann	nel
Group 10	Data(RO)		
SBS Data			
Read			
Configuration			
0x816:	used for	Data Trigger number u	
Memory	DAC	Source* to start this chann	nel
Group 11	Data(RO)		
DAC Data			
Read Configuration			
0x817:	used for	Data Trigger number i	
Memory	DAC	Source* to start this chann	nel
Group 11 SBS Data	Data(RO)		
Read			
Configuration			
	1.0	D	1
0x818:	used for DAC	Data Trigger number to start this change	
Memory Group 12	Data(RO)	Source. to start this chain	nei
DAC Data	Data(NO)		
Read			
Configuration			
0x819:	used for	Data Trigger number u	used
Memory	DAC	Source* to start this chan	
Group 12	Data(RO)		
SBS Data			
Read			
Configuration			
0x81a:	used for	Data Trigger number u	used
Memory	DAC	Source* to start this chann	
Group 13	Data(RO)		
DAC Data			
Read			
Configuration			
0x81b:	used for	Data Trigger number to	
Memory	DAC	Source* to start this chann	nel
Group 13	Data(RO)		
SBS Data			
Read Configuration			
Configuration			
0x81c:	used for	Data Trigger number u	
Memory	DAC	Source* to start this chann	nel
Group 14	Data(RO)		
DAC Data Read			
Configuration			
Comiguration			

0x81d: Memory Group 14 SBS Data Read	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
Configuration				
0x81e: Memory Group 15 DAC Data Read Configuration	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x81f:	used for		Data	Trigger number used
Memory Group 15 SBS Data Read Configuration	DAC Data(RO)		Source*	to start this channel
0x820: Memory Group 16 DAC Data Read Configuration	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x821: Memory Group 16 SBS Data Read Configuration	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x822: Memory Group 17 DAC Data Read Configuration	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x823: Memory Group 17 SBS Data Read Configuration	used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x880: Memory Group 0 static value for DAC		value used in manual mo	de	
0x881: Memory Group 0 static value for SBS		value used in manual mo	de	

0x882:	
	value used in manual mode
Memory	
Group 1	
static value	
for DAC	
0x883:	value used in manual mode
Memory	
Group 1	
static value	
for SBS	
101 303	
0x884:	value used in manual mode
Memory	
Group 2	
static value	
for DAC	
101 DAC	
0x885:	 value used in manual mode
Memory	
Group 2	
static value	
for SBS	
0x886:	value used in manual mode
Memory	
Group 3	
static value	
for DAC	
0x887:	value used in manual mode
Memory	
Group 3	
static value	
Static value	
for SBS	
	value used in manual mode
for SBS 0x888:	value used in manual mode
for SBS 0x888: Memory	value used in manual mode
for SBS 0x888: Memory Group 4	value used in manual mode
for SBS 0x888: Memory Group 4 static value	value used in manual mode
for SBS 0x888: Memory Group 4	value used in manual mode
for SBS 0x888: Memory Group 4 static value	value used in manual mode value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889:	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value	
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a:	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value	value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value for DAC 0x88b:	value used in manual mode value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value for DAC 0x88b: Memory	value used in manual mode value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value for DAC 0x88b: Memory Group 5	value used in manual mode value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value for DAC 0x88b: Memory Group 5 static value	value used in manual mode value used in manual mode
for SBS 0x888: Memory Group 4 static value for DAC 0x889: Memory Group 4 static value for SBS 0x88a: Memory Group 5 static value for DAC 0x88b: Memory Group 5	value used in manual mode value used in manual mode

0x88c:	value used in manual mode
Memory	
Group 6	
static value	
for DAC	
0x88d:	value used in manual mode
Memory	
Group 6	
static value	
for SBS	
101 3D3	
0x88e:	value used in manual mode
Memory	
Group 7	
static value	
for DAC	
101 DAC	
0x88f:	value used in manual mode
Memory	
Group 7	
static value	
for SBS	
0x890:	value used in manual mode
Memory	
Group 8	
static value	
for DAC	
0x891:	value used in manual mode
Memory	
Group 8	
Group 8	
static value	
static value	value used in manual mode
static value for SBS 0x892:	value used in manual mode
static value for SBS 0x892: Memory	value used in manual mode
static value for SBS 0x892: Memory Group 9	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value	value used in manual mode
static value for SBS 0x892: Memory Group 9	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value	value used in manual mode value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893:	
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory	
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9	
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value	
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static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value	
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894:	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC	value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC 0x895:	value used in manual mode value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC 0x895: Memory	value used in manual mode value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC 0x895: Memory Group 10	value used in manual mode value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC 0x895: Memory Group 10 static value for DAC	value used in manual mode value used in manual mode
static value for SBS 0x892: Memory Group 9 static value for DAC 0x893: Memory Group 9 static value for SBS 0x894: Memory Group 10 static value for DAC 0x895: Memory Group 10	value used in manual mode value used in manual mode

0x896:	value used in manual mode
Memory	
Group 11	
static value	
for DAC	
0x897:	value used in manual mode
Memory	
Group 11	
static value	
for SBS	
101 203	
0x898:	value used in manual mode
Memory	
Group 12	
static value	
for DAC	
0x899:	 value used in manual mode
Memory	
Group 12	
static value	
for SBS	
101 303	
0x89a:	value used in manual mode
Memory	
Group 13	
static value	
for DAC	
IOI DAC	
0x89b:	 value used in manual mode
Memory	
Group 13	
-10mp 15	
static value	
static value	
static value for SBS	
	value used in manual mode
for SBS 0x89c:	value used in manual mode
for SBS 0x89c: Memory	value used in manual mode
for SBS 0x89c: Memory Group 14	value used in manual mode
for SBS 0x89c: Memory Group 14 static value	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC	
for SBS 0x89c: Memory Group 14 static value	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC	
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory	
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14	
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value	
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e:	
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e:	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC 0x89f:	value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC 0x89f:	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC 0x89f: Memory Group 15	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC 0x89f: Memory Group 15 static value	value used in manual mode value used in manual mode
for SBS 0x89c: Memory Group 14 static value for DAC 0x89d: Memory Group 14 static value for SBS 0x89e: Memory Group 15 static value for DAC 0x89f: Memory Group 15	value used in manual mode value used in manual mode

0x8a0:		value used in manual mode
Memory		
Group 16		
static value		
for DAC		
0x8a1:		value used in manual mode
Memory		
Group 16		
static value		
for SBS		
0x8a2:		value used in manual mode
Memory		vario usea in manual mode
Group 17		
static value		
for DAC		
101 DAC		
0x8a3:		value used in manual mode
Memory		
Group 17		
static value		
for SBS		
0x900: Read	current read pointer position of read FSM	
pointer of		
Memory		
Group 0 for		
DAC		
0x901: Read	current read pointer position of read FSM	
pointer of	earrone read pointer position of read 15M	
Memory		
Group 0 for		
SBS		
0x902: Read	current read pointer position of read FSM	
pointer of		
Memory		
Group 1 for		
DAC		
0x903: Read	gurrant road pointer position of road FCM	
	current read pointer position of read FSM	
pointer of		
Memory		
Group 1 for		
SBS		
0x904: Read	current read pointer position of read FSM	
pointer of		
Memory		
Group 2 for		
DAC		
0x905: Read	current read pointer position of read FSM	
pointer of		
Memory		
Group 2 for		
SBS		

0x906: Read pointer of Memory Group 3 for DAC	current read pointer position of read FSM
0x907: Read pointer of Memory Group 3 for SBS	current read pointer position of read FSM
0x908: Read pointer of Memory Group 4 for DAC	current read pointer position of read FSM
0x909: Read pointer of Memory Group 4 for SBS	current read pointer position of read FSM
0x90a: Read pointer of Memory Group 5 for DAC	current read pointer position of read FSM
0x90b: Read pointer of Memory Group 5 for SBS	current read pointer position of read FSM
0x90c: Read pointer of Memory Group 6 for DAC	current read pointer position of read FSM
0x90d: Read pointer of Memory Group 6 for SBS	current read pointer position of read FSM
0x90e: Read pointer of Memory Group 7 for DAC	current read pointer position of read FSM
0x90f: Read pointer of Memory Group 7 for SBS	current read pointer position of read FSM

0x910: Read pointer of Memory Group 8 for	current read pointer position of read FSM
DAC	
0x911: Read pointer of Memory Group 8 for SBS	current read pointer position of read FSM
0x912: Read pointer of Memory Group 9 for DAC	current read pointer position of read FSM
0x913: Read pointer of Memory Group 9 for SBS	current read pointer position of read FSM
0x914: Read pointer of Memory Group 10 for DAC	current read pointer position of read FSM
0x915: Read pointer of Memory Group 10 for SBS	current read pointer position of read FSM
0x916: Read pointer of Memory Group 11 for DAC	current read pointer position of read FSM
0x917: Read pointer of Memory Group 11 for SBS	current read pointer position of read FSM
0x918: Read pointer of Memory Group 12 for DAC	current read pointer position of read FSM
0x919: Read pointer of Memory Group 12 for SBS	current read pointer position of read FSM

0.01 =	. 1
0x91a: Read pointer of Memory Group 13 for DAC	current read pointer position of read FSM
0x91b: Read pointer of Memory Group 13 for SBS	current read pointer position of read FSM
0x91c: Read pointer of Memory Group 14 for DAC	current read pointer position of read FSM
0x91d: Read pointer of Memory Group 14 for SBS	current read pointer position of read FSM
0x91e: Read pointer of Memory Group 15 for DAC	current read pointer position of read FSM
0x91f: Read pointer of Memory Group 15 for SBS	current read pointer position of read FSM
0x920: Read pointer of Memory Group 16 for DAC	current read pointer position of read FSM
0x921: Read pointer of Memory Group 16 for SBS	current read pointer position of read FSM
0x922: Read pointer of Memory Group 17 for DAC	current read pointer position of read FSM
0x923: Read pointer of Memory Group 17 for SBS	current read pointer position of read FSM

*Data source:

00: Stim. MEM Block X as Source (default)

01: Static value (manual mode, mainly for testing)

10: DSP direct stream as Source

11: Reserved, not Valid

Register	3:	1 3	0 2	9 2	28	27	26	25	24	23	22	21	20	19	18	17	16	,	15	14	13	12	11 1	0 9	8 7	7 6	5 4 3	3 2	2			1			0
0xa10: Current Voltage Switch																																			oltage mode; urrent mode
0xa14: Impedance Ground Control	e																											DoIm	pTest	Imp	oStg_l	DoStim	ulus	ImpSi	tg_Grounding
0xa1c: Impedance STG Config		npS	tg_	Fre	que	ency													Imp	oStg	g_Aı	mplit	ude							•					
0xa80: Electrode Group* 0 Source Select																									S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	up
0xa81: Electrode Group* 1 Source Select																									S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	up
0xa82: Electrode Group* 2 Source Select																									S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	up
0xa83: Electrode Group* 3 Source Select																									S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	up
0xa84: Electrode Group* 4 Source Select																									S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	up
0xa85: Electrode Group* 5 Source Select										_															S	Selec	t Stim	ulation	Mem	ory (Group	for Ele	ectro	de Gro	ир

0xa86:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group* 6		
Source		
Select		
Select		
0xa87:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group* 7		
Source		
Select		
0xa88:	Select Stimulation	on Memory Group for Electrode Group
Electrode		in Memory Group for Elections Group
Group* 8		
Source		
Select		
0xa89:	Calcat Ctimulatia	on Memory Group for Electrode Group
Electrode	Select Stillidation	in Memory Group for Electrone Group
Group* 9		
Source		
Select		
00	0.10/1./	- Marian Carrot for Florida I. Carro
0xa8a:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group*		
10		
Source		
Select		
0xa8b:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group*		
11		
Source		
Select		
0xa8c:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group*		
12		
Source		
Select		
0xa8d:	Select Stimulation	n Memory Group for Electrode Group
Electrode		
Group*		
13		
Source		
Select		
Sciect		
0xa8e:	Select Stimulation	n Memory Group for Electrode Group
Electrode		^
Group*		
14		
Source		
Select		

0xa8f:			Select Stimulation Memory Group for Electrode Group
Electrode			
Group*			
15			
Source			
Select			
0xa90:			Select Stimulation Memory Group for Electrode Group
Electrode			
Group*			
16			
Source			
Select			
0xa91:			Select Stimulation Memory Group for Electrode Group
Electrode			
Group*			
17			
Source			
Select			
0-1-00		DACD.	
0xb00:	Enable	DAC Data	
Dac A in			
Electr.			
Gr. 0			
Data			
Register			
0xb01:	Enable	DAC Data	
Dac B in	Enable	DAC Data	
Electr.			
Gr. 0			
Data			
Register			
0xb02:	Enable	DAC Data	
Dac A in			
Electr.			
Gr. 1			
Data			
Register			
0xb03:	Enable	DAC Data	
Dac B in			
Electr.			
Gr. 1			
Data			
Register			
	n	DAC Det	
0xb04:	Enable	DAC Data	
Dac A in			
Electr.			
Gr. 2			
Data			
Register			
0xb05:	Fnahle	DAC Data	
Dac B in	Enable		
Electr.			
1 1			
Gr. 2			
Data			
Register			
		1	

0xb06:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 3		
Data		
Register		
0xb07:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 3		
Data		
Register		
0xb08:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 4		
Data		
Register		
0xb09:	Enable	DAC Data
Dac B in	Lindoic	
Electr.		
Gr. 4		
Data		
Register		
0xb0a:	Enable	DAC Data
	Lilable	DAC Data
Dac A in		
Electr.		
Gr. 5		
Data		
Register		
0xb0b:	Enoble	DAC Data
	Eliable	DAC Data
Dac B in		
Electr.		
Gr. 5		
Data		
Register		
0xb0c:	Engl-1	DAC Data
	Enable	DAC Data
Dac A in		
Electr.		
Gr. 6		
Data		
Register		
0xb0d:	E a1.1	DAC Data
	Enable	DAC Data
Dac B in		
Electr.		
Gr. 6		
Data		
Register		
OrbOo	E a1.1	DAC Data
0xb0e:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 7		
Data		
Register		

0xb0f:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 7		
Data		
Register		
0xb10:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 8		
Data		
Register		
0xb11:	Enoble	DAC Data
	Lilable	DAC Data
Dac B in		
Electr.		
Gr. 8		
Data		
Register		
Register		
0xb12:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 9		
Data		
Register		
0xb13:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 9		
Data		
Register		
0xb14:	Enoble	DAC Data
	Lilable	DAC Data
Dac A in		
Electr.		
Gr. 10		
Data		
Register		
register		
0xb15:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 10		
Data		
Register		
		D.O.D.
0xb16:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 11		
Data		
Register		
0xb17:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 11		
Data		
Register		

0xb18:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 12		
Data		
Register		
0xb19:	Enable	DAC Data
Dac B in	Litable	DITC Dutte
Electr.		
Gr. 12		
Data		
Register		
0.11	Б 11	DAGE.
0xb1a:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 13		
Data		
Register		
0xb1b:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 13		
Data		
Register		
0xb1c:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 14		
Data		
Register		
0xb1d:	Enable	DAC Data
Dac B in	Lilable	DAC Data
Electr.		
Gr. 14		
Data		
Register		
0.11.	F 1.1	DACD.
0xb1e:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 15		
Data		
Register		
0xb1f:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 15		
Data		
Register		
0xb20:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 16		
Data		
Register		
	1	

0xb21:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 16		
Data		
Register		
0xb22:	Enable	DAC Data
Dac A in		
Electr.		
Gr. 17		
Data		
Register		
0xb23:	Enable	DAC Data
Dac B in		
Electr.		
Gr. 17		
Data		
Register		
0xb80:		Offset Correction Value for DAC A in Current Mode
Offset		
Register		
for DAC		
A 0		
		Office of the page of the
0xb81:		Offset Correction Value for DAC B in Current Mode
Offset		
Register		
for DAC		
B 0		
0xb82:		Offset Correction Value for DAC A in Current Mode
Offset		Offset Coffection value for DAC A in Cuffent Mode
Register		
for DAC		
A 1		
0xb83:		Offset Correction Value for DAC B in Current Mode
Offset		STACE CONTROL OF A PARTY OF A PAR
Register		
for DAC		
B 1		
0xb84:		Offset Correction Value for DAC A in Current Mode
Offset		
Register		
for DAC		
A 2		
0xb85:		Offset Correction Value for DAC B in Current Mode
Offset		
Register		
for DAC		
B 2		
D 2		
0xb86:		Offset Correction Value for DAC A in Current Mode
Offset		
Register		
for DAC		
A 3		

0xb87:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 3	
0xb88:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 4	
A4	
0xb89:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 4	
0.10.	Officet Competing Value for DAC A in Compet Made
0xb8a:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 5	
0xb8b:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 5	
0xb8c:	Offset Correction Value for DAC A in Current Mode
	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 6	
0xb8d:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 6	
0xb8e:	Offset Correction Value for DAC A in Current Mode
	Show Content of the Prioritin Culter Production
Offset	
Register	
for DAC	
A 7	
0xb8f:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 7	
D /	
0xb90:	Offset Correction Value for DAC A in Current Mode
Offset	The state of the s
Register	
for DAC	
A 8	

0xb91:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 8	
0xb92:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 9	
,	
0xb93:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 9	
0xb94:	Offset Correction Value for DAC A in Current Mode
Offset	A A A A A A A A A A A A A A A A A A A
Register	
for DAC	
A 10	
0xb95:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 10	
0xb96:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 11	
ATI	
0xb97:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 11	
0xb98:	Offset Correction Value for DAC A in Current Mode
Offset	The state of the s
Register	
for DAC	
A 12	
0xb99:	Officet Correction Value for DAC B in Correct Medic
	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 12	
0xb9a:	Offset Correction Value for DAC A in Current Mode
Offset	Short correction value for Drie A in Current Mode
Register	
for DAC	
A 13	

0xb9b:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 13	
0xb9c:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 14	
0xb9d:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 14	
0xb9e:	Offset Correction Value for DAC A in Current Mode
Offset	office Confection Funds for Diffe II in Culture Produc
Register	
for DAC	
A 15	
0xb9f:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 15	
D 13	
0xba0:	Offset Correction Value for DAC A in Current Mode
Offset	
Register	
for DAC	
A 16	
0xba1:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 16	
0xba2:	Offset Correction Value for DAC A in Current Mode
	Offset Coffection value for DAC A in Cuffent Wode
Offset	
Register	
for DAC	
A 17	
0xba3:	Offset Correction Value for DAC B in Current Mode
Offset	
Register	
for DAC	
B 17	
D 1 /	
0xbc0:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 0	
Weighting	
Factor	
I actor	

oxbc1: DAC B in Electr. Gr. 0 Weighting Weighting Factor in Q1.16 Format DAC A in Electr. Gr. 1 Weighting Factor in Q1.16 Format Weighting Factor Weighting Factor in Q1.16 Format DAC B in Electr. Gr. 1 Weighting Factor in Q1.16 Format Weighting Factor Weighting Factor in Q1.16 Format Oxbc3: Weighting Factor in Q1.16 Format Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor in Q1.16 Format Oxbc5: Weighting Factor in Q1.16 Format DAC B in Electr. Gr. 2 Weighting Factor in Q1.16 Format
in Electr. Gr. 0 Weighting Factor Oxbc2: DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format
Gr. 0 Weighting Factor Oxbc2: DAC A in Electr. Gr. 1 Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Gr. 2 Weighting Factor in Q1.16 Format
Weighting Factor Oxbc2: DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Gr. 2 Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format
Factor Oxbc2: DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format Weighting Factor Weighting Factor in Q1.16 Format
DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Weighting Factor in Q1.16 Format Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor in Q1.16 Format
DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Weighting Factor Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format
DAC A in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Weighting Factor Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format
in Electr. Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Oxbc5: DAC B in Electr.
Gr. 1 Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Oxbc5: DAC B in Electr.
Weighting Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Oxbc5: DAC B in Electr.
Factor Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Oxbc5: DAC B in Electr.
Oxbc3: DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Oxbc5: DAC B in Electr.
DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
DAC B in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
in Electr. Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
Gr. 1 Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
Weighting Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
Factor Oxbc4: DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr.
0xbc4: DAC A in Electr. Gr. 2 Weighting Factor 0xbc5: DAC B in Electr.
DAC A in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Weighting Factor in Q1.16 Format
in Electr. Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Weighting Factor in Q1.16 Format
Gr. 2 Weighting Factor Oxbc5: DAC B in Electr. Weighting Factor in Q1.16 Format
Weighting Factor Oxbc5: DAC B in Electr. Weighting Factor in Q1.16 Format
Factor Oxbc5: DAC B in Electr. Weighting Factor in Q1.16 Format
0xbc5: Weighting Factor in Q1.16 Format DAC B in Electr.
DAC B in Electr.
DAC B in Electr.
in Electr.
Gr. 2
Weighting
Factor
0xbc6: Weighting Factor in Q1.16 Format
DAC A
in Electr.
Gr. 3
Weighting
Factor
0xbc7: Weighting Factor in Q1.16 Format
DAC B
in Electr.
Gr. 3
Weighting
Factor
0xbc8: Weighting Factor in Q1.16 Format
DAC A Weighting Factor in Q1.10 Format
in Electr.
Gr. 4
Weighting
Factor
0xbc9: Weighting Factor in Q1.16 Format
DAC B
in Electr.
Gr. 4
Weighting
Factor

0xbca:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 5	
Weighting	
Factor	
0xbcb:	Weighting Factor in Q1.16 Format
DAC B	weighting Pactor in Q1.10 Pormat
in Electr.	
Gr. 5	
Weighting	
Factor	
0xbcc:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 6	
Weighting	
Factor	
0xbcd:	Waighting Factor in O1 16 Format
DAC B	Weighting Factor in Q1.16 Format
in Electr.	
Gr. 6	
Weighting	
Factor	
0xbce:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 7	
Weighting	
Factor	
0xbcf:	Weighting Factor in Q1.16 Format
DAC B	Weighting Lactor in Q1.10 Format
in Electr.	
Gr. 7	
Weighting	
Factor	
0xbd0:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 8	
Weighting	
Factor	
0xbd1:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 8	
Weighting	
Factor	
	William Francisco (Adder
0xbd2:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 9	
Weighting	
Factor	
	•

0xbd3:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 9	
Weighting	
Factor	
0xbd4:	Weighting Factor in Q1.16 Format
DAC A	weighting Factor in Q1.10 Format
in Electr.	
Gr. 10	
Weighting	
Factor	
0xbd5:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 10	
Weighting	
Factor	
0xbd6:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 11	
Weighting	
Factor	
0xbd7:	Weighting Factor in Q1.16 Format
DAC B	Weighting Luctor in Q1.10 Format
in Electr.	
Gr. 11	
Weighting	
Factor	
0xbd8:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 12	
Weighting	
Factor	
0xbd9:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 12	
Weighting	
Factor	
0xbda:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 13	
Weighting	
Factor	
0xbdb:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 13	
Weighting	
Factor	
1 actor	

0xbde:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 14	
Weighting	
Factor	
0xbdd:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 14	
Weighting	
Factor	
0xbde:	Weighting Factor in Q1.16 Format
DAC A	weighting ractor in Q1.10 Pormat
in Electr.	
Gr. 15	
Weighting	
Factor	
0xbdf:	Weighting Factor in Q1.16 Format
DAC B	
in Electr.	
Gr. 15	
Weighting	
Factor	
0xbe0:	Weighting Factor in Q1.16 Format
DAC A	
in Electr.	
Gr. 16	
Weighting	
Factor	
0xbe1:	
	Weighting Factor in Q1.16 Format
DAC B	Weighting Factor in Q1.16 Format
	Weighting Factor in Q1.16 Format
DAC B	Weighting Factor in Q1.16 Format
DAC B in Electr.	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor	
DAC B in Electr. Gr. 16 Weighting Factor 0xbe2:	Weighting Factor in Q1.16 Format Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A	
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr.	
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17	
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr.	
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17	
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17 Weighting Factor	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor 0xbe2: DAC A in Electr. Gr. 17 Weighting Factor 0xbe3:	
DAC B in Electr. Gr. 16 Weighting Factor 0xbe2: DAC A in Electr. Gr. 17 Weighting Factor 0xbe3: DAC B	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor 0xbe2: DAC A in Electr. Gr. 17 Weighting Factor 0xbe3: DAC B in Electr.	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17 Weighting Factor Oxbe3: DAC B in Electr. Gr. 17	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17 Weighting Factor Oxbe3: DAC B in Electr. Gr. 17 Weighting	Weighting Factor in Q1.16 Format
DAC B in Electr. Gr. 16 Weighting Factor Oxbe2: DAC A in Electr. Gr. 17 Weighting Factor Oxbe3: DAC B in Electr. Gr. 17	Weighting Factor in Q1.16 Format

$^*Electrode\ Group::$

0:	Electrode	0 -	15	
1:	Electrode	16 -	29	
2:	Electrode	30 -	43	
3:	Electrode	44 -	57	

```
4: Electrode 58 - 71
5: Electrode 72 - 85
6: Electrode 86 - 99
7: Electrode 100 - 113
8: Electrode 114 - 127
9: Electrode 128 - 141
10: Electrode 142 - 155
11: Electrode 156 - 169
12: Electrode 170 - 183
13: Electrode 184 - 197
14: Electrode 212 - 225
16: Electrode 226 - 239
17: Electrode 240 - 255
```

Register	31	3	0 29	28	2	7 20	25	; :	24	23	22	21	20	19)	18	17	16	1:	5 1	14	13	12	11	10	9	8	7	6	5 4	4 3	3 2	1	0
0xc50: Electrode Config ID					1	ı		-1					1		-				1						1			Ele	ctr	ode (Con	fig I	D	
0xc51: Config ID Source																														ectro		Conf	ig II)
0xc70: Electrode Mode Configuration	Ele	ecti	rodes	31 to	0	(Mar	ual 1	no	de: '	1'/	Aut	oma	tic	mod	e: '	'0', 1	bit	per	ele	ectr	ode)												
0xc71: Electrode Mode Configuration	Ele	ecti	rodes	63 to	32	2 (Ma	nual	m	ode:	'1'	/ At	itom	natio	e mo	de:	: '0',	1 bi	it pe	r e	elect	trod	e)												
0xc72: Electrode Mode Configuration	Ele	ecti	rodes	95 to	64	l (Ma	nual	m	ode:	'1'	/ Au	itom	natio	e mo	de:	: '0',	1 bi	it pe	r e	elect	rod	e)												
0xc73: Electrode Mode Configuration	Ele	ecti	rodes	127 1	to 9	96 (M	lanua	al r	node	e: '1	' / A	uto	mat	ic m	od	e: '0'	, 1 t	bit p	er	ele	ctro	de)												
0xc74: Electrode Mode Configuration	Ele	ecti	rodes	159 1	to 1	28 (1	Manı	ıal	mod	de: '	1'/	Aut	oma	atic n	no	de: '()', 1	bit	pe	er el	ectr	ode)											
0xc75: Electrode Mode Configuration	Ele	ecti	rodes	191 1	to 1	60 (1	Manı	ıal	mod	de: '	1'/	Aut	oma	atic n	no	de: '()', 1	bit	pe	er el	ectr	ode))											
0xc76: Electrode Mode Configuration	Ele	ecti	rodes	223 1	to 1	92 (1	Manı	ıal	moo	de: '	1'/	Aut	oma	atic n	no	de: '()', 1	bit	pe	er el	ectr	ode))											
0xc77: Electrode Mode Configuration	Ele	ecti	rodes	255 1	to 2	224 (1	Manı	ıal	mod	de: '	1'/	Aut	oma	atic n	no	de: '()', 1	bit	pe	er el	ectr	ode)											
0xca0: Electrode Enable	Ele	ecti	rodes	31 to	0,	1 bit	per	ele	ectro	de																								
0xca1: Electrode Enable	Ele	ecti	rodes	63 to	32	2, 1 b	it pe	r e	lectr	ode																								

0xca2: Electrode Enable	Electrodes 95 to 64, 1 bit per electrode
0xca3: Electrode Enable	Electrodes 127 to 96, 1 bit per electrode
0xca4: Electrode Enable	Electrodes 159 to 128, 1 bit per electrode
0xca5: Electrode Enable	Electrodes 191 to 160, 1 bit per electrode
0xca6: Electrode Enable	Electrodes 223 to 192, 1 bit per electrode
0xca7: Electrode Enable	Electrodes 255 to 224, 1 bit per electrode
0xcd0: Electrode MUX position when stimulus is active	Electrodes 15 to 0, 2 bit per electrode**
0xcd1: Electrode MUX position when stimulus is active	Electrodes 31 to 16, 2 bit per electrode**
0xcd2: Electrode MUX position when stimulus is active	Electrodes 47 to 32, 2 bit per electrode**
0xcd3: Electrode MUX position when stimulus is active	Electrodes 63 to 48, 2 bit per electrode**
0xcd4: Electrode MUX position when stimulus is active	Electrodes 79 to 64, 2 bit per electrode**
0xcd5: Electrode MUX position when stimulus is active	Electrodes 95 to 80, 2 bit per electrode**
0xcd6: Electrode MUX position when stimulus is active	Electrodes 111 to 96, 2 bit per electrode**
0xcd7: Electrode MUX position when stimulus is active	Electrodes 127 to 112, 2 bit per electrode**
0xcd8: Electrode MUX position when stimulus is active	Electrodes 143 to 128, 2 bit per electrode**

0xcd9: Electrode	Electrodes 159 to 144, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcda: Electrode	Electrodes 175 to 160, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcdb: Electrode	Electrodes 191 to 176, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcdc: Electrode	Electrodes 207 to 192, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcdd: Electrode	Electrodes 223 to 208, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcde: Electrode	Electrodes 239 to 224, 2 bit per electrode**
MUX position	
when stimulus is	
active	
0xcdf: Electrode	Electrodes 255 to 240, 2 bit per electrode**
MUX position	
when stimulus is	
active	

*Electrode Config ID Source Select:

```
00 00000: Trigger 0 ID
00 00001: Trigger 1 ID
00 00010: Trigger 2 ID
00 00011: Trigger 3 ID
00 00100: Trigger 4 ID
00 00101: Trigger 5 ID
00 00110: Trigger 6 ID
00 00111: Trigger 7 ID
00 01000: Trigger 8 ID
00 01001: Trigger 9 ID
00 01010: Trigger 10 ID
00 01011: Trigger 11 ID
00 01100: Trigger 12 ID
00 01101: Trigger 13 ID
00 01110: Trigger 14 ID
00 01111: Trigger 15 ID
00 10000: Trigger 16 ID
00 10001: Trigger 17 ID
00 10010: Reserved
```

```
00 11111: Reserved
01 00000: Sideband 1, bits 15:8
01 00001: Sideband 2, bits 15:8
01 00010: Sideband 3, bits 15:8
01 00011: Sideband 4, bits 15:8
01 00100: Sideband 5, bits 15:8
01 00101: Sideband 6, bits 15:8
01 00110: Sideband 7, bits 15:8
01 00111: Sideband 8, bits 15:8
01 01000: Sideband 9, bits 15:8
01 01001: Sideband 10, bits 15:8
01 01010: Sideband 11, bits 15:8
01 01011: Sideband 12, bits 15:8
01 01100: Sideband 13, bits 15:8
01 01101: Sideband 14, bits 15:8
01 01110: Sideband 15, bits 15:8
01 01111: Sideband 16, bits 15:8
01 10000: Sideband 17, bits 15:8
01 10001: Sideband 18, bits 15:8
01 10010: Reserved
01 11111: Reserved
10 XXXXX: Manual Register
11 XXXXX: Reserved
```

**Electrode MUX position:

```
00: electrode to ADC
01: DAC 0
10: DAC 1
11: GND (Impedance test, only in manual mode)
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	(0
0xf00:	Adı	ess			•		•								•	•	•			•		•			•								
Memory Address																																	
0xf04:	Byt	e 4							Byt	e 3							Byt	e 2							B	yte	1						
Memory																																	
Data																																	
0xf10: Max																												# c	f M	laxi	mun	ı us	ed
used																												М	emo	ry (Grou	ps (1 -
Memory																												18)				
Groups																																	

0xf11:		Segments needed*
MEM		Segments needed.
Segments		
Shift		
0xf12:		Trigger
Memory		Ptr.
Pointer		Config
Config		
0xf80:	Stimulation Data Vector**	·
Memory		
Group 0		
DAC Data		
Write		
Register		
0xf81:	Stimulation Data Vector**	
Memory		
Group 0		
SBS Data		
Write		
Register		
0xf82:	Stimulation Data Vector**	
Memory		
Group 1		
DAC Data		
Write		
Register		
0xf83:	Stimulation Data Vector**	
Memory		
Group 1		
SBS Data		
Write		
Register		
0xf84:	Stimulation Data Vector**	
Memory		
Group 2		
DAC Data		
Write		
Register		
0xf85:	Stimulation Data Vector**	
Memory		
Group 2		
SBS Data		
Write		
Register		
0xf86:	Stimulation Data Vector**	
Memory		
Group 3		
DAC Data		
Write		
Register		

0.007	Oct. 1 d. D. W. and
0xf87:	Stimulation Data Vector**
Memory	
Group 3	
SBS Data	
Write	
Register	
0xf88:	Stimulation Data Vector**
Memory	
Group 4	
DAC Data	
Write	
Register	
0xf89:	Stimulation Data Vector**
	Sumulation Data Vector***
Memory Group 4	
SBS Data	
Write	
Register	
0xf8a:	Stimulation Data Vector**
Memory	
Group 5	
DAC Data	
Write	
Register	
0xf8b:	Stimulation Data Vector**
Memory	
Group 5	
SBS Data	
Write	
Register	
0xf8c:	Stimulation Data Vector**
Memory	
Group 6	
DAC Data	
Write	
Register	
0xf8d:	Stimulation Data Vector**
Memory	Sumulation Data VCCtor
Group 6	
SBS Data	
Write	
Register	
0xf8e:	Stimulation Data Vector**
Memory	
Group 7	
DAC Data	
Write	
Register	
0xf8f:	Stimulation Data Vector**
Memory	
Group 7	
SBS Data	
Write	
Register	

0xf90:	Stimulation Data Vector**
Memory	
Group 8	
DAC Data	
Write	
Register	
0xf91:	Stimulation Data Vector**
Memory	
Group 8	
SBS Data	
Write	
Register	
0xf92:	Stimulation Data Vector**
Memory	
Group 9	
DAC Data	
Write	
Register	
0xf93:	Stimulation Data Vector**
Memory	
Group 9	
SBS Data	
Write	
Register	
0xf94:	Stimulation Data Vector**
Memory	
Group 10	
DAC Data	
Write	
Register	
0xf95:	Stimulation Data Vector**
Memory	
Group 10	
SBS Data	
Write	
Register	
0xf96:	Stimulation Data Vector**
Memory	
Group 11	
DAC Data	
Write	
Register	
0xf97:	Stimulation Data Vector**
Memory	
Group 11	
SBS Data	
Write	
Register	
0xf98:	Stimulation Data Vector**
Memory	
Group 12	
DAC Data	
Write	
Register	

0.000	C' 1.' D. V. **
0xf99:	Stimulation Data Vector**
Memory	
Group 12	
SBS Data	
Write	
Register	
0xf9a:	Stimulation Data Vector**
Memory	
Group 13	
DAC Data	
Write	
Register	
0xf9b:	Stimulation Data Vector**
Memory	
Group 13	
SBS Data	
Write	
Register	
0xf9c:	Stimulation Data Vector**
Memory	Samulation Samulation
Group 14	
DAC Data	
Write	
Register	
	0' 1' D. V. **
0xf9d:	Stimulation Data Vector**
Memory Group 14	
SBS Data	
Write	
Register	
0xf9e:	Stimulation Data Vector**
Memory	
Group 15 DAC Data	
Write	
Register	
0xf9f:	Stimulation Data Vector**
Memory	
Group 15	
SBS Data	
Write	
Register	
0xfa0:	Stimulation Data Vector**
Memory	
Group 16	
DAC Data	
Write	
Register	
0xfa1:	Stimulation Data Vector**
Memory	
Group 16	
SBS Data	
Write	
Register	

0xfa2:	Stimulation Data Vector**
Memory	
Group 17	
DAC Data	
Write	
Register	
0xfa3:	Stimulation Data Vector**
Memory	
Group 17	
SBS Data	
Write	
Register	

*shift value decoding:

```
0: 1 Segment
1: 2 Segments
2: 4 Segments
3: 8 Segments
4: 16 Segments
5: 32 Segments
6: 64 Segments
7: 128 Segments
8: 256 Segments
```

**Data Vector decoding:

```
Bit 31: Reserved

Bit 30 - 28:

000: DAC/Sideband data vector

001: loop pointer vector

010: Long loop pointer vector

011: Long loop control vector

111: END command
```

DAC/Sideband data vector (000):

```
Bit 27: Reserved

Bit 26: Repeat Timebase (0: 20 us, 1: 1000*20us)

Bit 25 - 16: Number of Repeats (0: Pattern is used 1x Timebase; 1: Pattern is used for 2x Timebase; ...)

Bit 15 - 0: DAC data value (unsigned 16 bit value, 0x8000 is zero level) / SBS data value

SBS Bit 0: Amplifier Protection Switch/Blanking

SBS Bit 3: Stimulation Switch

SBS Bit 4: Stimulus Select

SBS Bit 8-15: Electrode Config ID
```

loop pointer vector (001):

```
Bit 27 - 26: Loop Level

Bit 25 - 16: Number of Repeats (2: Vectors are repeated once, thus used twice)

Bit 15 - 0 : Address Offset (Number of Vectors to jump backward, 1: One Vector before the LoopPtr is repeated)
```

Long loop pointer vector (010):

Bit 27 - 0: Address Offset (Number of Vectors to jump backward)

Long loop control vector (011):

Bit 27 - 0: Number of Repeats

END command (111): Bit 27 - 0 : Reserved

Quelle(n) und Bearbeiter des/der Artikel(s)

 $\textbf{MEA2100-256 User Guide} \ \ \textit{Quelle}: \\ \textbf{http://wiki.mcs.de.com/index.php?oldid=24639} \ \ \textit{Bearbeiter}. \ \ \textit{Jesinger}, \ 166 \ anonyme \ \ \textit{Bearbeitungen} \\ \textbf{MEA2100-256 User Guide} \ \ \textit{Quelle}: \\ \textbf{MEA2100-256 User Guide} \ \$