MEA2100-Mini User Guide

Interfaceboard Address Map (Address bits 11-0), Base Address: 0x0000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000: Device ID																									0x0b = ME2100 IFB							
0x004: HW/FPGA Version									HW/Board Version								FPGA Version															
0x008: Configuration																								Cy2_notCy1						COD Pins		

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x010: GTP Status																															SCU2 link up	SCU1 link up
0x014: Error counter (RO)	error counter SCU2																error counter SCU1															
0x014: Error counter reset (WO)	any write resets the error counters																															

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x020: Reset																																Reset FPGA
0x024: Power enable																														SCU 2 power	SCU 1 power	IF analog
0x028: Waveform										SCU 2 delay								SCU 1 delay								IF delay						
0x02c: LED																						LED SCU 1/2 and IF register mode enable								LED SCU 1/2 and IF		

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x030: (WO)Flash Instruction Code Register																								Fifo Reset	Instruction Code							
0x030: (RO)Flash Status Register																						FIFO_empty	FIFO_full	Statemachine busy	Flash Status Register							
0x034: Flash Memory Address Register									Flash Address																							
0x038: Flash Data FIFO Register	256 Data Bytes in 64 DWords to/from Flash																															
0x03c: Flash HW configuration Register	Address length (1, 2 or 3 Bytes)								Clock Divider Register (Multiples of 2 divide 38.4 MHz)																							

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0f0: Lock other Cypress																																Lock

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x100: Trigger CTRL	Trigger update rate																														Trigger idle	Enable trigger
0x104: Trigger Configuration																	Trigger rise/fall send seperate															
0x108: Trigger Status Config																	Select trigger status source ('0'(default): register reflects SCU trigger status, '1': register reflects internal register status)															
0x110: Set Trigger (Write)																	Generate trigger event, self clearing if trigger rise/fall == '0'															
0x110: Trigger Event Monitor (Read)																	Trigger event bits at next trigger packet to SCU															
0x114: Clear Trigger (Write)																	Clear Trigger status, only when trigger rise/fall == '1'															
0x114: Trigger Status Monitor (Read)																	Trigger status bits at next trigger packet to SCU															
0x120: Trigger Armed																	Armed (1 bit per trigger)															

0x124: Trigger Running			Running (1 bit per trigger)	
0x140: Electrode/Segment ID Trigger 0		Segment/Trigger ID		Electrode config ID
0x144: Electrode/Segment ID Trigger 1		Segment/Trigger ID		Electrode config ID
0x148: Electrode/Segment ID Trigger 2		Segment/Trigger ID		Electrode config ID
0x14c: Electrode/Segment ID Trigger 3		Segment/Trigger ID		Electrode config ID
0x150: Electrode/Segment ID Trigger 4		Segment/Trigger ID		Electrode config ID
0x154: Electrode/Segment ID Trigger 5		Segment/Trigger ID		Electrode config ID
0x158: Electrode/Segment ID Trigger 6		Segment/Trigger ID		Electrode config ID
0x15c: Electrode/Segment ID Trigger 7		Segment/Trigger ID		Electrode config ID
0x160: Electrode/Segment ID Trigger 8		Segment/Trigger ID		Electrode config ID
0x164: Electrode/Segment ID Trigger 9		Segment/Trigger ID		Electrode config ID
0x168: Electrode/Segment ID Trigger 10		Segment/Trigger ID		Electrode config ID
0x16c: Electrode/Segment ID Trigger 11		Segment/Trigger ID		Electrode config ID

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x200: Trigger CTRL	Trigger update rate																														Trigger idle	Enable trigger
0x204: Trigger Configuration																					Trigger rise/fall send seperate											
0x208: Trigger Status Config																					Select trigger status source ('0'(default): register reflects SCU trigger status, '1': register reflects internal register status)											
0x210: Set Trigger (Write)																					Generate trigger event, self clearing if trigger rise/fall == '0'											
0x210: Trigger Event Monitor (Read)																					Trigger event bits at next trigger packet to SCU											
0x214: Clear Trigger (Write)																					Clear Trigger status, only when trigger rise/fall == '1'											
0x214: Trigger Status Monitor (Read)																					Trigger status bits at next trigger packet to SCU											
0x220: Trigger Armed																					Armed (1 bit per trigger)											
0x224: Trigger Running																					Running (1 bit per trigger)											
0x240: Electrode/Segment ID Trigger 0									Segment/Trigger ID																				Electrode config ID			
0x244: Electrode/Segment ID Trigger 1									Segment/Trigger ID																				Electrode config ID			
0x248: Electrode/Segment ID Trigger 2									Segment/Trigger ID																				Electrode config ID			
0x24c: Electrode/Segment ID Trigger 3									Segment/Trigger ID																				Electrode config ID			
0x250: Electrode/Segment ID Trigger 4									Segment/Trigger ID																				Electrode config ID			
0x254: Electrode/Segment ID Trigger 5									Segment/Trigger ID																				Electrode config ID			
0x258: Electrode/Segment ID Trigger 6									Segment/Trigger ID																				Electrode config ID			
0x25c: Electrode/Segment ID Trigger 7									Segment/Trigger ID																				Electrode config ID			
0x260: Electrode/Segment ID Trigger 8									Segment/Trigger ID																				Electrode config ID			

0x264: Electrode/Segment ID Trigger 9		Segment/Trigger ID		Electrode config ID
0x268: Electrode/Segment ID Trigger 10		Segment/Trigger ID		Electrode config ID
0x26c: Electrode/Segment ID Trigger 11		Segment/Trigger ID		Electrode config ID

Register	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Register	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x400: Digital single pulse	bits can only be set here, and will be cleared after the time defined in Digital single pulse duration 1 .. 4																															
0x404: Digital single pulse duration 1	Duration of Digital Data in multiple of 20 us for Pulse Register bits 0 to 7																															
0x408: Digital single pulse duration 2	Duration of Digital Data in multiple of 20 us for Pulse Register bits 8 to 15																															
0x40c: Digital single pulse duration 3	Duration of Digital Data in multiple of 20 us for Pulse Register bits 16 to 23																															
0x410: Digital single pulse duration 4	Duration of Digital Data in multiple of 20 us for Pulse Register bits 24 to 31																															
0x420: Digital periodic pulse generator 1 period																							Sample period									
0x421: Digital periodic pulse generator 2 period																							Sample period									
0x422: Digital periodic pulse generator 3 period																							Sample period									
0x423: Digital periodic pulse generator 4 period																							Sample period									
0x424: Digital periodic pulse generator 1 length																							Pulse length									

0x425: Digital periodic pulse generator 2 length		Pulse length		
0x426: Digital periodic pulse generator 3 length		Pulse length		
0x427: Digital periodic pulse generator 4 length		Pulse length		
0x428: Digital periodic pulse generator 1 config		Mode*		Digital IN bit select
0x429: Digital periodic pulse generator 2 config		Mode*		Digital IN bit select
0x42a: Digital periodic pulse generator 3 config		Mode*		Digital IN bit select
0x42b: Digital periodic pulse generator 4 config		Mode*		Digital IN bit select
0x440: Digital stimulator clear write pointer				channel (0..15)
0x444: Digital stimulator channel memory select (WO)		memory location		channel
0x448: Digital Stimulator channel data (WO)	Append data to current selected channel (selected via Digital stimulator channel memory select register 3:0)			
0x448: Digital Stimulator channel data (RO)	Read data from selected channel (selected via Digital stimulator channel memory select register 3:0)			
0x44c: Digital Stimulator start slope	mask	slope (0: falling, 1: rising)		
0x450: Digital Stimulator stop slope	mask	slope (0: falling, 1: rising)		

0x454: Digital Stimulator global repeat		per channel 1 bit (0: single, 1: loop)
0x480: Feedback data	Feedback data	
0x4a0: Data to Data Stream		
0x4a4: Mask for 'Digital Data-Stream'		
0x4b0: AUX data OUT		AUX data
0x4b4: AUX data IN		AUX data
0x4b8: AUX data direction		0: Input, 1: Output
0x4d0: Digital OUT port (RO)	Data	
0x4d4: Digital IN port (RO)	Data	
0x4d8: Direction of digital port	1: Input, 0: Output	
0x4dc: Digital port interrupt enable	1: Interrupt enabled, affects only inputs, 0: Interrupt disabled	

*__Mode:__

```
bit     function
 0      0: disabled,              1: enabled
 1      0: start on "DACQ Start", 1: start on "DACQ Start" AND selected 'Digital IN bit'
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x500: Digital data delay																											Number of sweeps to delay the digital data					
0x504: Delay interface board data																							Digital data register	Digital out stimulator	Digital pulse generator	DACQ is running	AUX in	Feedback		Digital OUT	Digital IN	Digital MUX
0x510: Delay SCU 1 trigger																							Trigger status (1 bit per trigger)									

0x514: Delay SCU 1 stimulation data			Sideband data (1 bit per sideband memory channel)	
0x520: Delay SCU 2 trigger			Trigger status (1 bit per trigger)	
0x524: Delay SCU 2 stimulation data			Sideband data (1 bit per sideband memory channel)	
0x540: Digital mux source target config	source Code*	source bit select*	target Code**	target bit select**
0x544: Digital mux source read prepare (WO)	don't care		target**	target bit select**

*Source Code and bits:

```
source Code  Source            Number of bits     source bit select

IFB

0x00         Digital In               32            0 - 31

0x01         Digital Single Pulse Reg 32            0 - 31

0x02         Feedback                 32            0 - 31

0x03         Aux Data In               2            0 -  1

             Fix 0                     1            2

             Fix 1                     1            3

             DACQ is running           4            4 -  7 legacy, only 2 devices here, do not use for future SW implementations

             Digital Peri. Pulse Gen.  8            8 - 15

             Digital Out Stimul.      16           16 - 31

0x04         Digital Data Reg.        32            0 - 31

0x05         DACQ is running          8             0 -  7

SCU 1/2 (SCU 1: 0x40-0x7F, SCU 2: 0x80-0xBF)

0x40/0x80    Trigger Status 0 - 11    24            0 - 23

0x42/0x82    Sideband data  0         16            0 - 15

0x43/0x83    Sideband data  1         16            0 - 15

0x44/0x84    Sideband data  2         16            0 - 15

0x45/0x85    Sideband data  3         16            0 - 15

0x46/0x86    Sideband data  4         16            0 - 15

0x47/0x87    Sideband data  5         16            0 - 15

0x48/0x88    Sideband data  6         16            0 - 15
```

```
0x49/0x89    Sideband data  7        16          0 - 15
0x4A/0x8A    Sideband data  8        16          0 - 15
0x4B/0x8B    Sideband data  9        16          0 - 15
0x4C/0x8C    Sideband data 10        16          0 - 15
0x4D/0x8D    Sideband data 11        16          0 - 15
```

****Target Code and bits:***

```
target Code  Target              Number of bits    target bit select
 0x0         Trigger for STGs on SCU 1  32          0 - 31
 0x1         Trigger for STGs on SCU 2  32          0 - 31
 0x2         Dig Out                    32          0 - 31
 0x3         Digital MUX Stream S0      32          0 - 31
 0x4         Digital MUX Stream S1      32          0 - 31
 0x5         Trigger for DACQ Start     32          0 - 31
 0x6         Digital Out Stimulator     32          0 - 31
 0x7-0xFF    Reserved
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x600: Data stream enable																			digital	DSP	DAC	Analog	ADC								SCU2 link up	SCU1 link up
0x604: FIFO control 0 -> DACQ path reset																																

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x700: Right audio channel													Source (DSP, IF, HS2, HS1)*												Channel							
0x704: Left audio channel													Source (DSP, IF, HS2, HS1)*												Channel							
0x710: Right attenuation																															Attenuation	
0x714: Right attenuation																															Attenuation	

*****Source:*** Source decoding:

```
0: No source
1: HS0
2: HS1
3: IF
4: DSP(bits 23 - 0)
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x800: Downsampling device 0																									Percentage of full data rate							
0x801: Downsampling device 1																									Percentage of full data rate							
0x802: Downsampling device 2																									Percentage of full data rate							
0x803: Downsampling device 3																									Percentage of full data rate							
0x804: Start devices																													Device 3	Device 2	Device 1	Device 0
0x808: Stop devices																													Device 3	Device 2	Device 1	Device 0
0x80c: Reset devices																													Reset Dev. 3	Reset Dev. 2	Reset Dev. 1	Reset Dev. 0
0x81c: Channel select device 0	Data source device*																(Sub-Group)/Segment select within data device															
0x81d: Channel select device 1	Data source device*																(Sub-Group)/Segment select within data device															
0x81e: Channel select device 2	Data source device*																(Sub-Group)/Segment select within data device															
0x81f: Channel select device 3	Data source device*																(Sub-Group)/Segment select within data device															
0x820: Channel Select device 0	Channel 0 to 31 for selected source and group																															
0x821: Channel Select device 1	Channel 0 to 31 for selected source and group																															
0x822: Channel Select device 2	Channel 0 to 31 for selected source and group																															
0x823: Channel Select device 3	Channel 0 to 31 for selected source and group																															

0x824: Channel Select device 0	Channel 32 to 63 for selected source and group
0x825: Channel Select device 1	Channel 32 to 63 for selected source and group
0x826: Channel Select device 2	Channel 32 to 63 for selected source and group
0x827: Channel Select device 3	Channel 32 to 63 for selected source and group
0x828: Channel Select device 0	Channel 64 to 95 for selected source and group
0x829: Channel Select device 1	Channel 64 to 95 for selected source and group
0x82a: Channel Select device 2	Channel 64 to 95 for selected source and group
0x82b: Channel Select device 3	Channel 64 to 95 for selected source and group
0x82c: Channel Select device 0	Channel 96 to 127 for selected source and group
0x82d: Channel Select device 1	Channel 96 to 127 for selected source and group
0x82e: Channel Select device 2	Channel 96 to 127 for selected source and group
0x82f: Channel Select device 3	Channel 96 to 127 for selected source and group
0x830: Channel Select device 0	Channel 128 to 159 for selected source and group

0x831: Channel Select device 1	Channel 128 to 159 for selected source and group
0x832: Channel Select device 2	Channel 128 to 159 for selected source and group
0x833: Channel Select device 3	Channel 128 to 159 for selected source and group
0x834: Channel Select device 0	Channel 160 to 191 for selected source and group
0x835: Channel Select device 1	Channel 160 to 191 for selected source and group
0x836: Channel Select device 2	Channel 160 to 191 for selected source and group
0x837: Channel Select device 3	Channel 160 to 191 for selected source and group
0x838: Channel Select device 0	Channel 192 to 223 for selected source and group
0x839: Channel Select device 1	Channel 192 to 223 for selected source and group
0x83a: Channel Select device 2	Channel 192 to 223 for selected source and group
0x83b: Channel Select device 3	Channel 192 to 223 for selected source and group
0x83c: Channel Select device 0	Channel 224 to 255 for selected source and group
0x83d: Channel Select device 1	Channel 224 to 255 for selected source and group

0x83e: Channel Select device 2	Channel 224 to 255 for selected source and group		
0x83f: Channel Select device 3	Channel 224 to 255 for selected source and group		
0x870: Data format device 0		Voltage range in 16 bit mode**	Data mode***
0x871: Data format device 1		Voltage range in 16 bit mode**	Data mode***
0x872: Data format device 2		Voltage range in 16 bit mode**	Data mode***
0x873: Data format device 3		Voltage range in 16 bit mode**	Data mode***

* ***Data source:***

Source:	Code:	Segment from/to:	bits:	
SCU 1	0x1	0	0 to 255	-> 256 channels per Headstage
SCU 2	0x5	0	0 to 255	-> 256 channels per Headstage
IF	0x9	0	0 to 7	-> 8 ADC channels
Reserved for analog	0xA	0 to 1(0: HS1, 1: HS2)	0 to 11	-> 0 to 31
STG DAC Data	0xB	0 to 1(0: HS1, 1: HS2)	0 to 11	-> DAC 0 to 11
DSP	0xC (not yet implemented)	0 to 7	0 to 255	-> 256 32 bit Channels
Digital Data	0xD	0 to 4(1/2: HS1, 3/4: HS2)	0 to 11/63	-> 14 32bit Vector****
Reserved	0xE	0		

** ***Voltage Range:***

	bit 07	06	05	04	Description:
16 bit mode	0	0	0	0	Bits 31 (sign) & 14 downto 0
16 bit mode	0	0	0	1	Bits 31 (sign) & 15 downto 1
16 bit mode	0	0	1	0	Bits 31 (sign) & 16 downto 2
16 bit mode	0	0	1	1	Bits 31 (sign) & 17 downto 3
16 bit mode	0	1	0	0	Bits 31 (sign) & 18 downto 4
16 bit mode	0	1	0	1	Bits 31 (sign) & 19 downto 5
16 bit mode	0	1	1	0	Bits 31 (sign) & 20 downto 6
16 bit mode	0	1	1	1	Bits 31 (sign) & 21 downto 7
16 bit mode	1	0	0	0	Bits 31 (sign) & 22 downto 8

*** ***Data mode:***

```
           bit  03  02  01  00     Description:
16 bit mode      S/U  0   0   0
reserved         S/U  0   0   1
24 bit real mode S/U  0   1   0  all 24 bit in a chain (only analog data)
32 bit mode      S/U  0   1   1  all data 32 bit aligned
                 S/U : Signed or unsigned mode - 0 = unsigned, 1 = signed
for digital data only 16 or 32 bit unsigned mode available! this will be configured via cypress with the select bits
voltage range is only for 16 bit analog data available
```

****_Digital Data 32bit vector:_**

```
Segment 0: (IFB Dig Data)

Bits:  Data Source:
 0, 1   Digital MUX Stream S0 (to be used on USB Port A)
 2, 3   Digital MUX Stream S1 (to be used on USB Port B)
 4, 5   Digital In
 6, 7   Digital Out
 8, 9   Feedback Register
10, 11  Digital Register
12      Aux Input and Dig Periodig Pulse
13      Digital Generator/Stimulator

Segment 1: (SCU 1 Sideband Data)

Bits:  Data Source:
 0, 1   Sideband Vector  0
 2, 3   Sideband Vector  1
 4, 5   Sideband Vector  2
 6, 7   Sideband Vector  3
 8, 9   Sideband Vector  4
10, 11  Sideband Vector  5
12, 13  Sideband Vector  6
14, 15  Sideband Vector  7
16, 17  Sideband Vector  8
18, 19  Sideband Vector  9
20, 21  Sideband Vector 10
22, 23  Sideband Vector 11

Segment 2: (SCU 1 Trigger Status)

Bits:  Data Source:
 0  Trigger 0 status
 2  Trigger 1 status
 4  Trigger 2 status
 6  Trigger 3 status
 8  Trigger 4 status
10  Trigger 5 status
```

```
12  Trigger 6 status
14  Trigger 7 status
16  Trigger 8 status
18  Trigger 9 status
20  Trigger 10 status
22  Trigger 11 status

Segment 3: (SCU 2 Sideband Data)

Bits:  Data Source:
 0, 1   Sideband Vector  0
 2, 3   Sideband Vector  1
 4, 5   Sideband Vector  2
 6, 7   Sideband Vector  3
 8, 9   Sideband Vector  4
10, 11  Sideband Vector  5
12, 13  Sideband Vector  6
14, 15  Sideband Vector  7
16, 17  Sideband Vector  8
18, 19  Sideband Vector  9
20, 21  Sideband Vector 10
22, 23  Sideband Vector 11

Segment 4: (SCU 2 Trigger Status)

Bits:  Data Source:
 0  Trigger 0 status
 2  Trigger 1 status
 4  Trigger 2 status
 6  Trigger 3 status
 8  Trigger 4 status
10  Trigger 5 status
12  Trigger 6 status
14  Trigger 7 status
16  Trigger 8 status
18  Trigger 9 status
20  Trigger 10 status
22  Trigger 11 status
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xb00: DSP Indata CTRL Register																								Int En							Clear Fifo Flags(WO)	Reset Fifo(WO)
0xb04: DSP Outdata CTRL Register																								Int En							Clear Fifo Flags(WO)	Reset Fifo(WO)
0xb08: DSP In Fifo Status Flags(RO)																									overflow occured	overflow	full	progr. full	progr. empty	empty	underflow	underflow occured
0xb0c: DSP Out Fifo Status Flags(RO)																									overflow occured	overflow	full	progr. full	progr. empty	empty	underflow	underflow occured
0xb10: DSP Indata Threshold Register															Fifo full TH								Fifo empty TH									
0xb14: DSP Outdata Threshold Register															Fifo full TH								Fifo empty TH (insert amount of transmit data here)									
0xb18: DSP Indata Channel Info(RO)	Configured channels, detected after a full sweep, reread if 0																															
0xb20: DSP Boot conf. Register															Bootmode								Reset	POR								
0xb24: DSP Mailbox CTRL Register																								Int En								
0xb28: DSP Mailbox Info Register																							Last used Address at write to Mailbox Memory									
0xb30: DSP Streamdata CTRL Register															Keep last Streamdata	Enable Streaming								Int En							Clear Fifo Flags(WO)	Reset Fifo(WO)

0xb34: DSP Stream Fifo Status Flags(RO)					overflow occured	overflow	full	progr. full	progr. empty	empty	underflow	underflow occured
0xb38: I2C Bus CTRL Register											Connect DSP I2C Bus with USB B I2C BUS	Connect DSP I2C Bus with USB A I2C BUS
0xb40: Filter Data Select Register			send IFB Filtered data				send HS2 Filtered data				send HS1 Filtered data	
0xb81: Indata Enable: Headstage 1												256 channels
0xb85: Indata Enable: Headstage 2												256 channels
0xb89: Indata Enable: IFB Analog												8 channels
0xb8b: Indata Enable: STG DAC Data											12 HS 2 channels*	12 HS 1 channels*
0xb8d: Indata Enable: Digital Data								18 HS 2 Trig. Stat. channels*	18 HS 2 SBS channels*	18 HS 1 Trig. Stat. channels*	18 HS 1 SBS channels*	8 IFB channels*
0xb8f: Indata Enable: Tail Data												6 channels*

**Data source details:*

```
for more details see Data Stream Select Register Description food notes at address 0x800
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xc00: Filter 1 coefficent b[0]	Filter coefficent b[0] as Q1.30 value																															
0xc08: Filter 1 coefficent b[1]	Filter coefficent b[1] as Q1.30 value																															
0xc0c: Filter 1 coefficent a[1]	Filter coefficent a[1] as Q1.30 value																															
0xc10: Filter 1 coefficent b[2]	Filter coefficent b[2] as Q1.30 value																															
0xc14: Filter 1 coefficent a[2]	Filter coefficent a[2] as Q1.30 value																															
0xc18: Filter 1 coefficent a[2]	lower bits of a[2]																lower bits of a[1]															
0xc1c: Filter 1 control																															Enable filter for SCU 2	Enable filter for SCU 1
0xc20: Filter 2 coefficent b[0]	Filter coefficent b[0] as Q1.30 value																															
0xc28: Filter 2 coefficent b[1]	Filter coefficent b[1] as Q1.30 value																															
0xc2c: Filter 2 coefficent a[1]	Filter coefficent a[1] as Q1.30 value																															
0xc30: Filter 2 coefficent b[2]	Filter coefficent b[2] as Q1.30 value																															
0xc34: Filter 2 coefficent a[2]	Filter coefficent a[2] as Q1.30 value																															

0xc38: Filter 2 coefficent a[2]	lower bits of a[2]			lower bits of a[1]		
0xc3c: Filter 2 control					Enable filter for SCU 2	Enable filter for SCU 1
0xc40: Filter 3 coefficent b[0]	Filter coefficent b[0] as Q1.30 value					
0xc48: Filter 3 coefficent b[1]	Filter coefficent b[1] as Q1.30 value					
0xc4c: Filter 3 coefficent a[1]	Filter coefficent a[1] as Q1.30 value					
0xc50: Filter 3 coefficent b[2]	Filter coefficent b[2] as Q1.30 value					
0xc54: Filter 3 coefficent a[2]	Filter coefficent a[2] as Q1.30 value					
0xc58: Filter 3 coefficent a[2]	lower bits of a[2]			lower bits of a[1]		
0xc5c: Filter 3 control					Enable filter for SCU 2	Enable filter for SCU 1
0xc60: Filter 4 coefficent b[0]	Filter coefficent b[0] as Q1.30 value					
0xc68: Filter 4 coefficent b[1]	Filter coefficent b[1] as Q1.30 value					
0xc6c: Filter 4 coefficent a[1]	Filter coefficent a[1] as Q1.30 value					
0xc70: Filter 4 coefficent b[2]	Filter coefficent b[2] as Q1.30 value					

0xc74: Filter 4 coefficent a[2]	Filter coefficent a[2] as Q1.30 value						
0xc78: Filter 4 coefficent a[2]	lower bits of a[2]			lower bits of a[1]			
0xc7c: Filter 4 control						Enable filter for SCU 2	Enable filter for SCU 1
0xcc0: filter frequency	Corner frequency of hardware filter in mHz						
0xcc4: filter information	filter order	band: lowpass		family		0: hardware filter	enabled

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xe00: DMA control																															DMA active	DMA start
0xe04: DMA start address																	Start address															
0xe08: DMA counter																						Counter										

Mini DMA command overview:

```
Command      Bit 31 to 24   Bit 23 to 0         Description
  SDTA         0x01          register address    Store next data to register address
  DATA         Data          Data                Data expected after SDTA command
  STP          0xFF          (anything)          Stop DMA
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xf00: (WO)EEPROM Instruction Code Register																								Fifo Reset	Instruction Code							
0xf00: (RO)EEPROM Status Register																						FIFO_empty	FIFO_full	Statemachine busy	Flash Status Register							

0xf04: EEPROM Memory Address Register		Flash Address
0xf08: EEPROM Data FIFO Register	256 Data Bytes in 64 DWords to/from Flash	
0xf0c: EEPROM HW configuration Register	Address length (1, 2 or 3 Bytes)	Clock Divider Register (Multiples of 2 divide 38.4 MHz)
0xf10: EEPROM Offset Register	Offset for reads and writes to the EEprom	
0xf14: EEPROM Size Register	Size of the EEprom Block available for this Image	

Register	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0xf80: FPGA GENERAL 2																	GENERAL 2 data															
0xf84: FPGA GENERAL 5																	GENERAL 5 data															
0xf90: direct connection to FPGA SPI Flash																															Cypress number (0 = none)	
0xf94: Config EEprom Base																	base address of config eeprom															
0xf98: FX3-USB Bootstrap Firmware																	Firmware Version of FX3 Bootstrap code this USB Port															
0xf9c: FX3-USB Bootstrap Firmware other port																	Firmware Version of FX3 Bootstrap code on other USB Port															
0xfb0: Message to other Cypress	A write will cause an interrupt on the other Cypress, with a read you can check is it is read already																															
0xfb4: Read Only: Message from other Cypress	Each bit which is set will be reset on read																															

SCU Address Map (Address bits 11-0), Base Address SCU 1: 0x8000, SCU 2: 0xC000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000: Device ID																									0x0c = ME2100 SCU							
0x001: Serial number low	lower 32 bit of SCU serial number, read as 4 ASCII bytes																															
0x002: Serial number high	higher 32 bit of SCU serial number, read as 4 ASCII bytes																															
0x004: FPGA Version																	FPGA firmware version															
0x008: PCB Revision																									Assembly Version				PCB Revision			

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x010: Port Status																																Link Up
0x014: Error Count																	CRC Error Count, reset on write															

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x020: Reset																																Reset

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x030: (WO)Flash Instruction Code Register																								Fifo Reset	Instruction Code							
0x030: (RO)Flash Status Register																						FIFO_empty	FIFO_full	Statemachine busy	Flash Status Register							
0x034: Flash Memory Address Register									Flash Address																							
0x038: Flash Data FIFO Register	256 Data Bytes in 64 DWords to/from Flash																															

0x03c: Flash HW configuration Register	Address length (1, 2 or 3 Bytes)	Clock Divider Register (Multiples of 2 divide 38.4 MHz)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x040: (WO)EEPROM Instruction Code Register																								Fifo Reset	Instruction Code							
0x040: (RO)EEPROM Status Register																						FIFO_empty	FIFO_full	Statemachine busy	Flash Status Register							
0x044: EEPROM Memory Address Register									Flash Address																							
0x048: EEPROM Data FIFO Register	256 Data Bytes in 64 DWords to/from Flash																															
0x04c: EEPROM HW configuration Register	Address length (1, 2 or 3 Bytes)		Clock Divider Register (Multiples of 2 divide 38.4 MHz)																													

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x050: DMA control																															DMA active	DMA start
0x054: DMA start address																	Start address															
0x058: DMA counter																						Counter										

Mini DMA command overview:

```
Command      Bit 31 to 24   Bit 23 to 0         Description
  SDTA         0x01          register address    Store next data to register address
  DATA         Data          Data                Data expected after SDTA command
  STP          0xFF          (anything)          Stop DMA
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x100: Number of detection electrodes	128 Electrodes																															
0x110: ADC Range	ADC range (0x00231860 = 2300 mV)																															
0x114: ADC Resolution	ADC Resolution (0x80000112 = 274 nV/bit)																															
0x118: DAC Resolution	ADC Resolution in bits (0x00000018 = 24 bit)																															
0x11c: Gain	Gain of the DACQ System (0x80002710 = gain 10.0)																															
0x120: Limitations	Limitaions of this System can be written here																															
0x130: Max Sampling Freqency	Maximum Frequenzy that is allowed to be set at configuration for the user (0x0000C350 = 50 kHz)																															

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x400: Enable blanking	Electrode 32 to 1																															
0x401: Enable blanking	Electrode 64 to 33																															
0x402: Enable blanking	Electrode 96 to 65																															
0x403: Enable blanking	Electrode 128 to 97																															
0x480: Blanking control for stimulus channels	Force data keep																													Enable data keep on stimulation channels, post filter	Enable data keep on stimulation channels, mid filter	Enable data keep on stimulation channels, pre filter
0x484: Stimulus data keep pre filter								onset delay														offset delay										
0x488: Stimulus data keep mid filter								onset delay														offset delay										
0x48c: Stimulus data keep post filter								onset delay														offset delay										
0x4a0: Blanking control for non-stimulus channels	Force data keep																													Enable data keep on measurement channels, post filter	Enable data keep on measurement channels, mid filter	Enable data keep on measurement channels, pre filter

0x4a4: Non-stimulus data keep pre filter		onset delay		offset delay
0x4a8: Non-stimulus data keep mid filter		onset delay		offset delay
0x4ac: Non-stimulus data keep post filter		onset delay		offset delay
0x4c0: Highpass Filterreset				Reset filter
0x4c4: Highpass reset duration				Duration in 20us units

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x600: Filter 1 coefficent b[0]	Filter coefficent b[0] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x608: Filter 1 coefficent b[1]	Filter coefficent b[1] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x60c: Filter 1 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)																															
0x610: Filter 1 coefficent b[2]	Filter coefficent b[2] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x614: Filter 1 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)																															
0x618: Filter 1 coefficent lower bits	lower bits of a[2]																lower bits of a[1]															
0x61c: Filter 1 control																															Enable Blanking	Enable Filter

0x620: Filter 2 coefficent b[0]	Filter coefficent b[0] as Q1.16 value														0 to extend coefficient to Q1.30	
0x628: Filter 2 coefficent b[1]	Filter coefficent b[1] as Q1.16 value														0 to extend coefficient to Q1.30	
0x62c: Filter 2 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)															
0x630: Filter 2 coefficent b[2]	Filter coefficent b[2] as Q1.16 value														0 to extend coefficient to Q1.30	
0x634: Filter 2 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)															
0x638: Filter 2 coefficent lower bits	lower bits of a[2]												lower bits of a[1]			
0x63c: Filter 2 control															Enable Blanking	Enable Filter
0x640: Filter 3 coefficent b[0]	Filter coefficent b[0] as Q1.16 value														0 to extend coefficient to Q1.30	
0x648: Filter 3 coefficent b[1]	Filter coefficent b[1] as Q1.16 value														0 to extend coefficient to Q1.30	
0x64c: Filter 3 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)															
0x650: Filter 3 coefficent b[2]	Filter coefficent b[2] as Q1.16 value														0 to extend coefficient to Q1.30	
0x654: Filter 3 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)															
0x658: Filter 3 coefficent lower bits	lower bits of a[2]												lower bits of a[1]			

0x65c: Filter 3 control			Enable Blanking	Enable Filter
0x660: Filter 4 coefficent b[0]	Filter coefficent b[0] as Q1.16 value	0 to extend coefficient to Q1.30		
0x668: Filter 4 coefficent b[1]	Filter coefficent b[1] as Q1.16 value	0 to extend coefficient to Q1.30		
0x66c: Filter 4 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)			
0x670: Filter 4 coefficent b[2]	Filter coefficent b[2] as Q1.16 value	0 to extend coefficient to Q1.30		
0x674: Filter 4 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)			
0x678: Filter 4 coefficent lower bits	lower bits of a[2]		lower bits of a[1]	
0x67c: Filter 4 control			Enable Blanking	Enable Filter
0x6a0: Filter 2b coefficent b[0]	Filter coefficent b[0] as Q1.16 value	0 to extend coefficient to Q1.30		
0x6a8: Filter 2b coefficent b[1]	Filter coefficent b[1] as Q1.16 value	0 to extend coefficient to Q1.30		
0x6ac: Filter 2b coefficent a[1]	Filter coefficent a[1] as Q1.30 value for one clock after blank (Q1.33 together with lower bits register)			
0x6a0: Filter 2b coefficent b[2]	Filter coefficent b[2] as Q1.16 value	0 to extend coefficient to Q1.30		
0x6a4: Filter 2b coefficent a[2]	Filter coefficent a[2] as Q1.30 value for one clock after blank (Q1.33 together with lower bits register)			

0x6a8: Filter 2b coefficent lower bits	lower bits of a[2]		lower bits of a[1]			
0x6c0: hardware filter frequency	Corner frequency of hardware filter in mHz					
0x6c4: hardware filter information	filter order	band: lowpass	family		0: hardware filter	enabled
0x6d0: highpass filter frequency	Corner frequency of highpass filter in mHz					
0x6d4: highpass filter information	filter order	band: highpass	family		1: software filter	enabled
0x6e0: lowpass filter frequency	Corner frequency of lowpass filter in mHz					
0x6e4: lowpass filter information	filter order	band: lowpass	family		1: software filter	enabled

Register	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0xe00: Link State																																Link up
0xe04: Cable delay																					Cable length in units of 9.766 ns											
0xe0c: Test																																
0xe10: Headstage magic	magic number from headstage																															
0xe14: Headstage framecount	Framecounter from headstage																															
0xe18: Local framecount	Local framecounter																															
0xe1c: Local framecount	Local framecounter																															

0xe20: Test DAC control										Impedance test					Enable testmode
0xe21: DAC1 amplitude								DAC amplitude							
0xe22: DAC2 amplitude								DAC amplitude							
0xe23: Impedance amplitude								DAC amplitude							
0xe24: DAC1 period								DAC period							
0xe25: DAC2 period								DAC period							
0xe26: Impedance period								DAC period							
0xe27: Select MUX 1	2 bits per MUX for DAC 16 .. 1														
0xe28: Select MUX 2	2 bits per MUX for DAC 32 .. 17														
0xe29: DAC Control										grounding		ref_a1	ref_a0	ref_en	cur/volt
0xe2a: External stimulation							en_stim_a1	en_stim_a0					ext_stim_a1	ext_stim_a0	ext_stim_en
0xe30: Headstage clock enable															enable

SCU Stimulation Address Map (Address bits 11-0) Base Address: SCU 1: 0x9000 SCU 2: 0xD000

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x100: Voltage Range	Voltage range (0x0000 2710 = 10000 mV)																															
0x104: Voltage Resolution	Voltage resolution (0x8000 01F4 = 500 uV)																															
0x108: Current Range	Current range (0x0000 03E8 = 1000 uA)																															
0x10c: Current Resolution	Current resolution (0x0000 0032 = 50 nA)																															
0x120: Trigger																	Number of trigger (12)															
0x130: Stimulation Memory																	Number of memory channels (24)															
0x140: DAC Properties	Number of DAC Channels (12)																Number of DAC memory channels (12)															
0x144: DAC Resolution																	Resolution in bits (16)															
0x150: Sideband Properties	Number of sidebands (12)																Number of sideband memory channels (12)															
0x160: Number of Stimulation Electrodes																	Stimulation Electrodes (128)															
0x170: Memory Configuration	Memory size per channel in 32 bit entries (0x0020 0000 = 2 M entries)																															
0x174: Total Memory Size	Memory size in 32 bit entries (0x0400 0000 = 64 M entires)																															

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x200: Memory Control Register for DAC in Memory Group 0																									Segment Selector*							
0x201: Start Pointer for DAC in Memory Group 0	Start Memory Pointer																															
0x202: End Pointer for DAC in Memory Group 0	End Memory Pointer																															
0x203: Write Pointer for DAC in Memory Group 0	Write Memory Pointer, write will clear Channel																															
0x208: Memory Control Register for SBS in Memory Group 0																									Segment Selector*							
0x209: Start Pointer for SBS in Memory Group 0	Start Memory Pointer																															

0x20a: End Pointer for SBS in Memory Group 0	End Memory Pointer	
0x20b: Write Pointer for SBS in Memory Group 0	Write Memory Pointer, write will clear Channel	
0x210: Memory Control Register for DAC in Memory Group 1		Segment Selector*
0x211: Start Pointer for DAC in Memory Group 1	Start Memory Pointer	
0x212: End Pointer for DAC in Memory Group 1	End Memory Pointer	
0x213: Write Pointer for DAC in Memory Group 1	Write Memory Pointer, write will clear Channel	
0x218: Memory Control Register for SBS in Memory Group 1		Segment Selector*
0x219: Start Pointer for SBS in Memory Group 1	Start Memory Pointer	
0x21a: End Pointer for SBS in Memory Group 1	End Memory Pointer	
0x21b: Write Pointer for SBS in Memory Group 1	Write Memory Pointer, write will clear Channel	
0x220: Memory Control Register for DAC in Memory Group 2		Segment Selector*
0x221: Start Pointer for DAC in Memory Group 2	Start Memory Pointer	
0x222: End Pointer for DAC in Memory Group 2	End Memory Pointer	
0x223: Write Pointer for DAC in Memory Group 2	Write Memory Pointer, write will clear Channel	
0x228: Memory Control Register for SBS in Memory Group 2		Segment Selector*

0x229: Start Pointer for SBS in Memory Group 2	Start Memory Pointer	
0x22a: End Pointer for SBS in Memory Group 2	End Memory Pointer	
0x22b: Write Pointer for SBS in Memory Group 2	Write Memory Pointer, write will clear Channel	
0x230: Memory Control Register for DAC in Memory Group 3		Segment Selector*
0x231: Start Pointer for DAC in Memory Group 3	Start Memory Pointer	
0x232: End Pointer for DAC in Memory Group 3	End Memory Pointer	
0x233: Write Pointer for DAC in Memory Group 3	Write Memory Pointer, write will clear Channel	
0x238: Memory Control Register for SBS in Memory Group 3		Segment Selector*
0x239: Start Pointer for SBS in Memory Group 3	Start Memory Pointer	
0x23a: End Pointer for SBS in Memory Group 3	End Memory Pointer	
0x23b: Write Pointer for SBS in Memory Group 3	Write Memory Pointer, write will clear Channel	
0x240: Memory Control Register for DAC in Memory Group 4		Segment Selector*
0x241: Start Pointer for DAC in Memory Group 4	Start Memory Pointer	
0x242: End Pointer for DAC in Memory Group 4	End Memory Pointer	
0x243: Write Pointer for DAC in Memory Group 4	Write Memory Pointer, write will clear Channel	

0x248: Memory Control Register for SBS in Memory Group 4		Segment Selector*
0x249: Start Pointer for SBS in Memory Group 4	Start Memory Pointer	
0x24a: End Pointer for SBS in Memory Group 4	End Memory Pointer	
0x24b: Write Pointer for SBS in Memory Group 4	Write Memory Pointer, write will clear Channel	
0x250: Memory Control Register for DAC in Memory Group 5		Segment Selector*
0x251: Start Pointer for DAC in Memory Group 5	Start Memory Pointer	
0x252: End Pointer for DAC in Memory Group 5	End Memory Pointer	
0x253: Write Pointer for DAC in Memory Group 5	Write Memory Pointer, write will clear Channel	
0x258: Memory Control Register for SBS in Memory Group 5		Segment Selector*
0x259: Start Pointer for SBS in Memory Group 5	Start Memory Pointer	
0x25a: End Pointer for SBS in Memory Group 5	End Memory Pointer	
0x25b: Write Pointer for SBS in Memory Group 5	Write Memory Pointer, write will clear Channel	
0x260: Memory Control Register for DAC in Memory Group 6		Segment Selector*
0x261: Start Pointer for DAC in Memory Group 6	Start Memory Pointer	
0x262: End Pointer for DAC in Memory Group 6	End Memory Pointer	

0x263: Write Pointer for DAC in Memory Group 6	Write Memory Pointer, write will clear Channel	
0x268: Memory Control Register for SBS in Memory Group 6		Segment Selector*
0x269: Start Pointer for SBS in Memory Group 6	Start Memory Pointer	
0x26a: End Pointer for SBS in Memory Group 6	End Memory Pointer	
0x26b: Write Pointer for SBS in Memory Group 6	Write Memory Pointer, write will clear Channel	
0x270: Memory Control Register for DAC in Memory Group 7		Segment Selector*
0x271: Start Pointer for DAC in Memory Group 7	Start Memory Pointer	
0x272: End Pointer for DAC in Memory Group 7	End Memory Pointer	
0x273: Write Pointer for DAC in Memory Group 7	Write Memory Pointer, write will clear Channel	
0x278: Memory Control Register for SBS in Memory Group 7		Segment Selector*
0x279: Start Pointer for SBS in Memory Group 7	Start Memory Pointer	
0x27a: End Pointer for SBS in Memory Group 7	End Memory Pointer	
0x27b: Write Pointer for SBS in Memory Group 7	Write Memory Pointer, write will clear Channel	
0x280: Memory Control Register for DAC in Memory Group 8		Segment Selector*
0x281: Start Pointer for DAC in Memory Group 8	Start Memory Pointer	

0x282: End Pointer for DAC in Memory Group 8	End Memory Pointer	
0x283: Write Pointer for DAC in Memory Group 8	Write Memory Pointer, write will clear Channel	
0x288: Memory Control Register for SBS in Memory Group 8		Segment Selector*
0x289: Start Pointer for SBS in Memory Group 8	Start Memory Pointer	
0x28a: End Pointer for SBS in Memory Group 8	End Memory Pointer	
0x28b: Write Pointer for SBS in Memory Group 8	Write Memory Pointer, write will clear Channel	
0x290: Memory Control Register for DAC in Memory Group 9		Segment Selector*
0x291: Start Pointer for DAC in Memory Group 9	Start Memory Pointer	
0x292: End Pointer for DAC in Memory Group 9	End Memory Pointer	
0x293: Write Pointer for DAC in Memory Group 9	Write Memory Pointer, write will clear Channel	
0x298: Memory Control Register for SBS in Memory Group 9		Segment Selector*
0x299: Start Pointer for SBS in Memory Group 9	Start Memory Pointer	
0x29a: End Pointer for SBS in Memory Group 9	End Memory Pointer	
0x29b: Write Pointer for SBS in Memory Group 9	Write Memory Pointer, write will clear Channel	
0x2a0: Memory Control Register for DAC in Memory Group 10		Segment Selector*

0x2a1: Start Pointer for DAC in Memory Group 10	Start Memory Pointer	
0x2a2: End Pointer for DAC in Memory Group 10	End Memory Pointer	
0x2a3: Write Pointer for DAC in Memory Group 10	Write Memory Pointer, write will clear Channel	
0x2a8: Memory Control Register for SBS in Memory Group 10		Segment Selector*
0x2a9: Start Pointer for SBS in Memory Group 10	Start Memory Pointer	
0x2aa: End Pointer for SBS in Memory Group 10	End Memory Pointer	
0x2ab: Write Pointer for SBS in Memory Group 10	Write Memory Pointer, write will clear Channel	
0x2b0: Memory Control Register for DAC in Memory Group 11		Segment Selector*
0x2b1: Start Pointer for DAC in Memory Group 11	Start Memory Pointer	
0x2b2: End Pointer for DAC in Memory Group 11	End Memory Pointer	
0x2b3: Write Pointer for DAC in Memory Group 11	Write Memory Pointer, write will clear Channel	
0x2b8: Memory Control Register for SBS in Memory Group 11		Segment Selector*
0x2b9: Start Pointer for SBS in Memory Group 11	Start Memory Pointer	
0x2ba: End Pointer for SBS in Memory Group 11	End Memory Pointer	
0x2bb: Write Pointer for SBS in Memory Group 11	Write Memory Pointer, write will clear Channel	

Segment Selector:

```
Segment 0 to 255 reflect the Segment ID 0 to 255 from Trigger CTRL logic.
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x500: Test Status															MEM test read/write in process	MEM test failed						MEM statemachine busy										
0x504: Test Control														Stop test	Start test	write / not read									Patternmode*							
0x508: Pattern	32 bit pattern for the test																															
0x50c: Fail counter -> 31-0 -> number of failed memory patterns (cleared on write)																																
0x510: Address pointer		the current address Pointer (for progress monitor, max Value: 0x0FFFFF80)																														
0x514: First fail address		the address Pointer of the first failed address of memory test																														
0x520: Memory status																							calibration done	selfrefresh active								enter selfrefresh
0x524: Memory size	0x20000000 == 512 MByte																															

Pattermode options:

```
0: Counter
1: Pattern
2: Shift Pattern right
3: Shift Pattern left
4: Toggle Pattern after every write
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x600: Trigger 0 Control Register																									Trigger configuration*							
0x601: Trigger 1 Control Register																									Trigger configuration*							
0x602: Trigger 2 Control Register																									Trigger configuration*							
0x603: Trigger 3 Control Register																									Trigger configuration*							
0x604: Trigger 4 Control Register																									Trigger configuration*							
0x605: Trigger 5 Control Register																									Trigger configuration*							
0x606: Trigger 6 Control Register																									Trigger configuration*							
0x607: Trigger 7 Control Register																									Trigger configuration*							
0x608: Trigger 8 Control Register																									Trigger configuration*							
0x609: Trigger 9 Control Register																									Trigger configuration*							
0x60a: Trigger 10 Control Register																									Trigger configuration*							
0x60b: Trigger 11 Control Register																									Trigger configuration*							
0x640: Stop Trigger																					Trigger 11 to 0, 1 bit per trigger											
0x644: Trigger Speed Monitor																	Trigger speed**															
0x680: Trigger 0 event limit	Stop trigger after this number of events																															
0x681: Trigger 1 event limit	Stop trigger after this number of events																															
0x682: Trigger 2 event limit	Stop trigger after this number of events																															
0x683: Trigger 3 event limit	Stop trigger after this number of events																															
0x684: Trigger 4 event limit	Stop trigger after this number of events																															
0x685: Trigger 5 event limit	Stop trigger after this number of events																															
0x686: Trigger 6 event limit	Stop trigger after this number of events																															
0x687: Trigger 7 event limit	Stop trigger after this number of events																															
0x688: Trigger 8 event limit	Stop trigger after this number of events																															

0x689: Trigger 9 event limit	Stop trigger after this number of events
0x68a: Trigger 10 event limit	Stop trigger after this number of events
0x68b: Trigger 11 event limit	Stop trigger after this number of events
0x6c0: Trigger 0 event counter	current trigger events
0x6c1: Trigger 1 event counter	current trigger events
0x6c2: Trigger 2 event counter	current trigger events
0x6c3: Trigger 3 event counter	current trigger events
0x6c4: Trigger 4 event counter	current trigger events
0x6c5: Trigger 5 event counter	current trigger events
0x6c6: Trigger 6 event counter	current trigger events
0x6c7: Trigger 7 event counter	current trigger events
0x6c8: Trigger 8 event counter	current trigger events
0x6c9: Trigger 9 event counter	current trigger events
0x6ca: Trigger 10 event counter	current trigger events
0x6cb: Trigger 11 event counter	current trigger events
0x700: Trigger 0 repeat limit	number of times to reapeat a trigger
0x701: Trigger 1 repeat limit	number of times to reapeat a trigger
0x702: Trigger 2 repeat limit	number of times to reapeat a trigger
0x703: Trigger 3 repeat limit	number of times to reapeat a trigger
0x704: Trigger 4 repeat limit	number of times to reapeat a trigger
0x705: Trigger 5 repeat limit	number of times to reapeat a trigger
0x706: Trigger 6 repeat limit	number of times to reapeat a trigger
0x707: Trigger 7 repeat limit	number of times to reapeat a trigger

0x708: Trigger 8 repeat limit	number of times to reapeat a trigger
0x709: Trigger 9 repeat limit	number of times to reapeat a trigger
0x70a: Trigger 10 repeat limit	number of times to reapeat a trigger
0x70b: Trigger 11 repeat limit	number of times to reapeat a trigger
0x740: Trigger 0 repeat counter	current trigger repeats
0x741: Trigger 1 repeat counter	current trigger repeats
0x742: Trigger 2 repeat counter	current trigger repeats
0x743: Trigger 3 repeat counter	current trigger repeats
0x744: Trigger 4 repeat counter	current trigger repeats
0x745: Trigger 5 repeat counter	current trigger repeats
0x746: Trigger 6 repeat counter	current trigger repeats
0x747: Trigger 7 repeat counter	current trigger repeats
0x748: Trigger 8 repeat counter	current trigger repeats
0x749: Trigger 9 repeat counter	current trigger repeats
0x74a: Trigger 10 repeat counter	current trigger repeats
0x74b: Trigger 11 repeat counter	current trigger repeats
0x780: Trigger 0 segment ID	current segment ID
0x781: Trigger 1 segment ID	current segment ID
0x782: Trigger 2 segment ID	current segment ID
0x783: Trigger 3 segment ID	current segment ID
0x784: Trigger 4 segment ID	current segment ID
0x785: Trigger 5 segment ID	current segment ID
0x786: Trigger 6 segment ID	current segment ID

0x787: Trigger 7 segment ID	current segment ID
0x788: Trigger 8 segment ID	current segment ID
0x789: Trigger 9 segment ID	current segment ID
0x78a: Trigger 10 segment ID	current segment ID
0x78b: Trigger 11 segment ID	current segment ID

*__Trigger configuration:__

```
Bit 0: Enable Trigger: not Armed -> Armed
Bit 3:1:
      0: Stop stimulus sequence at recuring of same trigger event
      1: Restart stimulus sequence at recuring of same trigger event
      2: Ignore same trigger and continue processing
      3: Gate stimulus sequence at trigger event
Bit 5:4:
      0: Stop stimulus sequence at occuring of other trigger event
      1: Restart stimulus sequence at occuring of other trigger event
      2: Ignore other trigger and continue processing
bit 7-6: Status of Trigger statemachine (00: not Armed, 01: Armed, 10: Triggerd (running), 11: Reserved)
```

**__Trigger speed:__

```
Value    STG speed
0x00     12.5 kHz
0x01     25 kHz
0x02     50 kHz (default)
0x03     100 kHz
0x04     200 kHz
0x05     400 kHz
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x800: Memory Group 0 DAC Data Read Configuration																used for DAC Data(RO)							Data Source*		Trigger number used to start this channel							
0x801: Memory Group 0 SBS Data Read Configuration																used for DAC Data(RO)							Data Source*		Trigger number used to start this channel							

0x802: Memory Group 1 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x803: Memory Group 1 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x804: Memory Group 2 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x805: Memory Group 2 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x806: Memory Group 3 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x807: Memory Group 3 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x808: Memory Group 4 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x809: Memory Group 4 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x80a: Memory Group 5 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel

0x80b: Memory Group 5 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x80c: Memory Group 6 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x80d: Memory Group 6 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x80e: Memory Group 7 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x80f: Memory Group 7 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x810: Memory Group 8 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x811: Memory Group 8 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x812: Memory Group 9 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x813: Memory Group 9 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel

0x814: Memory Group 10 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x815: Memory Group 10 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x816: Memory Group 11 DAC Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x817: Memory Group 11 SBS Data Read Configuration		used for DAC Data(RO)		Data Source*	Trigger number used to start this channel
0x880: Memory Group 0 static value for DAC			value used in manual mode		
0x881: Memory Group 0 static value for SBS			value used in manual mode		
0x882: Memory Group 1 static value for DAC			value used in manual mode		
0x883: Memory Group 1 static value for SBS			value used in manual mode		
0x884: Memory Group 2 static value for DAC			value used in manual mode		
0x885: Memory Group 2 static value for SBS			value used in manual mode		

0x886: Memory Group 3 static value for DAC		value used in manual mode
0x887: Memory Group 3 static value for SBS		value used in manual mode
0x888: Memory Group 4 static value for DAC		value used in manual mode
0x889: Memory Group 4 static value for SBS		value used in manual mode
0x88a: Memory Group 5 static value for DAC		value used in manual mode
0x88b: Memory Group 5 static value for SBS		value used in manual mode
0x88c: Memory Group 6 static value for DAC		value used in manual mode
0x88d: Memory Group 6 static value for SBS		value used in manual mode
0x88e: Memory Group 7 static value for DAC		value used in manual mode
0x88f: Memory Group 7 static value for SBS		value used in manual mode

0x890: Memory Group 8 static value for DAC		value used in manual mode
0x891: Memory Group 8 static value for SBS		value used in manual mode
0x892: Memory Group 9 static value for DAC		value used in manual mode
0x893: Memory Group 9 static value for SBS		value used in manual mode
0x894: Memory Group 10 static value for DAC		value used in manual mode
0x895: Memory Group 10 static value for SBS		value used in manual mode
0x896: Memory Group 11 static value for DAC		value used in manual mode
0x897: Memory Group 11 static value for SBS		value used in manual mode
0x900: Read pointer of Memory Group 0 for DAC	current read pointer position of read FSM	
0x901: Read pointer of Memory Group 0 for SBS	current read pointer position of read FSM	

0x902: Read pointer of Memory Group 1 for DAC	current read pointer position of read FSM
0x903: Read pointer of Memory Group 1 for SBS	current read pointer position of read FSM
0x904: Read pointer of Memory Group 2 for DAC	current read pointer position of read FSM
0x905: Read pointer of Memory Group 2 for SBS	current read pointer position of read FSM
0x906: Read pointer of Memory Group 3 for DAC	current read pointer position of read FSM
0x907: Read pointer of Memory Group 3 for SBS	current read pointer position of read FSM
0x908: Read pointer of Memory Group 4 for DAC	current read pointer position of read FSM
0x909: Read pointer of Memory Group 4 for SBS	current read pointer position of read FSM
0x90a: Read pointer of Memory Group 5 for DAC	current read pointer position of read FSM
0x90b: Read pointer of Memory Group 5 for SBS	current read pointer position of read FSM

0x90c: Read pointer of Memory Group 6 for DAC	current read pointer position of read FSM
0x90d: Read pointer of Memory Group 6 for SBS	current read pointer position of read FSM
0x90e: Read pointer of Memory Group 7 for DAC	current read pointer position of read FSM
0x90f: Read pointer of Memory Group 7 for SBS	current read pointer position of read FSM
0x910: Read pointer of Memory Group 8 for DAC	current read pointer position of read FSM
0x911: Read pointer of Memory Group 8 for SBS	current read pointer position of read FSM
0x912: Read pointer of Memory Group 9 for DAC	current read pointer position of read FSM
0x913: Read pointer of Memory Group 9 for SBS	current read pointer position of read FSM
0x914: Read pointer of Memory Group 10 for DAC	current read pointer position of read FSM
0x915: Read pointer of Memory Group 10 for SBS	current read pointer position of read FSM

0x916: Read pointer of Memory Group 11 for DAC	current read pointer position of read FSM
0x917: Read pointer of Memory Group 11 for SBS	current read pointer position of read FSM

__Data source:__

```
00: Stim. MEM Block X as Source (default)
01: Static value (manual mode, mainly for testing)
10: DSP direct stream as Source
11: Reserved, not Valid
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xa10: Current Voltage Switch																														1 = voltage mode; 0 = current mode (per HS one bit)		
0xa14: Impedance Ground Control						DoImpTest HS3	ImpStg_DoStimulus HS3	ImpStg_Grounding HS3						DoImpTest HS2	ImpStg_DoStimulus HS2	ImpStg_Grounding HS2						DoImpTest HS1	ImpStg_DoStimulus HS1	ImpStg_Grounding HS1					DoImpTest HS0	ImpStg_DoStimulus HS0	ImpStg_Grounding HS0
0xa1c: Impedance STG Config	ImpStg_Frequency																ImpStg_Amplitude															
0xa80: Electrode Group* 1 Source Select																														Select Stimulation Memory Group for Electrode Group		
0xa81: Electrode Group* 2 Source Select																														Select Stimulation Memory Group for Electrode Group		
0xa82: Electrode Group* 3 Source Select																														Select Stimulation Memory Group for Electrode Group		
0xa83: Electrode Group* 4 Source Select																														Select Stimulation Memory Group for Electrode Group		

0xa84: Electrode Group* 5 Source Select			Select Stimulation Memory Group for Electrode Group
0xa85: Electrode Group* 6 Source Select			Select Stimulation Memory Group for Electrode Group
0xb00: Dac A in Electr. Gr. 1 Data Register		Enable	DAC Data
0xb01: Dac B in Electr. Gr. 1 Data Register		Enable	DAC Data
0xb02: Dac A in Electr. Gr. 2 Data Register		Enable	DAC Data
0xb03: Dac B in Electr. Gr. 2 Data Register		Enable	DAC Data
0xb04: Dac A in Electr. Gr. 3 Data Register		Enable	DAC Data
0xb05: Dac B in Electr. Gr. 3 Data Register		Enable	DAC Data
0xb06: Dac A in Electr. Gr. 4 Data Register		Enable	DAC Data

0xb07: Dac B in Electr. Gr. 4 Data Register		Enable	DAC Data
0xb08: Dac A in Electr. Gr. 5 Data Register		Enable	DAC Data
0xb09: Dac B in Electr. Gr. 5 Data Register		Enable	DAC Data
0xb0a: Dac A in Electr. Gr. 6 Data Register		Enable	DAC Data
0xb0b: Dac B in Electr. Gr. 6 Data Register		Enable	DAC Data
0xb80: Offset Register for DAC A 1			Offset Correction Value for DAC A in Current Mode
0xb81: Offset Register for DAC B 1			Offset Correction Value for DAC B in Current Mode
0xb82: Offset Register for DAC A 2			Offset Correction Value for DAC A in Current Mode
0xb83: Offset Register for DAC B 2			Offset Correction Value for DAC B in Current Mode

0xb84: Offset Register for DAC A 3		Offset Correction Value for DAC A in Current Mode
0xb85: Offset Register for DAC B 3		Offset Correction Value for DAC B in Current Mode
0xb86: Offset Register for DAC A 4		Offset Correction Value for DAC A in Current Mode
0xb87: Offset Register for DAC B 4		Offset Correction Value for DAC B in Current Mode
0xb88: Offset Register for DAC A 5		Offset Correction Value for DAC A in Current Mode
0xb89: Offset Register for DAC B 5		Offset Correction Value for DAC B in Current Mode
0xb8a: Offset Register for DAC A 6		Offset Correction Value for DAC A in Current Mode
0xb8b: Offset Register for DAC B 6		Offset Correction Value for DAC B in Current Mode
0xbc0: DAC A in Electr. Gr. 1 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc1: DAC B in Electr. Gr. 1 Weighting Factor		Weighting Factor in Q1.16 Format

0xbc2: DAC A in Electr. Gr. 2 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc3: DAC B in Electr. Gr. 2 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc4: DAC A in Electr. Gr. 3 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc5: DAC B in Electr. Gr. 3 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc6: DAC A in Electr. Gr. 4 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc7: DAC B in Electr. Gr. 4 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc8: DAC A in Electr. Gr. 5 Weighting Factor		Weighting Factor in Q1.16 Format
0xbc9: DAC B in Electr. Gr. 5 Weighting Factor		Weighting Factor in Q1.16 Format
0xbca: DAC A in Electr. Gr. 6 Weighting Factor		Weighting Factor in Q1.16 Format

0xbcb: DAC B in Electr. Gr. 6 Weighting Factor		Weighting Factor in Q1.16 Format

*Electrode Group::

```
0: HS1 Electrodes
1: HS2 Electrodes
2: HS3 Electrodes
3: HS4 Electrodes
4: SCU LED 1 Stimulator
5: SCU LED 2 Stimulator
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xc50: Electrode Config ID																									Electrode Config ID							
0xc51: Config ID Source																										Electrode Config ID source select*						
0xc60: External electrode enable																									External stimulation enable (2 bit per HS - Stim A+B)							
0xc70: Electrode Mode Configuration	Electrodes 31 to 0 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc71: Electrode Mode Configuration	Electrodes 63 to 32 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc72: Electrode Mode Configuration	Electrodes 95 to 64 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc73: Electrode Mode Configuration	Electrodes 127 to 96 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc74: Electrode Mode Configuration	Electrodes 159 to 128 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc75: Electrode Mode Configuration	Electrodes 191 to 160 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc76: Electrode Mode Configuration	Electrodes 223 to 192 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xc77: Electrode Mode Configuration	Electrodes 255 to 224 (Manual mode: '1' / Automatic mode: '0', 1 bit per electrode)																															
0xca0: Electrode Enable	Electrodes 31 to 0, 1 bit per electrode																															

0xca1: Electrode Enable	Electrodes 63 to 32, 1 bit per electrode
0xca2: Electrode Enable	Electrodes 95 to 64, 1 bit per electrode
0xca3: Electrode Enable	Electrodes 127 to 96, 1 bit per electrode
0xca4: Electrode Enable	Electrodes 159 to 128, 1 bit per electrode
0xca5: Electrode Enable	Electrodes 191 to 160, 1 bit per electrode
0xca6: Electrode Enable	Electrodes 223 to 192, 1 bit per electrode
0xca7: Electrode Enable	Electrodes 255 to 224, 1 bit per electrode
0xcd0: Electrode MUX position when stimulus is active	Electrodes 15 to 0, 2 bit per electrode**
0xcd1: Electrode MUX position when stimulus is active	Electrodes 31 to 16, 2 bit per electrode**
0xcd2: Electrode MUX position when stimulus is active	Electrodes 47 to 32, 2 bit per electrode**
0xcd3: Electrode MUX position when stimulus is active	Electrodes 63 to 48, 2 bit per electrode**
0xcd4: Electrode MUX position when stimulus is active	Electrodes 79 to 64, 2 bit per electrode**
0xcd5: Electrode MUX position when stimulus is active	Electrodes 95 to 80, 2 bit per electrode**
0xcd6: Electrode MUX position when stimulus is active	Electrodes 111 to 96, 2 bit per electrode**
0xcd7: Electrode MUX position when stimulus is active	Electrodes 127 to 112, 2 bit per electrode**
0xcd8: Electrode MUX position when stimulus is active	Electrodes 143 to 128, 2 bit per electrode**

0xcd9: Electrode MUX position when stimulus is active	Electrodes 159 to 144, 2 bit per electrode**
0xcda: Electrode MUX position when stimulus is active	Electrodes 175 to 160, 2 bit per electrode**
0xcdb: Electrode MUX position when stimulus is active	Electrodes 191 to 176, 2 bit per electrode**
0xcdc: Electrode MUX position when stimulus is active	Electrodes 207 to 192, 2 bit per electrode**
0xcdd: Electrode MUX position when stimulus is active	Electrodes 223 to 208, 2 bit per electrode**
0xcde: Electrode MUX position when stimulus is active	Electrodes 239 to 224, 2 bit per electrode**
0xcdf: Electrode MUX position when stimulus is active	Electrodes 255 to 240, 2 bit per electrode**

[*] ***Electrode Config ID Source Select:***

```
00 00000: Trigger  0 ID
00 00001: Trigger  1 ID
00 00010: Trigger  2 ID
00 00011: Trigger  3 ID
00 00100: Trigger  4 ID
00 00101: Trigger  5 ID
00 00110: Trigger  6 ID
00 00111: Trigger  7 ID
00 01000: Trigger  8 ID
00 01001: Trigger  9 ID
00 01010: Trigger 10 ID
00 01011: Trigger 11 ID
00 01100: Reserved
  ...
00 11111: Reserved

01 00000: Sideband  1, bits 15:8
01 00001: Sideband  2, bits 15:8
01 00010: Sideband  3, bits 15:8
01 00011: Sideband  4, bits 15:8
```

```
01 00100: Sideband  5, bits 15:8
01 00101: Sideband  6, bits 15:8
01 00110: Sideband  7, bits 15:8
01 00111: Sideband  8, bits 15:8
01 01000: Sideband  9, bits 15:8
01 01001: Sideband 10, bits 15:8
01 01010: Sideband 11, bits 15:8
01 01100: Reserved
  ...
01 11111: Reserved

10 XXXXX: Manual Register

11 XXXXX: Reserved
```

** ***Electrode MUX position:***

```
00: electrode to ADC
01: DAC 0
10: DAC 1
11: GND (Impedance test, only in manual mode)
```

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xf00: Memory Address	Adress																															
0xf04: Memory Data	Byte 4								Byte 3								Byte 2								Byte 1							
0xf10: Max used Memory Groups																												# of Maximum used Memory Groups (1 - 18)				
0xf11: MEM Segments Shift																														Segments needed*		
0xf12: Memory Pointer Config																																Trigger Ptr. Config
0xf80: Memory Group 0 DAC Data Write Register	Stimulation Data Vector**																															

0xf81: Memory Group 0 SBS Data Write Register	Stimulation Data Vector**
0xf82: Memory Group 1 DAC Data Write Register	Stimulation Data Vector**
0xf83: Memory Group 1 SBS Data Write Register	Stimulation Data Vector**
0xf84: Memory Group 2 DAC Data Write Register	Stimulation Data Vector**
0xf85: Memory Group 2 SBS Data Write Register	Stimulation Data Vector**
0xf86: Memory Group 3 DAC Data Write Register	Stimulation Data Vector**
0xf87: Memory Group 3 SBS Data Write Register	Stimulation Data Vector**
0xf88: Memory Group 4 DAC Data Write Register	Stimulation Data Vector**
0xf89: Memory Group 4 SBS Data Write Register	Stimulation Data Vector**

0xf8a: Memory Group 5 DAC Data Write Register	Stimulation Data Vector**
0xf8b: Memory Group 5 SBS Data Write Register	Stimulation Data Vector**
0xf8c: Memory Group 6 DAC Data Write Register	Stimulation Data Vector**
0xf8d: Memory Group 6 SBS Data Write Register	Stimulation Data Vector**
0xf8e: Memory Group 7 DAC Data Write Register	Stimulation Data Vector**
0xf8f: Memory Group 7 SBS Data Write Register	Stimulation Data Vector**
0xf90: Memory Group 8 DAC Data Write Register	Stimulation Data Vector**
0xf91: Memory Group 8 SBS Data Write Register	Stimulation Data Vector**
0xf92: Memory Group 9 DAC Data Write Register	Stimulation Data Vector**

0xf93: Memory Group 9 SBS Data Write Register	Stimulation Data Vector**
0xf94: Memory Group 10 DAC Data Write Register	Stimulation Data Vector**
0xf95: Memory Group 10 SBS Data Write Register	Stimulation Data Vector**
0xf96: Memory Group 11 DAC Data Write Register	Stimulation Data Vector**
0xf97: Memory Group 11 SBS Data Write Register	Stimulation Data Vector**

**shift value decoding:*

```
 0:   1 Segment
 1:   2 Segments
 2:   4 Segments
 3:   8 Segments
 4:  16 Segments
 5:  32 Segments
 6:  64 Segments
 7: 128 Segments
 8: 256 Segments
```

***Data Vector decoding:*

```
Bit 31: Reserved
Bit 30 - 28:
    000: DAC/Sideband data vector
    001: loop pointer vector
    010: Long loop pointer vector
    011: Long loop control vector
    111: END command
```

DAC/Sideband data vector (000):

```
Bit 27: Reserved
Bit 26: Repeat Timebase (0: 20 us, 1: 1000*20us)
Bit 25 – 16: Number of Repeats (0: Pattern is used 1x Timebase; 1: Pattern is used for 2x Timebase; ...)
Bit 15 – 0 : DAC data value (unsigned 16 bit value, 0x8000 is zero level) / SBS data value
    SBS Bit 0    : Amplifier Protection Switch/Blanking
    SBS Bit 3    : Stimulation Switch
    SBS Bit 4    : Stimulus Select
    SBS Bit 8-15 : Electrode Config ID
```

loop pointer vector (001):

```
Bit 27 – 26: Loop Level
Bit 25 – 16: Number of Repeats (2: Vectors are repeated once, thus used twice)
Bit 15 – 0 : Address Offset (Number of Vectors to jump backward, 1: One Vector before the LoopPtr is repeated)
```

Long loop pointer vector (010):

```
Bit 27 – 0 : Address Offset (Number of Vectors to jump backward)
```

Long loop control vector (011):

```
Bit 27 – 0 : Number of Repeats
```

END command (111):

```
Bit 27 – 0 : Reserved
```

Headstage Address Map (Address bits 10-0) Base Address SCU1: 0xA000, 0xA800, 0xB000, 0xB800; SCU2 :0xE000, 0xE800, 0xF000, 0xF800

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000: Device ID																									0x0c = ME2100 SCU							
0x001: Serial number low	lower 32 bit of SCU serial number, read as 4 ASCII bytes																															
0x002: Serial number high	higher 32 bit of SCU serial number, read as 4 ASCII bytes																															
0x004: FPGA Version																	FPGA firmware version															
0x008: PCB Revision																									Assembly Version				PCB Revision			
0x00c: ADC Power																															enable 18 V	

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x020: Reset																																Reset

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x031: (RO) Flash Size																																
0x032: Write/Read Address																																
0x033: Write/Read Data																																

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x040: persistant command : 0x6 next write is persistant																																

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x100: Number of detection electrodes	32 Electrodes																															
0x110: ADC Range	ADC range (0x00231860 = 2300 mV)																															
0x114: ADC Resolution per bit	ADC Resolution (0x80000112 = 274 nV/bit)																															
0x118: ADC Bit Count	ADC Resolution in bits (0x00000018 = 24 bit)																															
0x11c: Gain	Gain of the DACQ System (0x80002710 = gain 10.0)																															
0x120: Limitations	Limitaions of this System can be written here																															
0x130: Max Sampling Freqency	Maximum Frequenzy that is allowed to be set at configuration for the user (0x0000C350 = 50 kHz)																															
0x180: Voltage Range	Voltage range (0x0000 2710 = 10000 mV)																															
0x184: Voltage Resolution	Voltage resolution (0x8000 01F4 = 500 uV)																															
0x188: Current Range	Current range (0x0000 03E8 = 1000 uA)																															
0x18c: Current Resolution	Current resolution (0x0000 0032 = 50 nA)																															
0x1c0: DAC Properties	Number of DAC Channels (2)																												Number of DAC memory channels (2)			
0x1c4: DAC Resolution																													Resolution in bits (16)			
0x1e0: Number of Stimulation Electrodes																													Stimulation Electrodes (32)			

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x200: ADS131A04 Command																	SPI Command															
0x220: ADC Select for Read																									ADC Number							
0x240: ADS131A04 Reg 0x00 ID_MSB																									NU_CH							
0x241: ADS131A04 Reg 0x01 ID_LSB																									REV_ID							
0x242: ADS131A04 Reg 0x02 STAT_1																										F_OPC	F_SPI	F_ADCIN	F_WDT	F_RESYNC	F_DRDY	F_CHECK
0x243: ADS131A04 Reg 0x03 STAT_P																													F_IN4P	F_IN3P	F_IN2P	F_IN1P
0x244: ADS131A04 Reg 0x03 STAT_N																													F_IN4N	F_IN3N	F_IN2N	F_IN1N
0x245: ADS131A04 Reg 0x05 STAT_S																														F_STARTUP	F_CS	F_FRAME
0x246: ADS131A04 Reg 0x06 ERROR_CNT																									ER							
0x247: ADS131A04 Reg 0x07 STAT_M2																											M2PIN[1:0]		M1PIN[1:0]			M0PIN[1:0]	
0x24b: ADS131A04 Reg 0x0B A_SYS_CFG																									VNCPEN	HRM	1	VREF_4V	INT_REFEN	COMP_TH[2:0]		
0x24c: ADS131A04 Reg 0x0C D_SYS_CFG																									WDT_EN	CRC_MODE	DNDLY[1:0]		HIZDLY[1:0]		FIXED	CRC_EN
0x24d: ADS131A04 Reg 0x0D CLK1																									CLKSRC				CLK_DIV[2:0]			

0x24e: ADS131A04 Reg 0x0E CLK2		ICLK_DIV[2:0] 0 OSR[3:0]
0x24f: ADS131A04 Reg 0x0F ADC_ENA		ENA[3:0]
0x251: ADS131A04 Reg 0x11 ADC1		GAIN1_[2:0]
0x252: ADS131A04 Reg 0x12 ADC2		GAIN2_[2:0]
0x253: ADS131A04 Reg 0x12 ADC3		GAIN3_[2:0]
0x254: ADS131A04 Reg 0x14 ADC4		GAIN4_[2:0]

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x400: ADC 1 Data									ADC Data																							
0x401: ADC 2 Data									ADC Data																							
0x402: ADC 3 Data									ADC Data																							
0x403: ADC 4 Data									ADC Data																							
0x404: ADC 5 Data									ADC Data																							
0x405: ADC 6 Data									ADC Data																							
0x406: ADC 7 Data									ADC Data																							
0x407: ADC 8 Data									ADC Data																							
0x408: ADC 9 Data									ADC Data																							
0x409: ADC 10 Data									ADC Data																							
0x40a: ADC 11 Data									ADC Data																							
0x40b: ADC 12 Data									ADC Data																							
0x40c: ADC 13 Data									ADC Data																							
0x40d: ADC 14 Data									ADC Data																							
0x40e: ADC 15 Data									ADC Data																							
0x40f: ADC 16 Data									ADC Data																							

0x410: ADC 17 Data		ADC Data
0x411: ADC 18 Data		ADC Data
0x412: ADC 19 Data		ADC Data
0x413: ADC 20 Data		ADC Data
0x414: ADC 21 Data		ADC Data
0x415: ADC 22 Data		ADC Data
0x416: ADC 23 Data		ADC Data
0x417: ADC 24 Data		ADC Data
0x418: ADC 25 Data		ADC Data
0x419: ADC 26 Data		ADC Data
0x41a: ADC 27 Data		ADC Data
0x41b: ADC 28 Data		ADC Data
0x41c: ADC 29 Data		ADC Data
0x41d: ADC 30 Data		ADC Data
0x41e: ADC 31 Data		ADC Data
0x41f: ADC 32 Data		ADC Data
0x420: ADC 33 Data		ADC Data
0x421: ADC 34 Data		ADC Data
0x422: ADC 35 Data		ADC Data
0x423: ADC 36 Data		ADC Data
0x424: ADC 37 Data		ADC Data
0x425: ADC 38 Data		ADC Data
0x426: ADC 39 Data		ADC Data
0x427: ADC 40 Data		ADC Data
0x428: ADC 41 Data		ADC Data

0x429: ADC 42 Data		ADC Data
0x42a: ADC 43 Data		ADC Data
0x42b: ADC 44 Data		ADC Data
0x42c: ADC 45 Data		ADC Data
0x42d: ADC 46 Data		ADC Data
0x42e: ADC 47 Data		ADC Data
0x42f: ADC 48 Data		ADC Data
0x430: ADC 49 Data		ADC Data
0x431: ADC 50 Data		ADC Data
0x432: ADC 51 Data		ADC Data
0x433: ADC 52 Data		ADC Data
0x434: ADC 53 Data		ADC Data
0x435: ADC 54 Data		ADC Data
0x436: ADC 55 Data		ADC Data
0x437: ADC 56 Data		ADC Data
0x438: ADC 57 Data		ADC Data
0x439: ADC 58 Data		ADC Data
0x43a: ADC 59 Data		ADC Data
0x43b: ADC 60 Data		ADC Data
0x43c: ADC 61 Data		ADC Data
0x43d: ADC 62 Data		ADC Data
0x43e: ADC 63 Data		ADC Data
0x43f: ADC 64 Data		ADC Data

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x600: Filter 1 coefficent b[0]	Filter coefficent b[0] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x602: Filter 1 coefficent b[1]	Filter coefficent b[1] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x603: Filter 1 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)																															
0x604: Filter 1 coefficent b[2]	Filter coefficent b[2] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x605: Filter 1 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)																															
0x606: Filter 1 coefficent lower bits	lower bits of a[2]																lower bits of a[1]															
0x607: Filter 1 control																															Enable Blanking	Enable Filter
0x608: Filter 2 coefficent b[0]	Filter coefficent b[0] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x60a: Filter 2 coefficent b[1]	Filter coefficent b[1] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x60b: Filter 2 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)																															
0x60c: Filter 2 coefficent b[2]	Filter coefficent b[2] as Q1.16 value																		0 to extend coefficient to Q1.30													
0x60d: Filter 2 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)																															
0x60e: Filter 2 coefficent lower bits	lower bits of a[2]																lower bits of a[1]															

0x60f: Filter 2 control			Enable Blanking	Enable Filter
0x610: Filter 3 coefficent b[0]	Filter coefficent b[0] as Q1.16 value	0 to extend coefficient to Q1.30		
0x612: Filter 3 coefficent b[1]	Filter coefficent b[1] as Q1.16 value	0 to extend coefficient to Q1.30		
0x613: Filter 3 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)			
0x614: Filter 3 coefficent b[2]	Filter coefficent b[2] as Q1.16 value	0 to extend coefficient to Q1.30		
0x615: Filter 3 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)			
0x616: Filter 3 coefficent lower bits	lower bits of a[2]		lower bits of a[1]	
0x617: Filter 3 control			Enable Blanking	Enable Filter
0x618: Filter 4 coefficent b[0]	Filter coefficent b[0] as Q1.16 value	0 to extend coefficient to Q1.30		
0x61a: Filter 4 coefficent b[1]	Filter coefficent b[1] as Q1.16 value	0 to extend coefficient to Q1.30		
0x61b: Filter 4 coefficent a[1]	Filter coefficent a[1] as Q1.30 value (Q1.33 together with lower bits register)			
0x61c: Filter 4 coefficent b[2]	Filter coefficent b[2] as Q1.16 value	0 to extend coefficient to Q1.30		
0x61d: Filter 4 coefficent a[2]	Filter coefficent a[2] as Q1.30 value (Q1.33 together with lower bits register)			

0x61e: Filter 4 coefficent lower bits	lower bits of a[2]		lower bits of a[1]			
0x61f: Filter 4 control					Enable Blanking	Enable Filter
0x620: Filter 2b coefficent b[0]	Filter coefficent b[0] as Q1.16 value		0 to extend coefficient to Q1.30			
0x622: Filter 2b coefficent b[1]	Filter coefficent b[1] as Q1.16 value		0 to extend coefficient to Q1.30			
0x623: Filter 2b coefficent a[1]	Filter coefficent a[1] as Q1.30 value for one clock after blank (Q1.33 together with lower bits register)					
0x624: Filter 2b coefficent b[2]	Filter coefficent b[2] as Q1.16 value		0 to extend coefficient to Q1.30			
0x625: Filter 2b coefficent a[2]	Filter coefficent a[2] as Q1.30 value for one clock after blank (Q1.33 together with lower bits register)					
0x626: Filter 2b coefficent lower bits	lower bits of a[2]		lower bits of a[1]			
0x630: hardware filter frequency	Corner frequency of hardware filter in mHz					
0x631: hardware filter information	filter order	band: lowpass	family		0: hardware filter	enabled
0x634: highpass filter frequency	Corner frequency of highpass filter in mHz					
0x635: highpass filter information	filter order	band: highpass	family		1: software filter	enabled
0x638: lowpass filter frequency	Corner frequency of lowpass filter in mHz					

0x639: lowpass filter information	filter order	band: lowpass	family		1: software filter	enabled

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x702: DAC C Value																	DAC Data															
0x780: DAC A Offset																	DAC Offset															
0x781: DAC B Offset																	DAC Offset															

Quelle(n) und Bearbeiter des/der Artikel(s)

MEA2100-Mini User Guide *Quelle*: http://wiki.mcs.de.com/index.php?oldid=24640 *Bearbeiter*: Jesinger, 9 anonyme Bearbeitungen