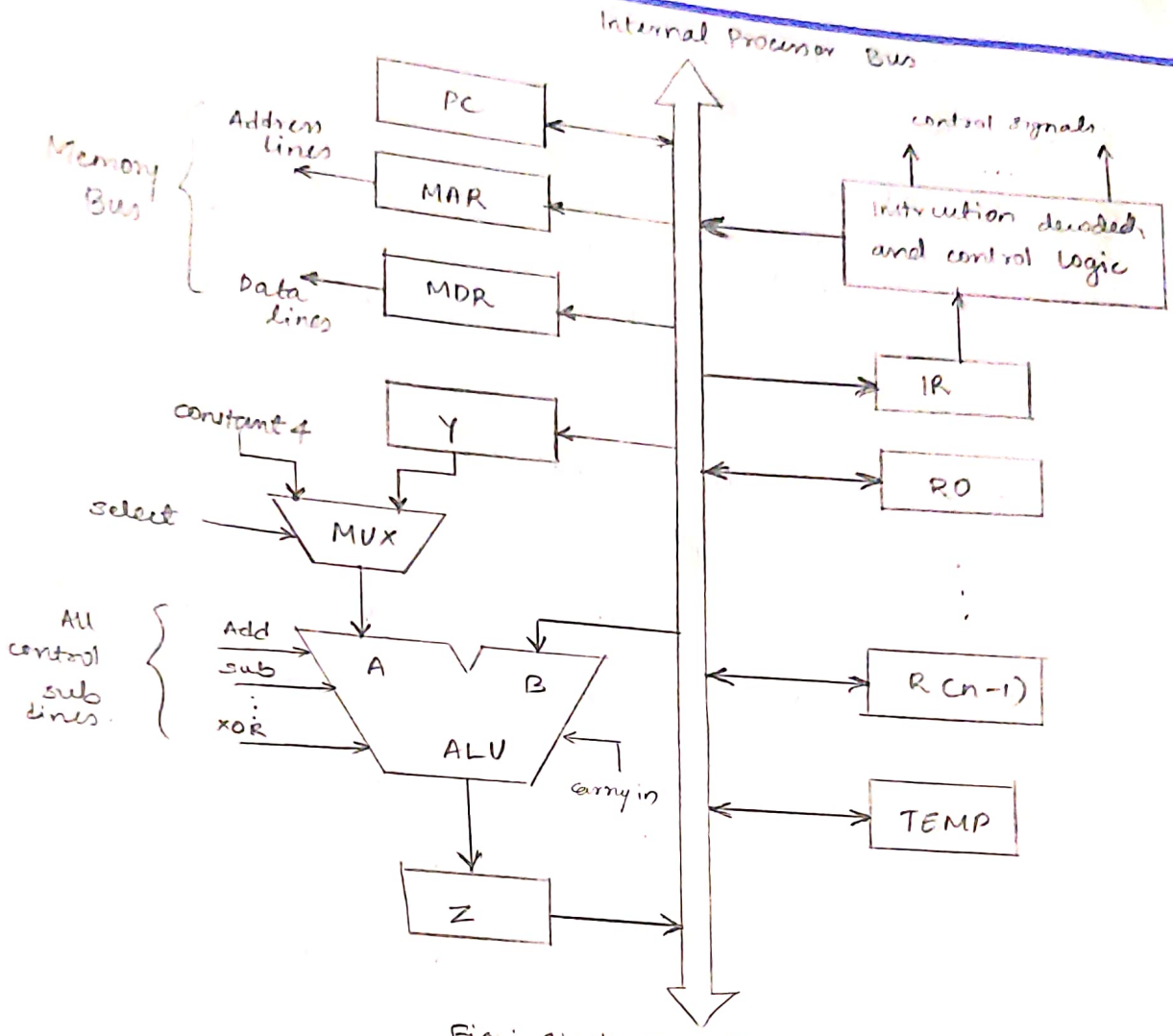


Fig : Single Bus Organizations

- ALU and all the registers are interconnected via a single common bus.
- The data and address lines of the external memory bus connected to the internal processor bus via the memory data register MDR and the memory address register, MAR respectively
- Register MDR has two inputs and two outputs
- Data may be loaded into MDR either from the memory bus or from the internal processor bus.
- The data stored in MDR may be placed on either bus.

- The input of MAR is connected to its internal bus and its output is connected to the external bus.
- The control lines of the memory bus are connected to the instruction decoder and control logic.
- This unit is responsible for issuing the signals that control the operation of all the units inside the processor and for increasing with the memory bus.
- The MUX selects either the output of register y or a constant value 4 to be protected or input A of the ALU.
- The constant 4 is used to increment the contents of the program counter

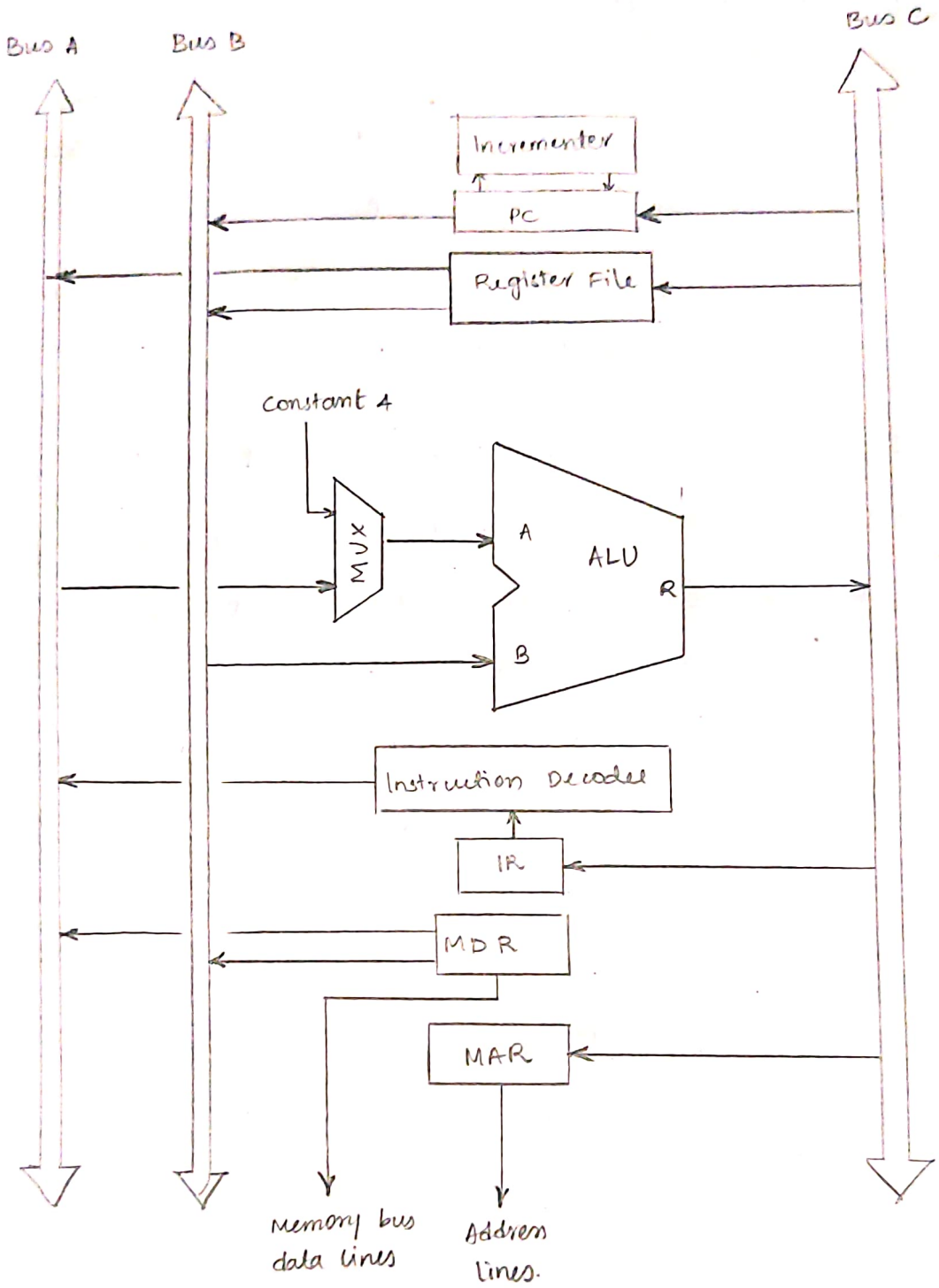
With few exceptions, the operations specified by an instruction can be caused out by performing one or more of the following actions.

- Read the contents of a given memory location and load them into a processor register.
- Read data from one or more processor registers.
- Perform an arithmetic or logic operations and place the result into a processor register.
- Share data from a processor register into a given memory location.

Multiple Bus Organization

- To reduce the number of steps needed, most commercial processors provide multiple internal paths that enable several transfers to take place in parallel.
- Figure shows a three bus structure used to connect the register and the ALU of the processor.
- All general purpose register are combined into a single block called the register file. It consists of three parts There are two outputs, allowing the concepts of two different registers to be accessed simultaneously and have their contents placed on bus A and B. The third part always the data on bus A and B. The third part always the data on bus C to be loaded into a third register during the same clock cycle
- Bus A and B are used to transfer the source operands the A and B inputs of the ALU, where an arithmetic or logic operation may be performed. The result is transferred to the destination over bus C.

Incrementer unit, which is used to increment the PC by 4.

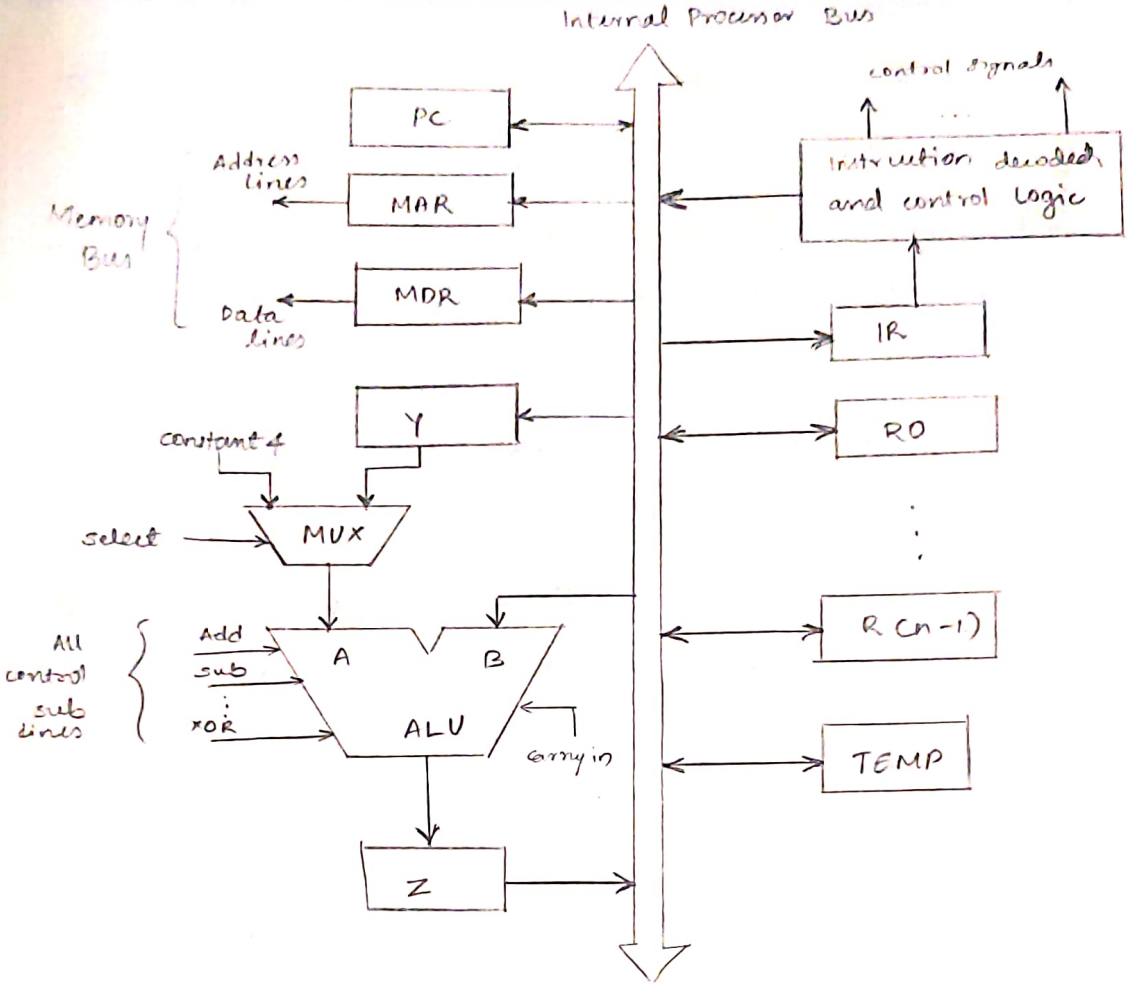


Ex. Consider 3 operands instructions

ADD R_4, R_5, R_6

step Action

1. PC_{out} R=B MAR in, Read IncPC
2. WMFC
3. MDR_{outB}; R=B, IR_{in}
4. $R_{4\,outA}$, $R_{5\,outB}$, Select A, Add, $R6_{in}$, End.



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