

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination June 2022 (2019 scheme)

**Course Code: CST202****Course Name: Computer Organization and Architecture****Max. Marks: 100****Duration: 3 Hours****PART A***(Answer all questions; each question carries 3 marks)***Marks**

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|----|---|---|
| 1 | Describe auto increment and decrement addressing mode with help of example? | 3 |
| 2 | Name the registers which are connected to both external and internal bus? What are the signals associated with these registers? | 3 |
| 3 | Write the register transfer logic format for a conditional control statement, Give an example? | 3 |
| 4 | Discuss the logic used behind the booth multiplication algorithm | 3 |
| 5 | Draw a 3X2 array multiplier? | 3 |
| 6 | Discuss about pipeline hazards? | 3 |
| 7 | Write a note on micro-program control? | 3 |
| 8 | What are different types of control organization? | 3 |
| 9 | What are interrupts, List the sequence of steps following an interrupt request? | 3 |
| 10 | Which design feature of SRAM cells helps in value retention without refresh? | 3 |

PART B*(Answer one full question from each module, each question carries 14 marks)***Module -1**

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|----|---|----|
| 11 | a) Compare and contrast single bus and multi-bus organization of CPU? | 4 |
| | b) Write the three-address, two-address and one-address representations of the operation below with relevant assumptions, evaluate following:
i, $(A+B) * (C+D)$
ii, $C \leftarrow [A] + [B]$ | 10 |
| 12 | a) With the help of a neat figure, describe the data path inside the processor? | 6 |
| | b) Draw the diagram of single bus organization, write the control sequence for the instruction ADD [R2], R3 for the above mentioned single bus organization. | 8 |

Module -2

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|----|---|----|
| 13 | a) Describe processor organization with diagram using
i) scratchpad memory
ii) Two-port memory
iii) Accumulator register | 10 |
| | b) Draw and explain about true/complement circuit? | 4 |

- 14 a) Give the structure of status register, which is connected to 8bit ALU . 8
 b) Design 4-bit combinational logic shifter which will perform the operation given below with 2 control variable H1&H0? 6
 i) Shrl
 ii) clear
 iii) Load all bits with 1

Module -3

- 15 a) Draw the flowchart and explain restoring division method with an example? 6
 b) Describe in detail about data hazards and resolution techniques? 8
 16 a) Draw the flowchart of Booth's multiplication algorithm and multiply -5 X -4 using booth's algorithm? 8
 b) Identify the various types of hazards occurring during the execution of the following program in a pipelined system. Where the pipeline consist of five stages, opcode fetch , instruction decode, operand fetch, execution, store the result. All stages take equal time duration 6

```
MOV [R1],[R2]
MOV R3,[R1]
SUB R2,R3
ADD R1,R3
CALL 5000
MOV R2,R3
```

Module -4

- 17 a) With the help of a diagram explain the functioning of a micro-program sequencer in a micro-programmed controlled processor? 10
 b) Compare instruction formats of horizontal and vertical microinstructions? 4
 18 a) Explain the organization of micro-programmed computer with a block diagram? 8
 b) Explain with an example one flip-flop per state method of control organization? 6

Module -5

- 19 a) Explain in detail about the mechanisms for accessing I/O devices? 9
 b) Discuss about different types of read only memories? 5
 20 a) Explain internal organization of 1 K X 8 memory chip with suitable diagram 5
 b) How does the various mapping scheme present in cache memory differ from each other. 9
