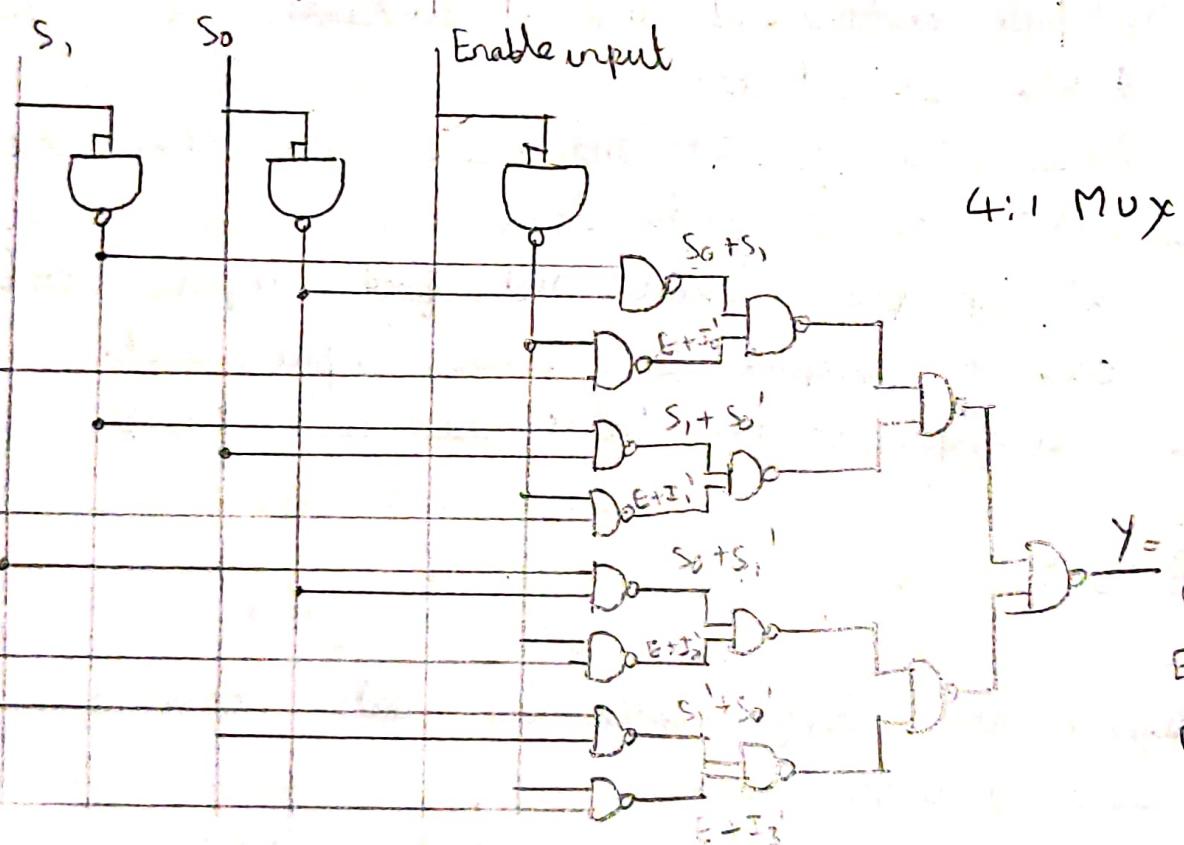


S_1	S_0	E	I_0	I_1	I_2	I_3	Y
x	x	1	x	x	x	x	0
0	0	0	0	x	x	x	0
0	0	0	1	x	x	x	1
0	1	0	x	0	x	x	0
0	1	0	x	1	x	x	1
1	0	0	x	x	0	x	0
1	0	0	x	x	1	x	1
1	1	0	x	x	x	0	0
1	1	0	x	x	x	1	1

Truth Table



$$Y = E'S_1'S_0'I_0 + E'S_1'S_0'I_1 + E'S_1S_0'I_2 + E'S_1S_0'I_3$$

L

$$Y = E'S_1'S_0'I_0 + E'S_1'S_0'I_1 + E'S_1S_0'I_2 + E'S_1S_0'I_3$$

4. Multiplexers and Demultiplexers

b) using gates

AIM:

- a) i) To design and set up 4:1 multiplexer using NAND gates
ii) To design and set up 1:4 demultiplexer using NAND gates
- b) i) To familiarize MUX (8:1) IC 74151
ii) To familiarize DEMUX IC 74154
- b) Realize combinational circuit using MUX IC 74151
i) Half adder using IC 74151

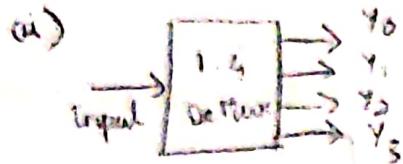
COMPONENTS REQUIRED

IC 7400, IC 7404, IC 7432, IC 74151, IC 74154
IC Trainer Kit

THEORY

- a) Multiplexers are very useful in digital systems.
They transfer a large number of information units over smaller number of channels, under control of selection signals. Multiplexer means many to one. select lines select any input to output

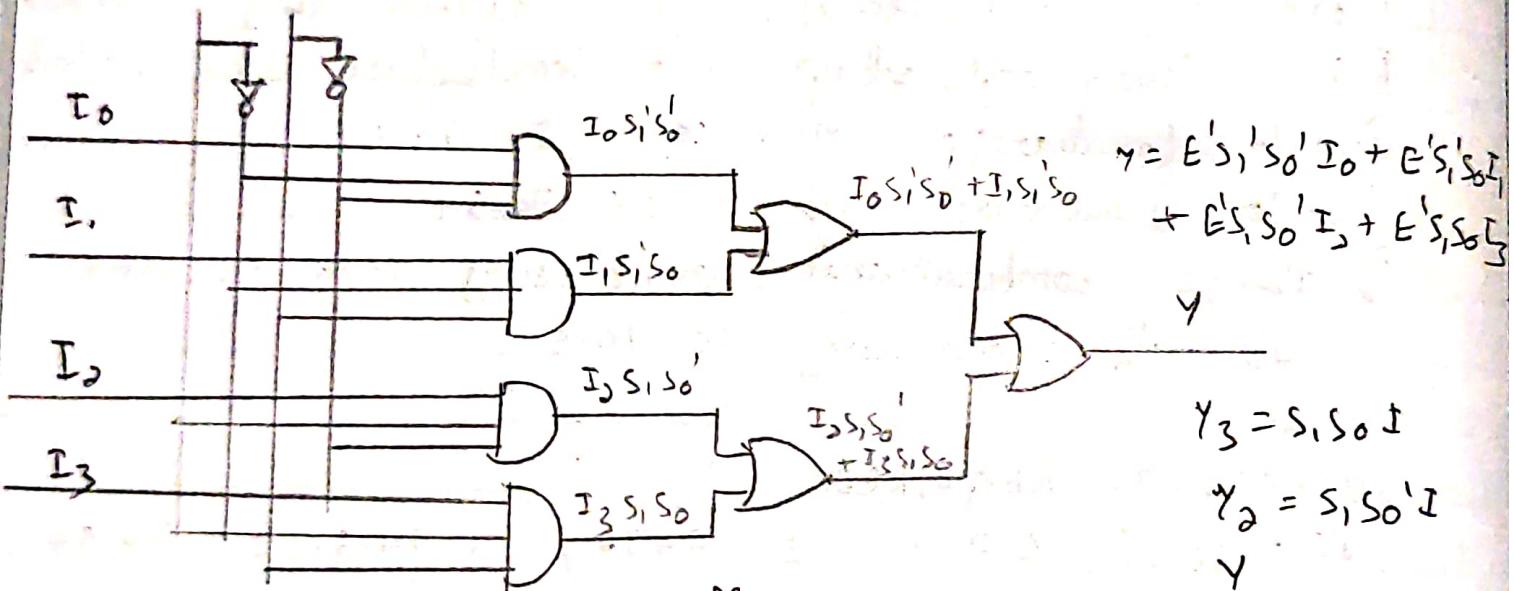
The general multiplexer has 2^n input signals, n control signals and 1 output signal.



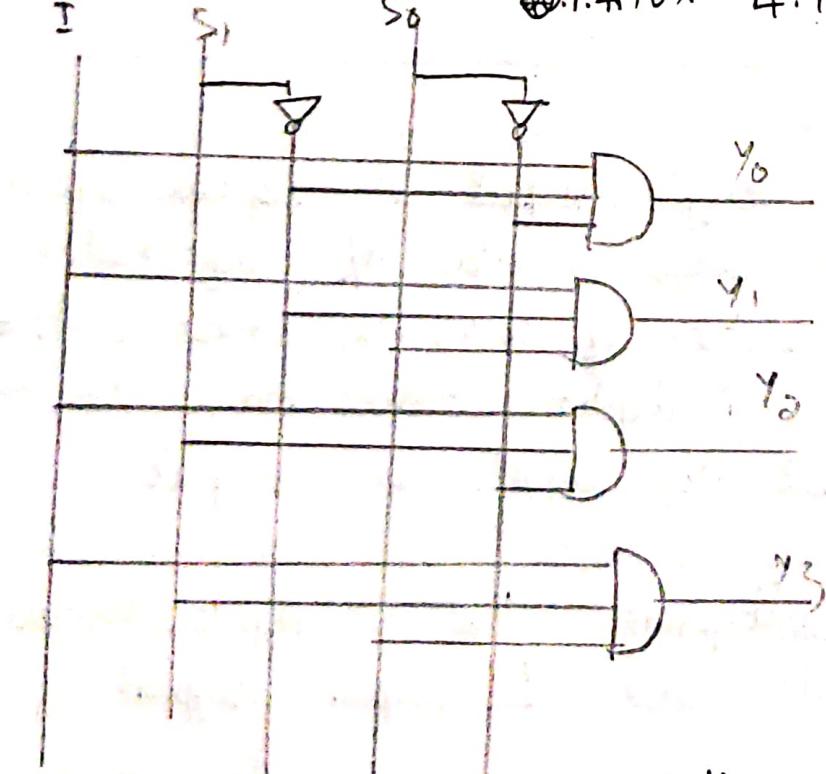
Truth Table

E	D	$S_1 S_0$	Y_3	Y_2	Y_1	Y_0
1	0	X X	X	X	X	X
0	1	0 0	0	0	0	1
0	1	0 1	0	0	1	0
0	1	1 0	0	1	0	0
0	1	1 1	1	0	0	0

(ii) $S_1 \quad S_0$



(iii) $I \quad S_1 \quad S_0 \quad \text{DEMUX}$



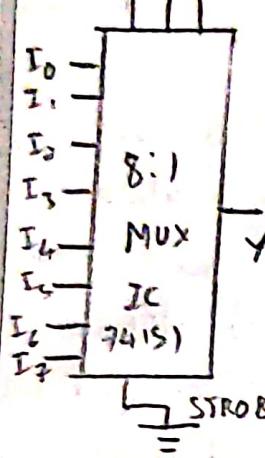
De-multiplexer performs opposite of multiplexers. They transfer a small number of information units over a large number of channels under the control of selection signals. The general de-mux has 1 input signal, n control signal, 2^n output signal. De-mux circuit can be realized using a decoder circuit with enable.

- i) combinational circuits is a circuit in which we combine different gates in the circuit for example encoder, decoder, multiplexer and demultiplexer.
- output depends only on present input
 - No memory
 - n inputs, m outputs

PROCEDURE:

1. Check all components for working
2. Insert the appropriate IC into IC base
3. Make connections as shown in circuit diagrams

(iii)



	V_{cc}	D_0	D_1	D_2	D_3	D_4	D_5	S_1	S_0
16	1	1	1	1	1	1	1	1	1
	1	2	3	4	5	6	7	8	

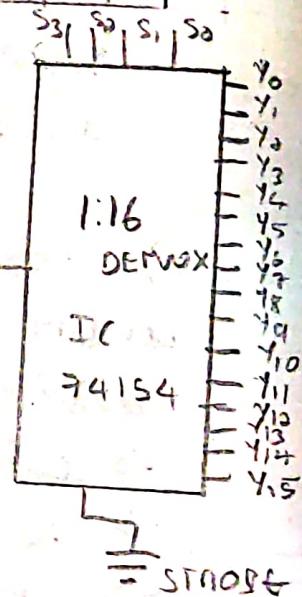
$D_3 \ D_2 \ D_1 \ D_0 \ Y \ \bar{Y} \text{ Strobe GND}$

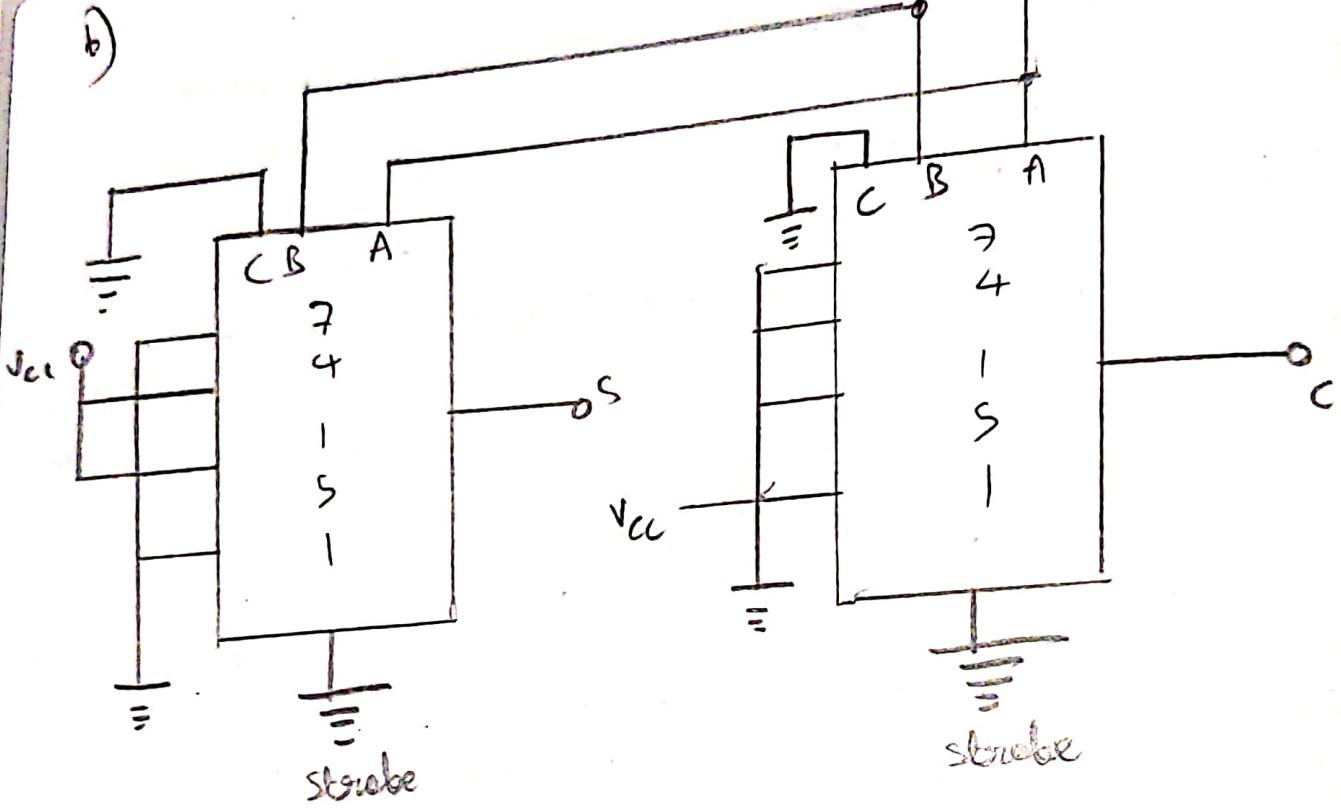
Strobe	S_2	S_1	S_0	Y	\bar{Y}
Active	0	0	0	D_0	D_0
low	0	0	1	D_1	D_1
	0	1	0	D_2	D_2
	0	1	1	D_3	D_3
	1	0	0	D_4	D_4
	1	0	1	D_5	D_5
	1	1	0	D_6	D_6
	1	1	1	D_7	D_7

(iv)

$Y_{15} \ Y_{14} \ Y_{13} \ Y_{12} \ Y_{11}$
24 23 22 21 20 19 18 17 16 15 14 13
IC 74154
1 2 3 4 5 6 7 8 9 10 11 12
$Y_0 \ Y_1 \ Y_2 \ Y_3 \ Y_4 \ Y_5 \ Y_6 \ Y_7 \ Y_8 \ Y_9 \ Y_{10} \text{ GND}$

$S_3 \ S_2 \ S_1 \ S_0$	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	
0 0 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D
0 0 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0 0 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D
0 0 1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0 1 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D
0 1 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0 1 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D
0 1 1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 0 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 0 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 0 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 0 1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 1 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 1 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 1 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1 1 1 1	D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	





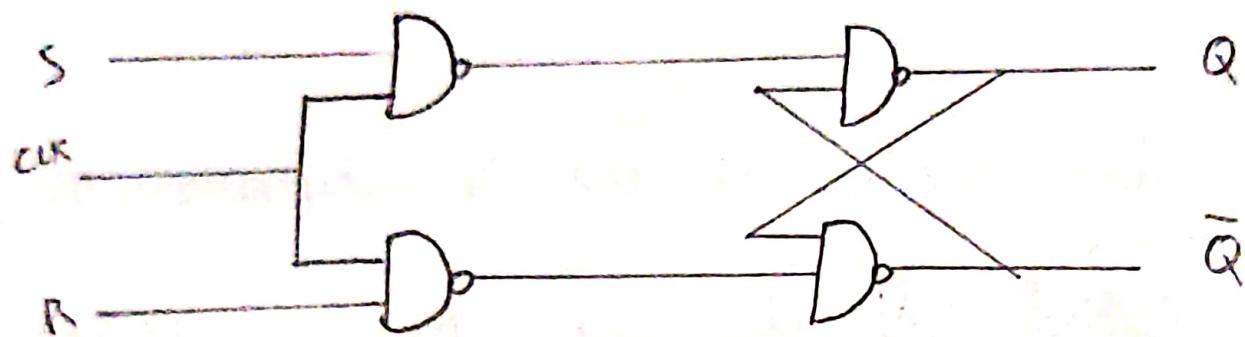
Half adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

RESULT

- a) Realized multiplexers and De Multiplexers using gates
- b) Realized half adder using MUX & DEMUX ICs

1. SR flip flop



CLK	S	R	Q	\bar{Q}
1	0	0	Q	\bar{Q}
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid Previous	
0	x	x	Previous	

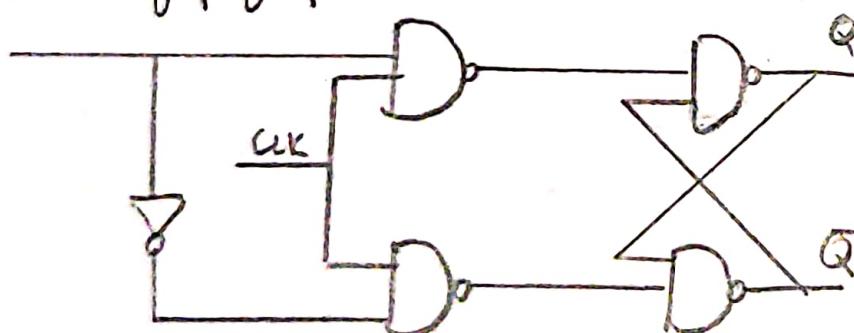
Previous

Reset

Set

Excitation table

2. D flip flop



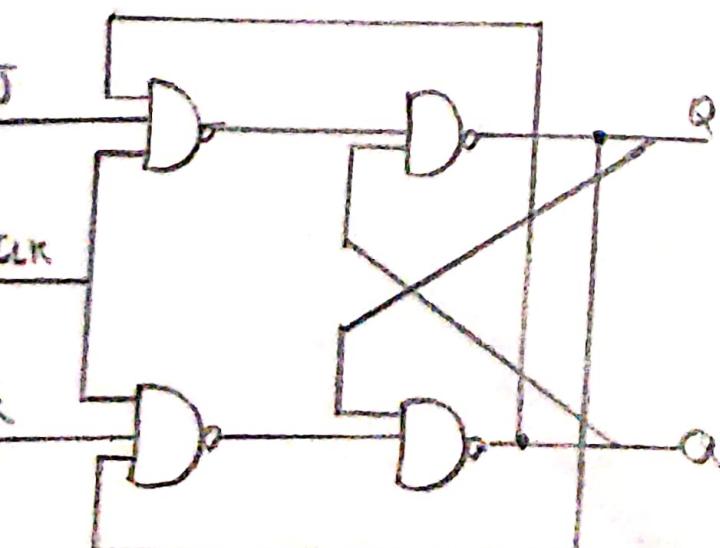
CLK	D	Q	\bar{Q}
1	0	0	1
1	1	1	0
0	x	Q	\bar{Q}

first

set

No change

3. J-K flip flop



CLK	J	K	Q	Q'
1	0	0	Q	\bar{Q}'
1	0	1	0	1
1	1	0	1	0
1	1	1	Q'	Q
0	x	x	Q'	Q

No change

Reset

Set

Toggle

No change

5. Study of flip flops

AIM:

Truth Table verification

To Implementa Flip Flops: SR, D, T, JK and Master slave JK Flip Flops using basic gates

COMPONENTS:

IC Trainer Kit, IC 7400, Patch cords

THEORY:

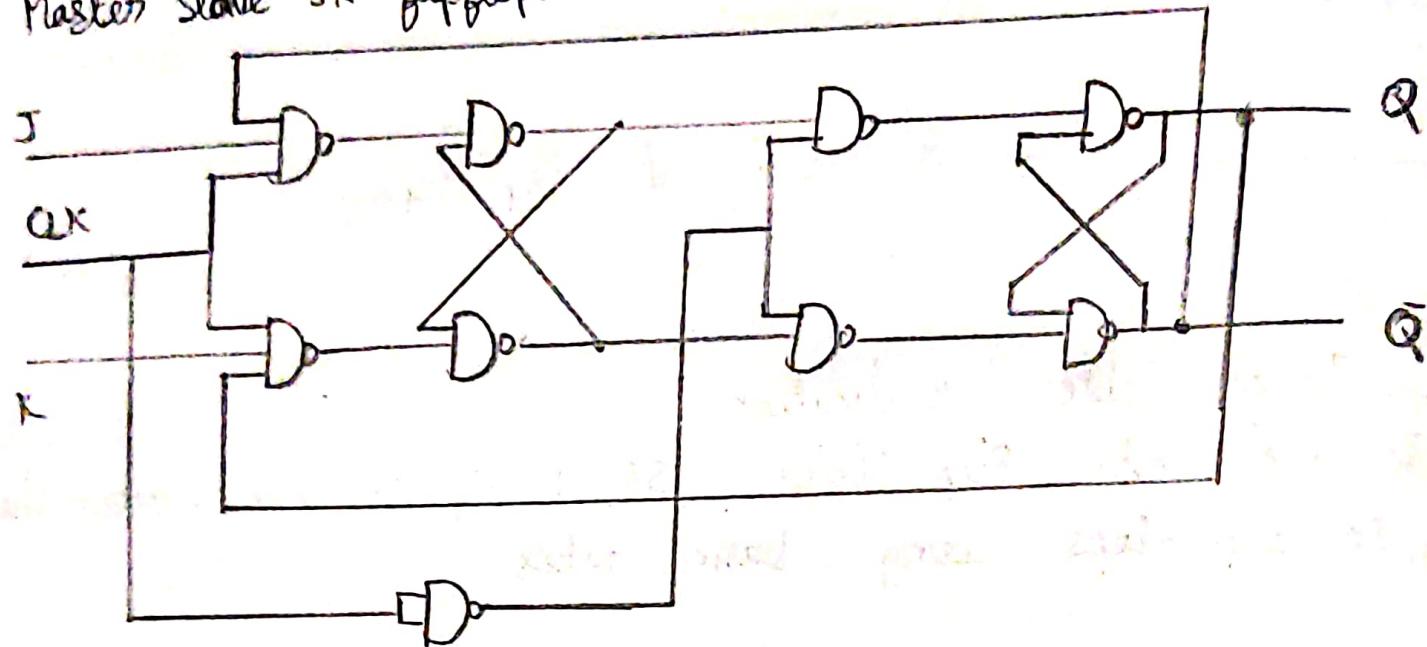
→ Logic circuits incorporate memory cells are called sequential logic circuits. Their output depends not only upon present value of input but also on previous values. They often require a timing generator for their operation.

→ The latch is a basic bi-stable memory element widely used in sequential circuits. Usually with two outputs Q and Q'

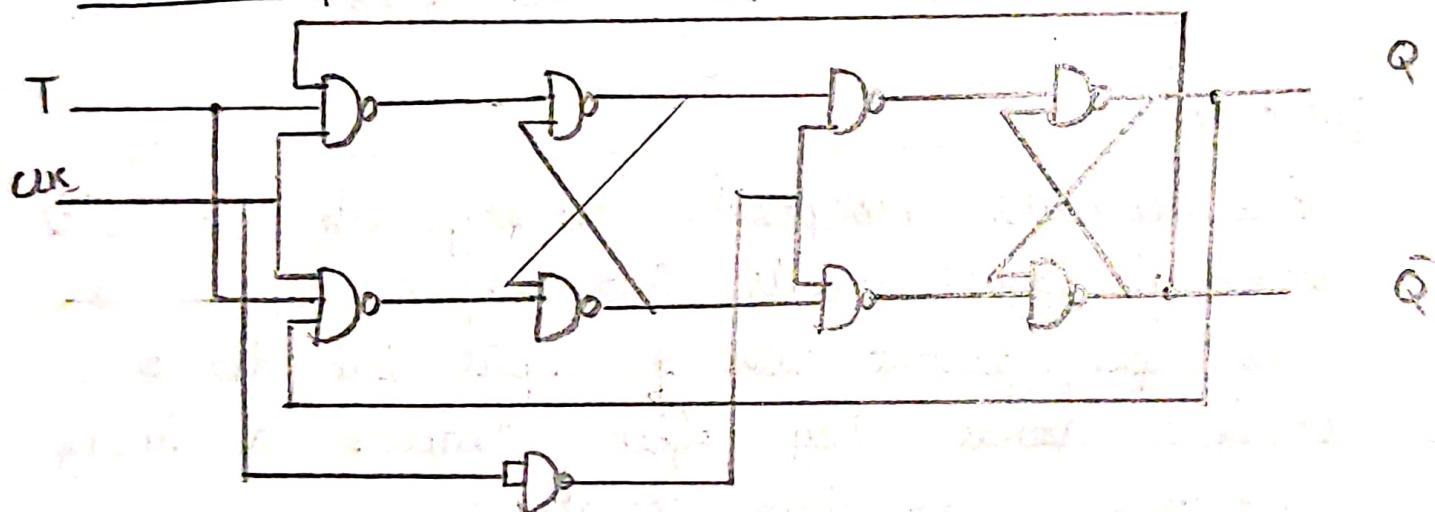
SR LATCH

→ SR latch consist of two cross coupled NAND or NOR gates.

Master slave JK flip flop:



T Flip flop



CLK	T	Q	Q'
1	0	Q	Q'
1	1	Q	Q
0	X	Q	Q'

Previous state

Toggle

Previous state

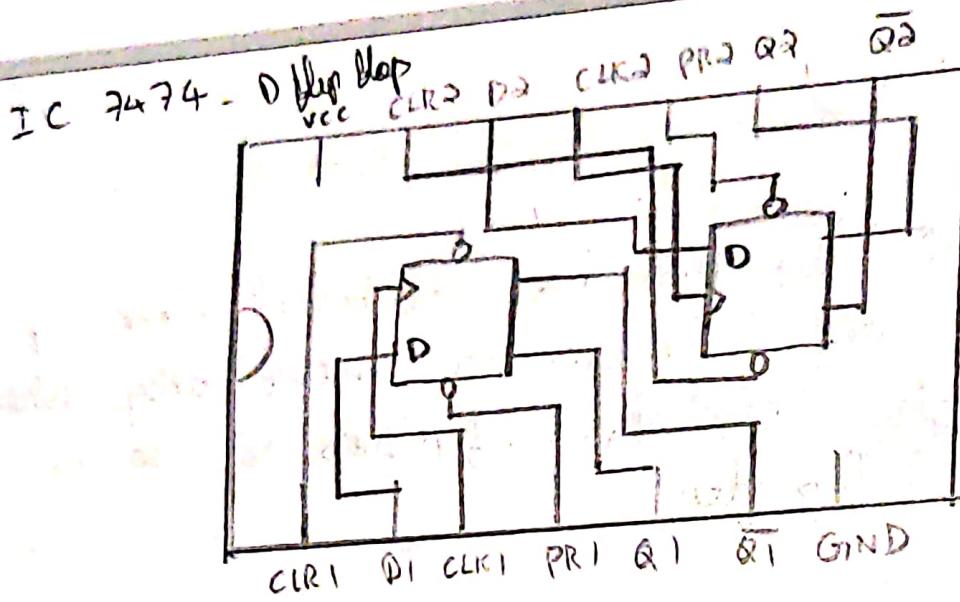
→ A clocked SR flip flop has additional clock input so that S and R inputs are active only when clock is high. Clocked SR flip-flop is also called "enabled" S-R flip-flop.

→ A D latch combines S and R inputs of an S-R latch into one input by adding an inverter.

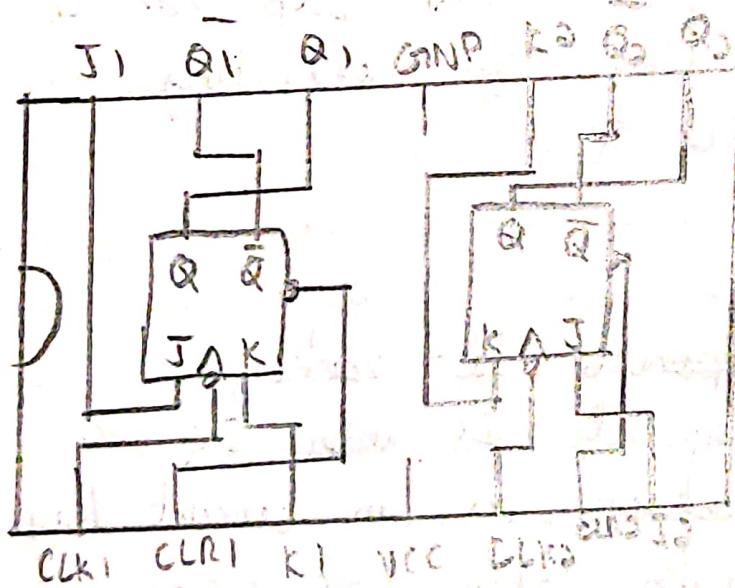
When the clock is high, the output follows the D input and when the clock goes low, the state is latched. A S-R flip flop can be converted to T-flip flop by connecting S input to \bar{Q}_1 and R to Q.

PROCEDURE:

1. Check all components for working
2. Insert appropriate IC into IC base
3. Make connections as in circuit diagram
4. Verify Truth Table and observe outputs



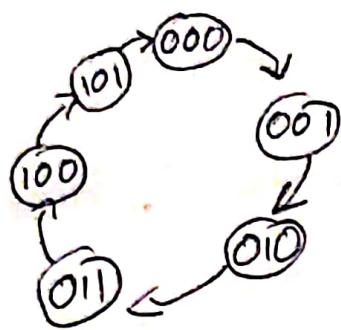
IC 7473 JK FF



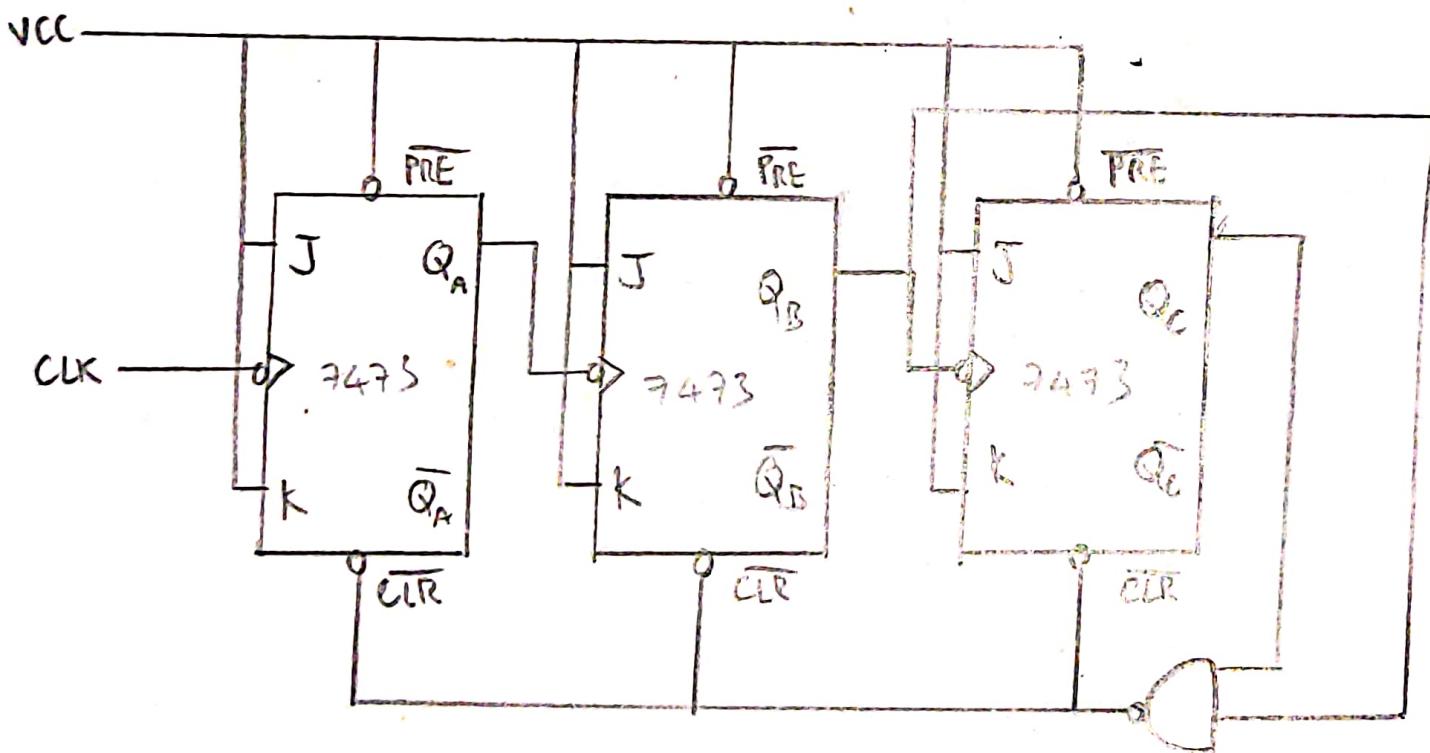
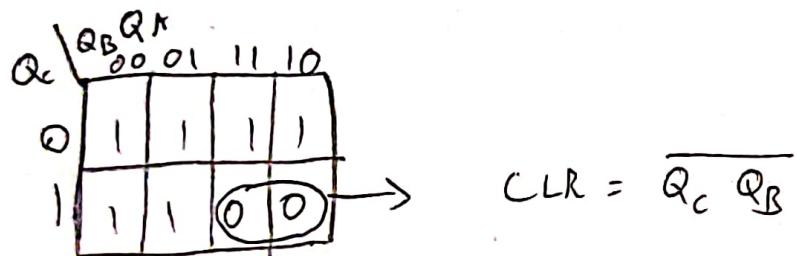
RESULT:

- a) Implemented flip flops SR, D, JK, Master slave, T using basic gates
- b) Familiarized ICs 7473 and 7474

a) Mod 6 up counter



CLK	Q_C	Q_B	Q_A	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	0	0	0	0 ← Reset



Mod 6 up counter

6. Asynchronous counters

AIM:

- (a) Design a Mod 6 up counter using JK ff
- (b) Design a Mod 8 down counter using JK ff

COMPONENTS REQUIRED

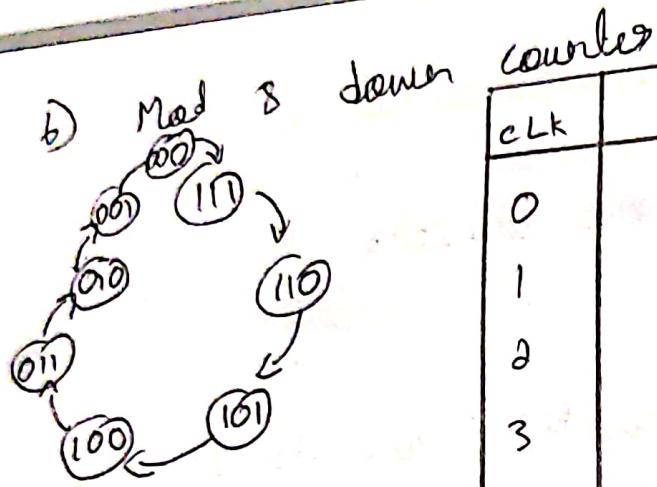
IC 7473, Patch cords, IC Trainers kit

THEORY:

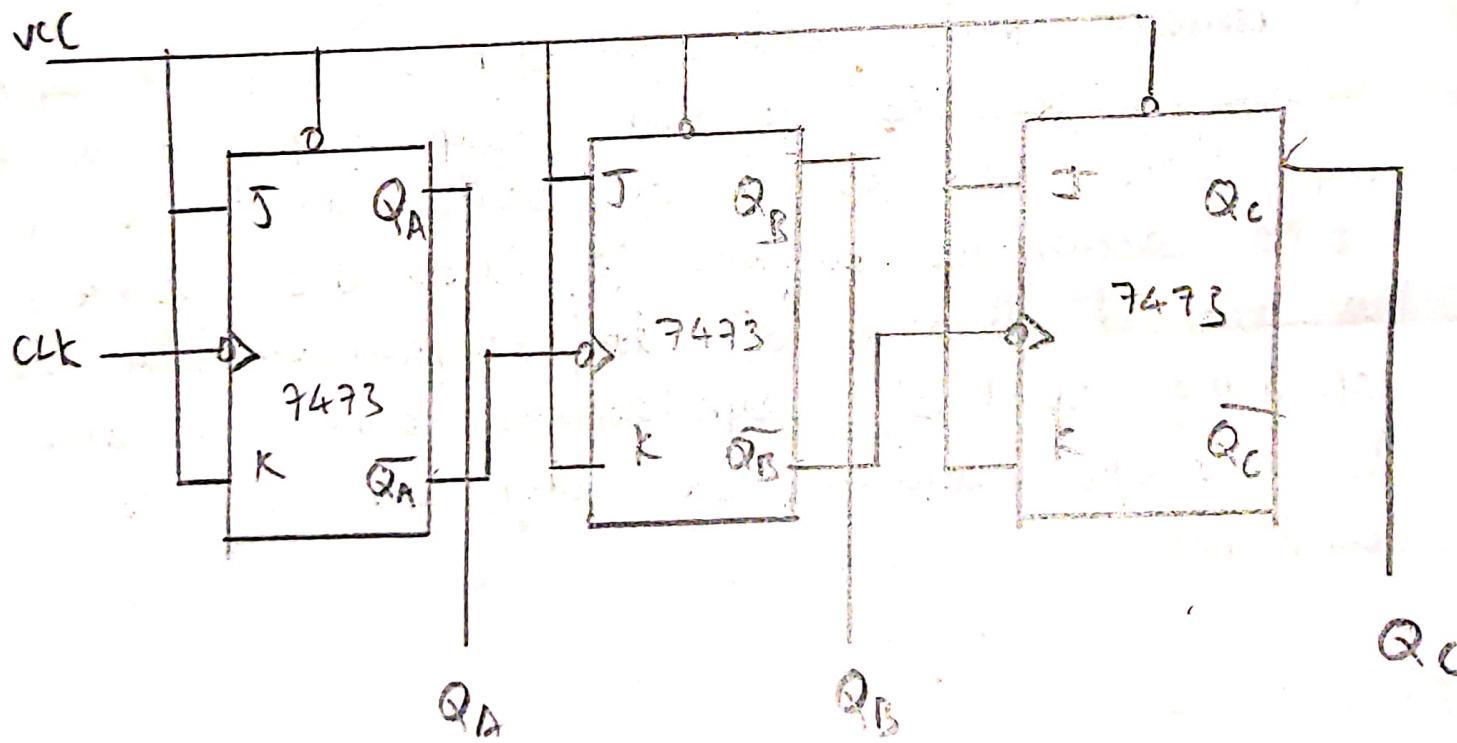
A counter which each flip-flop is triggered by the output goes to previous flip flop. As all the flip-flops do not change state simultaneously spike occurs at output. To avoid this, strobe pulse is required. Because of the propagation delay the operating speed of asynchronous counter is low. Asynchronous counter are easy and simple to construct.

PROCEDURE:

1. Check all components for their working
2. Insert the appropriate IC into the IC base
3. Make connections as shown in the circuit diagram
4. Verify truth table and observe outputs



clk	Q_A	Q_B	Q_C
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1



Mod 8 down counter

Result:

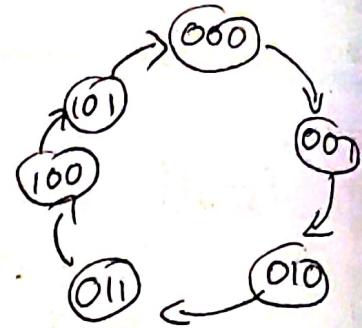
Designed Mod 6 up counter, and Mod 8 down counter

a) Mod 5 up counter

JK ff excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
0	0	0



Present state			Next state								
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	0	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

Q_C	Q_B	Q_A
0	0	0
1	0	X
1	X	X

$$J_A = \overline{Q}_C$$

Q_C	Q_B	Q_A
X	1	X
X	X	X

$$K_A = 1$$

Q_C	Q_B	Q_A
0	1	X
0	X	X

$$J_B = Q_A$$

Q_C	Q_B	Q_A
X	X	1
X	X	X

$$K_B = Q_A$$

Q_C	Q_B	Q_A
0	0	1
X	X	X

$$J_C = Q_B Q_A$$

Q_C	Q_B	Q_A
X	X	X
1	X	X

$$K_C = 1$$

7. Synchronous Counters

AIM:

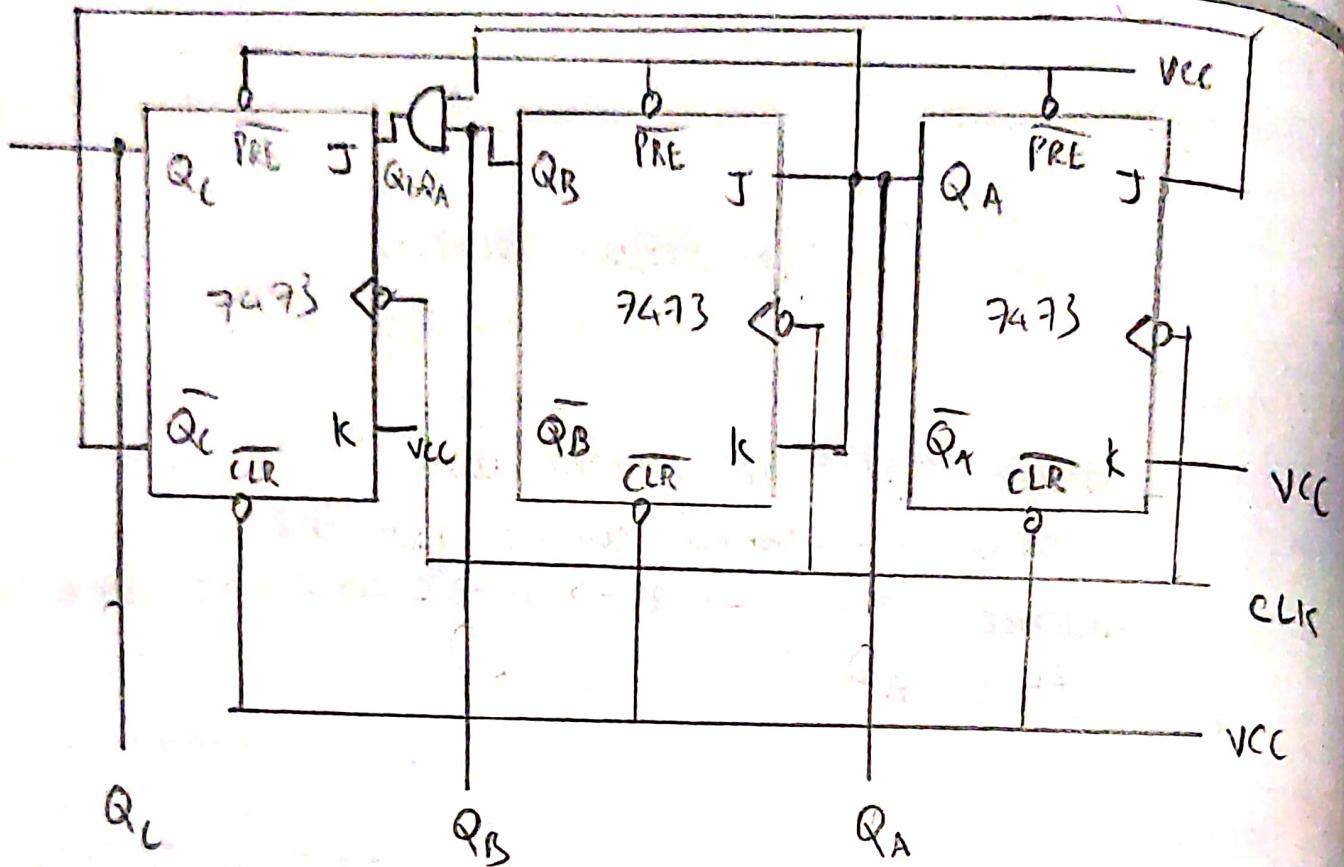
- To design Mod-5 up counter using JK ff
- To design synchronous counter for the sequence $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0$ using T ff

COMPONENTS:

IC 74193, IC Trainer, patch cords, IC 7406, IC 7432

THEORY:

A counter in which each flip flop is triggered by the output goes to previous flip flop. As all flip flop states do not change simultaneously in asynchronous counter, spike occurs at output. To avoid this strobe pulse is required. Because of propagation delay the operating speed of asynchronous counter is low. This problem can be solved by triggering all flip flops in synchronous with clock signal.

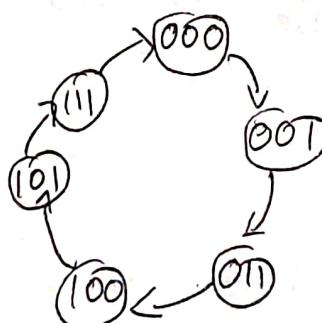


Mod 5 up counter

b) Sequence: $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$

T FF excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



Present State			Next State			T_C	T_B	T_A
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}			
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1	0
1	1	1	0	0	0	1	1	1

and such counters are called synchronous counter

PROCEDURE:

1. Check all connections and components for working
2. Insert appropriate IC into IC base
3. Make connections as shown in circuit diagram
4. Verify Truth Table and observe outputs

Q_C	$Q_B Q_A$
0	00 01 11 10
1	00 01 11 X

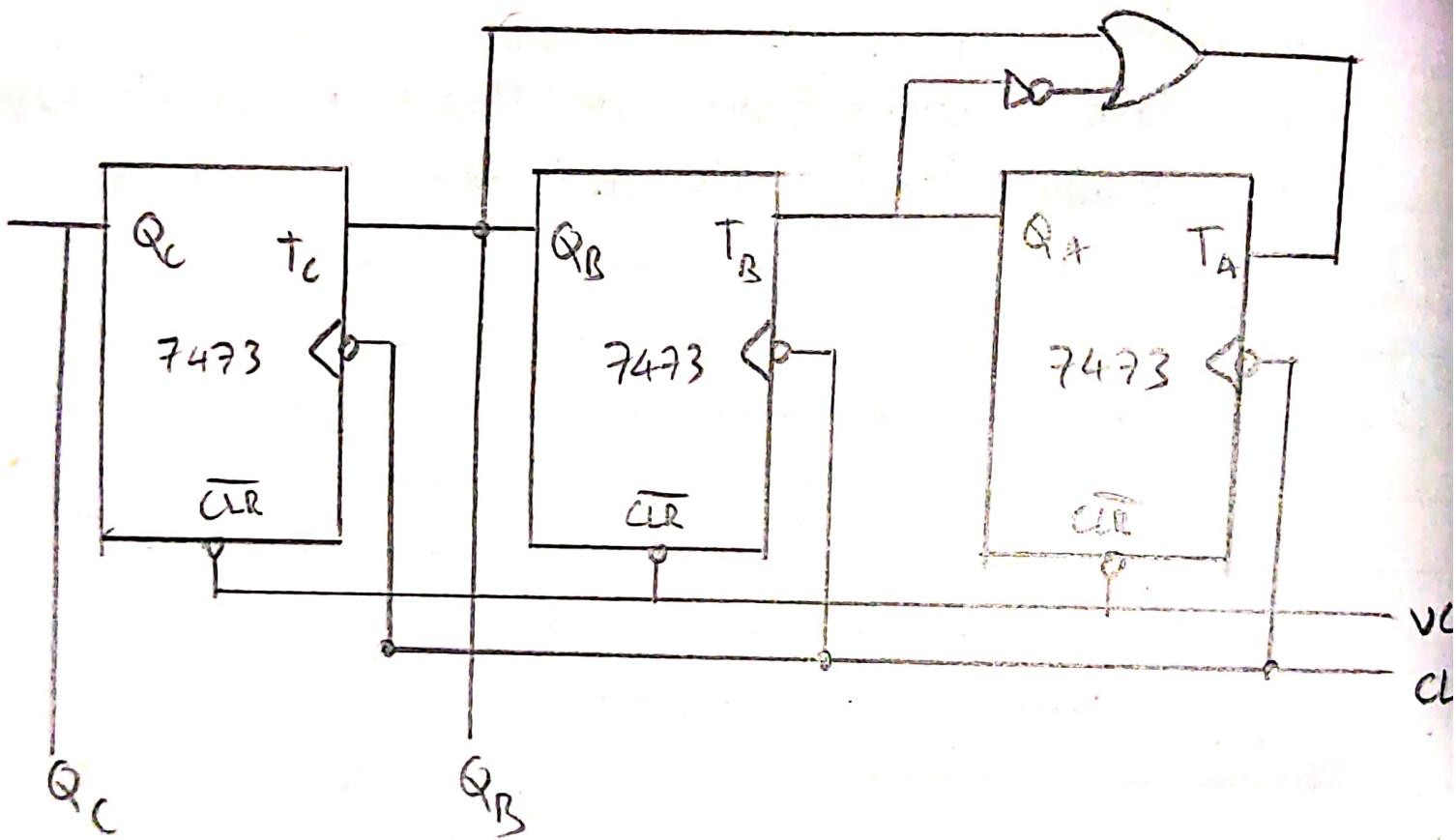
$$T_C = Q_B$$

Q_C	$Q_B Q_A$
0	01 11 X
1	11 11 X

$$T_B = Q_B$$

Q_C	$Q_B Q_A$
0	10 11 X
1	10 11 X

$$T_A = Q_A' + Q_B$$

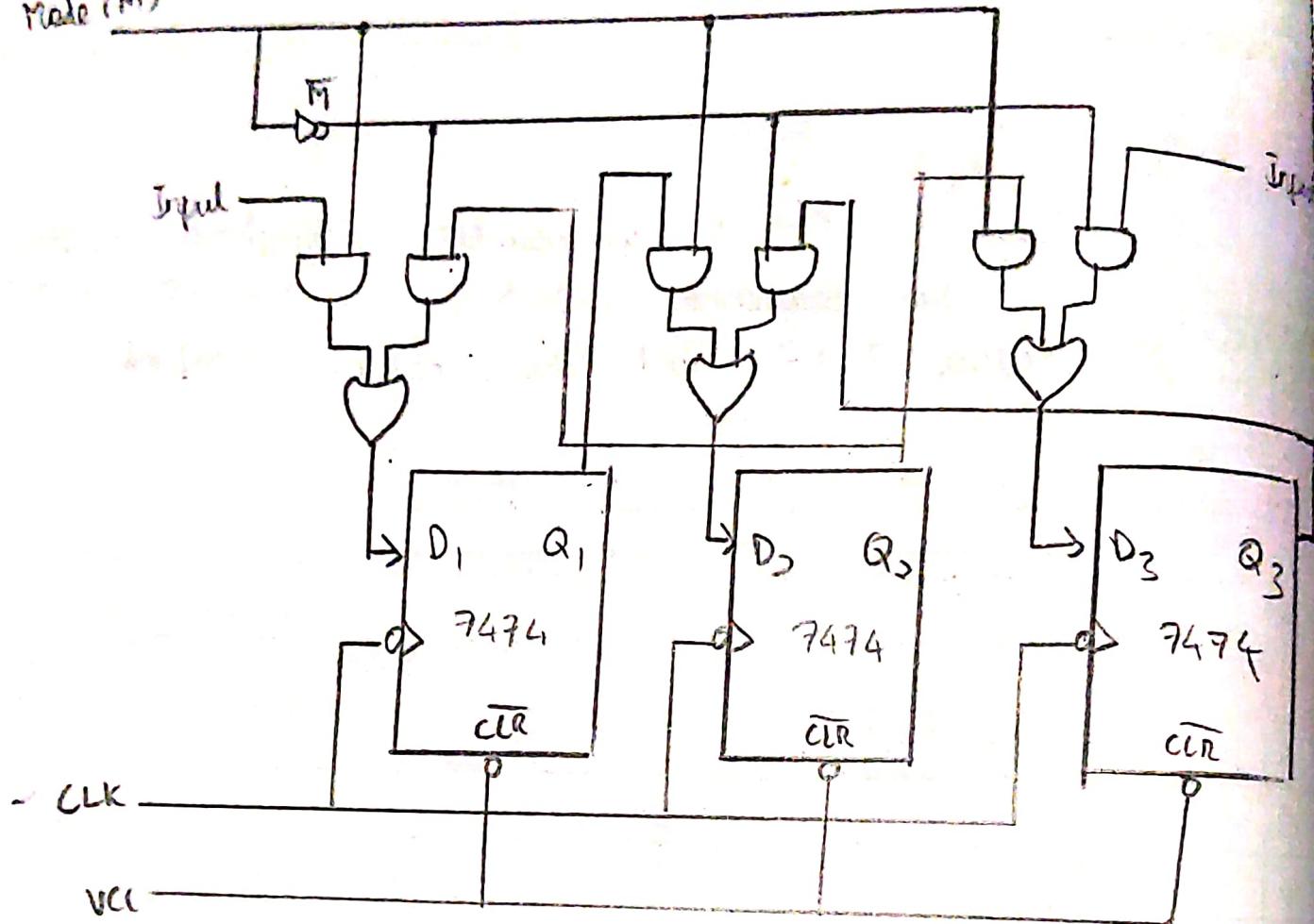


Result:

Designed Mod 5 up counter (Synchronous) using JKFF
and for sequence $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0$
using T FF and its working verified.

Mode (M)

Bi-directional shift-registers



Observations

Input	Mode	CLK	Q_1	Q_2	Q_3
1	1	0	0	0	0
1	1	1	1	0	0
1	1	2	1	1	0
1	1	3	1	1	1
0	1	4	0	1	1
0	1	5	0	0	1
0	1	6	0	0	0
1	0	1	0	0	0
1	0	2	0	0	1
1	0	3	0	1	1
1	0	4	1	1	1
0	0	5	1	1	0
0	0	6	1	0	0
0	0	7	0	0	0

8. Realization of Shift Registers

AIM:

- To realize serial input left/rush shift registers (bidirectional) using D FFs
- Ring counter and Johnson counter using D FFs

COMPONENTS:

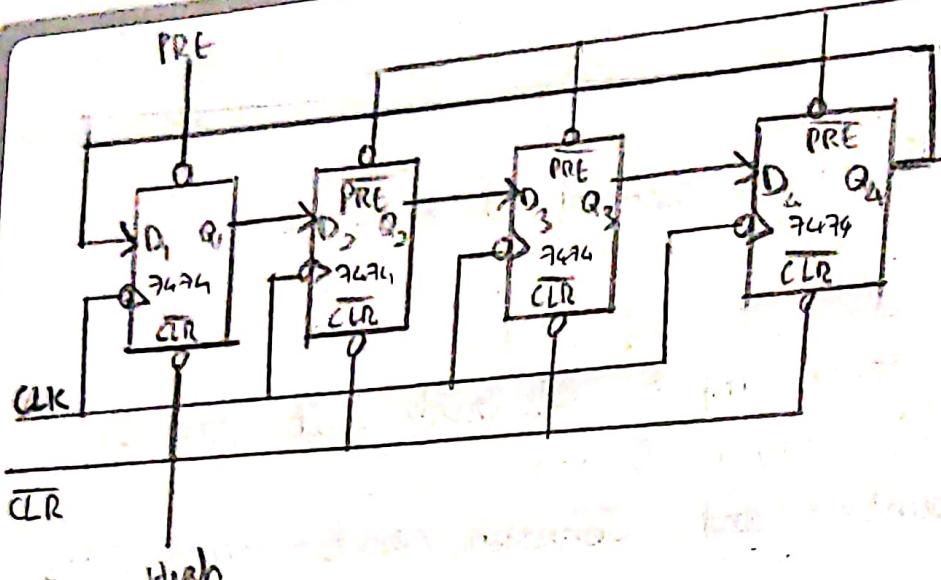
IC 7474, IC Travers, patch cords, IC 7408, IC 7432

THEORY:

- A register is a collection of flip flops. It is used to store information as multiple bits of data. The information stored in these registers can be transferred with help of shift registers.
- Shift registers store such that the bits can be moved within the register and in/out by applying clock pulse

Types:

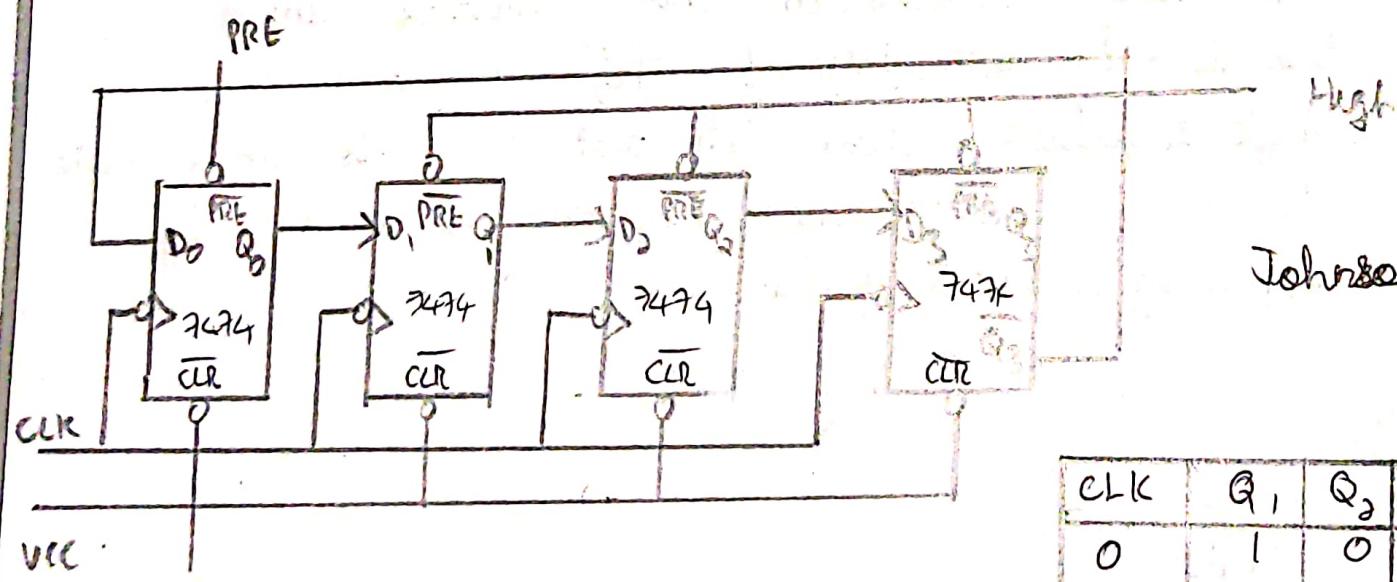
1. SISO
2. SIPO
3. PISO
4. PIPO
5. Bidirectional shift Registers



Ring counter

observation table

CLK	Q_1	Q_2	Q_3	Q_4
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0



Johnson counter

observation table

CLK	Q_1	Q_2	Q_3	Q_4
0	1	0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	0	0	0	0

→ Ring counter is a basic register with direct feedback such that the contents of the register simply circulate around the register when clock is running. Here the last output Q_7 in the shift register is connected back to serial input.

→ A basic ring counter can be slightly modified to produce Johnson counter. Here complemented last output is connected to serial input.

PROCEDURE:

1. Check all component for working
2. Insert the appropriate IC into IC base
3. Make connections as shown
4. Apply clock to pin 9 and observe output

RESULT:

Realized bidirectional shift register, ring counter and Johnson counter using D ffs