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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, **MAY 2021**

Course Code:CST202

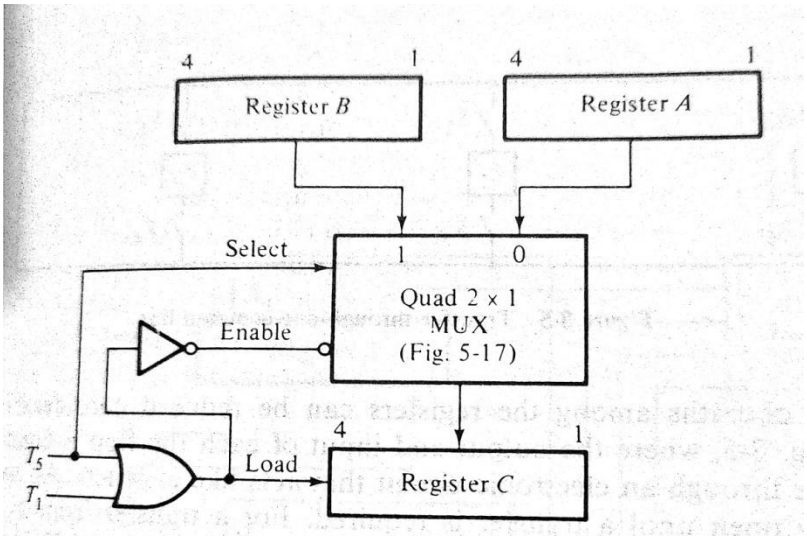
Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Explanation with example - 1.5 marks each	3
2	Instruction cycle - explanation - 3 marks	3
3	Two port memory has two address lines. Hence delay for memory access is reduced Explanation - 3 marks	3
4	Contents of A are transferred to C when timing variable T_1 occurs. Contents of B are transferred to C when timing variable T_2 occurs. A multiplexer circuit needs to be used to select between two possible paths	3



5	Flow chart - 3 marks	3
6	Explanation with example - 3 marks	3
7	Explanation with diagram - 3 marks	3
8	Explanation - 1.5 marks each	3
9	Any three types of ROM - 3 marks	3
10	Explanation - 3 marks	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11 a) 1) Arrays - indexed addressing mode 4

2) Pointers - indirect addressing mode

3) Constants - Immediate addressing mode

4) Variables - Register Mode, Absolute mode

Correct answers with example for each - 4 marks

b) *Illustrate the single bus organization of processor unit with the help of suitable diagrams.* 10

Explanation with diagram - 4 marks

Explain , listing the control signals, how the following operations are handled in this organization.

i) Transfer contents of register R5 to R1

Set output enable signal of R5 to high. This places contents of R5 on the bus. Next set input enable signal of R1 to high. This loads data from processor bus to register R1.

ii) *Move (R6), R2* (*Fetch a word from memory and move it to register R2, when the memory address is stored in register R6*)

$R6_{out}$, MAR_{in}, Read

MDR_{inE}, WMFC

MDR_{out}, $R2_{in}$

Correct answer (not necessarily in the exact form as given above) - 3 marks each

OR

12 a) Outline the differences in instruction execution during straight line sequencing and branching using suitable examples 7

Explanation with example - 3.5 marks each

b) *Differentiate between big endian and little endian byte ordering* 7

Explanation with example - 3 marks.

Consider a computer that has a byte addressable memory organized as 32 bit words. A program reads ASCII characters entered at a key board and stores them

in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name Johnson has been entered in case:
i) Big Endian Byte ordering is used

Byte contents in hex, starting at location 1000, will be 4A, 6F, 68, 6E, 73, 6F, 6E. The two words at 1000 and 1004 will be 4A6F686E and 736F6EXX.

ii) Little Endian Byte ordering is used

Byte contents in hex, starting at location 1000, will be 4A, 6F, 68, 6E, 73, 6F, 6E. The two words at 1000 and 1004 will be 6E686F4A and XX6E6F73.

Correct answer -2 marks each for big endian and little endian ordering

Module -2

13 a) *Illustrate and explain the organization of a processor unit where processor registers and ALU are connected through common buses.* 7

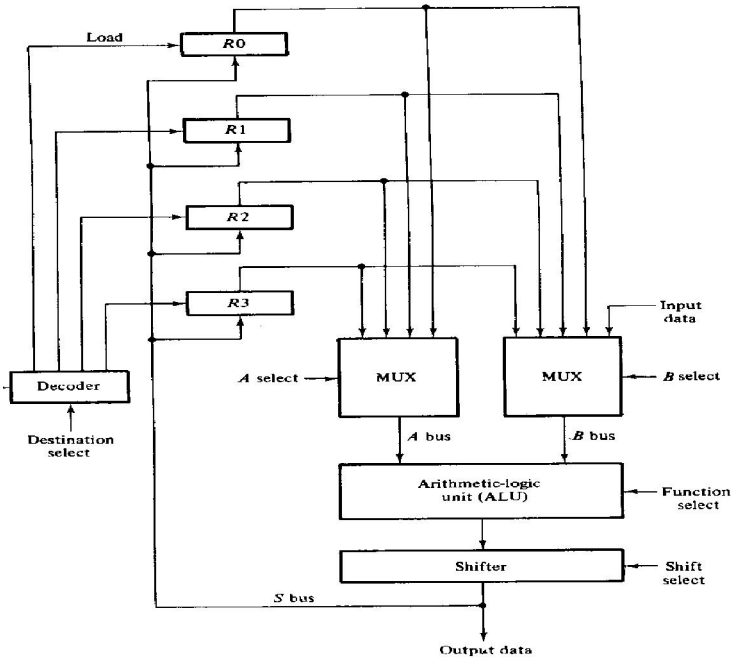


Figure 9-1 Processor registers and ALU connected through common buses

Explanation with diagram - 4 marks

Explain how the micro operation ***R2 ← R3+R4*** *would be performed using this organization, where R2, R3 and R4 are processor registers.*

- MUX A selector: Places content of R3 into Bus A.
- MUX B selector: Places content of R4 into Bus B.
- ALU function selector: Selects addition operation

- Shift selector: Selects no shift
- Decoder destination selector: Selects R2 as destination.

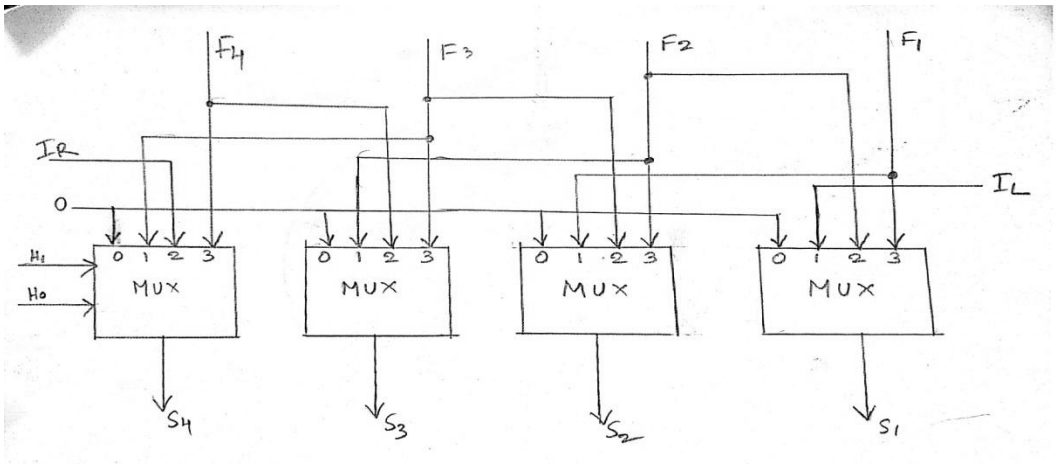
Correct answer - 3 marks

b) *Explain with the help of a block diagram the design of a 4 bit status register for an 8 bit ALU. The four status bits are C (carry), S(sign), Z(zero) and V (overflow). Clearly indicate the purpose of each status bit and how they are set or reset.* 7

Status register - Explanation with diagram - 7 marks

14 a) Design and draw a combinational logic shifter using multiplexers with two selection variables, H_1 and H_0. The operations of shifter should be as specified in the following table: 10

H_1	H_0	Operation	Function
0	0	S←0	Transfer 0's to S
0	1	S←shl F	Shift left F into S
1	0	S←shr F	Shift right F into S
1	1	S←F	No shift



Correct design and block diagram - 10 marks

If the answer is same as that of the shifter given in textbook, 5 marks can be given

b) *Describe about arithmetic, logic and shift micro operations, listing the available operations in each category.* 4

Explanation - 4 marks

Module -3

15 a) *Outline the hardware requirement for multiplying two binary numbers in sign magnitude format and specify a flowchart for same. Illustrate the algorithm, showing the contents of registers, for the multiplication of **11111** by **10101*** 8

Hardware specification and flowchart -4 marks
Correct answer with all steps - 4 marks
Answer is 1010001011

b) *Instruction pipeline* 6
Arithmetic pipeline
Processor pipeline

16 a) *Design and draw the block diagram for a 4 by 3 array multiplier.* 8

Since k=4 and j=3, we need 4x3 = 12 AND gates and two 4 bit adders to produce a product of 7 bits.

Design with block diagram - 8 marks

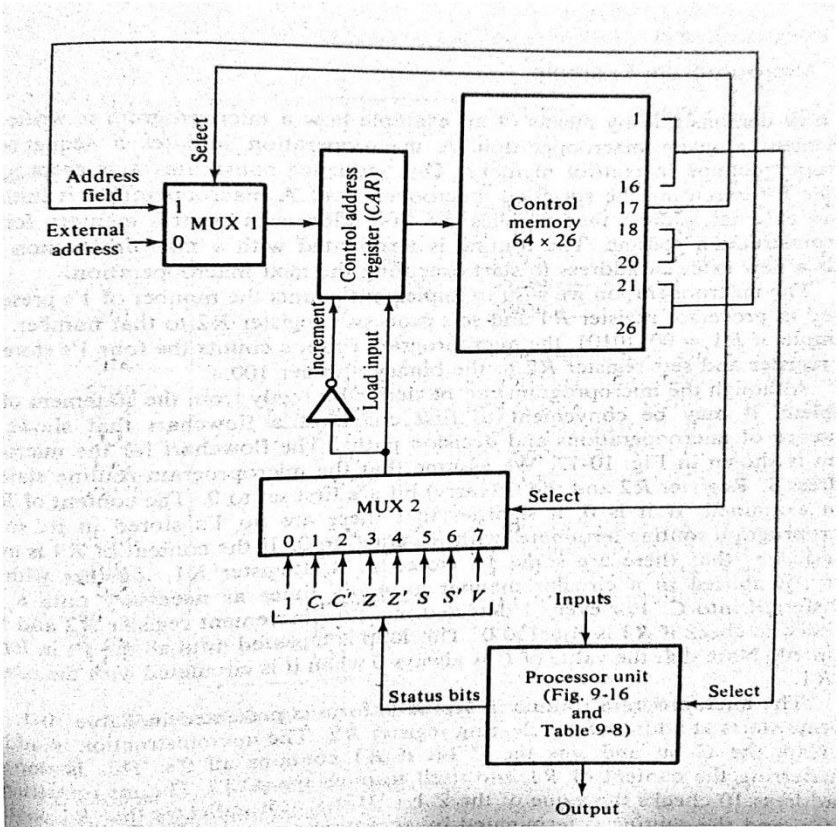
b) *Short circuiting ----2 marks* 6
Internal forwarding -4 marks

Module -4

17 a) *Illustrate the working of a micro program sequencer with the help of diagrams* 7

Explanation with diagram - 7 marks

b) *Outline with the help of a block diagram, how a micro program control unit can be used for controlling the processor unit.* 7



Explanation with block diagram - 7 marks

18 a) *Illustrate the steps for designing a micro programmed control circuit for the addition and subtraction of binary numbers in sign magnitude form. Specify the block diagram of control circuitry and the binary micro program for control memory.* 14

Algorithm/ flowchart specification - 3 marks

Hardware configuration - 4 marks

Symbolic micro program - 3 marks

Binary micro program - 4 marks

Module -5

19 a) *Explain with examples the three types of mapping functions used in cache memory* 7

Direct, Associative and Set associative mapping

Explanation with example - 7 marks

b) *What are interrupts? Outline the actions taking place in a processor once an interrupt has been raised*

Interrupts - definition - 2 mark

Interrupt service - explanation - 5 marks

20 a) *What is a DRAM? Compare the two types of DRAMs, highlighting their differences.* 7

DRAM - explanation with diagram - 2 marks

Synchronous and Asynchronous DRAMs - explanation - 2.5 marks each

b) *Outline how Direct Memory Access is implemented? Differentiate between cycle stealing DMA and burst mode DMA.*

DMA working - explanation - 3 marks

Differentiating - 2 marks each

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