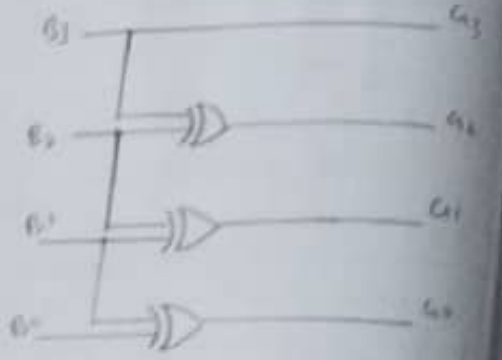
BINARY				GRAY			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

LOGIC DIAGRAM



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EXPERIMENT NO 2

BCD CONVERTERS

AIM: To design and implement binary to Gray code and BCD to Excess 3 code converters

COMPONENTS REQUIRED IC 7400, IC 7486, IC 7408, Patch cords and IC Trainer kit

THEORY

Gray code system is a binary number system in which every successive pair of numbers differ in only one bit It is used in applications in which the normal sequence of binary numbers generated by the hardware may produce an error or ambiguity during the transition from one number to the next

CONVERTING BINARY TO GRAY CODE

Let B_3 B_2 B_1 B_0 be the bits representing the binary numbers where B_0 is the LSB and B_3 is the MSB and let G_3 G_2 G_1 G_0 be the bits representing the Gray code of binary numbers where G_0 is LSB and G_3 is MSB

The truth table is shown on the left

To find the corresponding digital circuit we will use k map technique for each of the gray code bits as output with all the binary bits as input

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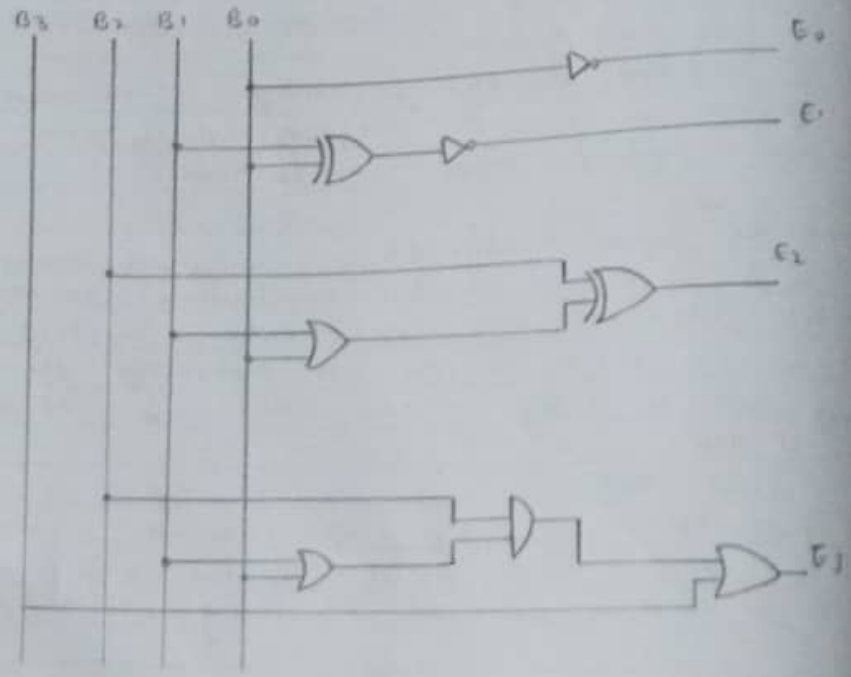
BCD (8421)	EXCESS-3
B_3 B_2 B_1 B_0	E_3 E_2 E_1 E_0
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0

LOGIC DIAGRAM



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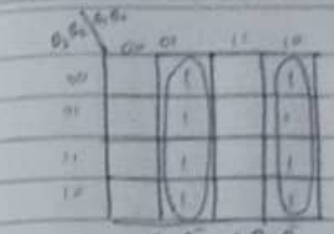
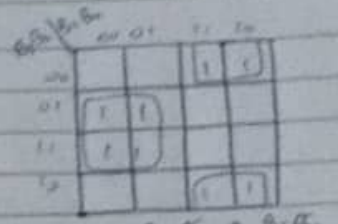
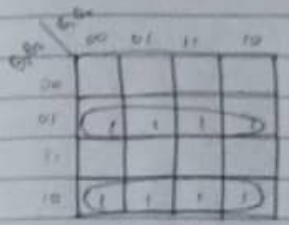


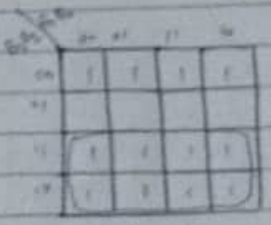
$G_0 = B_1\bar{B_0} + B_0\bar{B_1}$



$G_1 = B_2\bar{B_1} + B_1\bar{B_2}$



$G_2 = B_2\bar{B_3} + B_3\bar{B_2}$



$G_3 = B_3$

Corresponding minimized boolean expressions for gray code bits

$G_0 = B_0\bar{B_1} + B_1\bar{B_0} = B_0 \oplus B_1$

$G_1 = B_2\bar{B_1} + B_1\bar{B_2} = B_1 \oplus B_2$

$G_2 = B_2\bar{B_3} + B_3\bar{B_2} = B_2 \oplus B_3$

$G_3 = B_3$

BCD (8421) to Excess 3 code

THEORY

Excess 3 code is an unweighted self complementary BCD code. Self complimenting property means that the 1's complement of an excess 3 code number is the 9's complement of corresponding decimal number. This property is helpful since a decimal number can be 9's complimented (for subtraction) as easily as a binary

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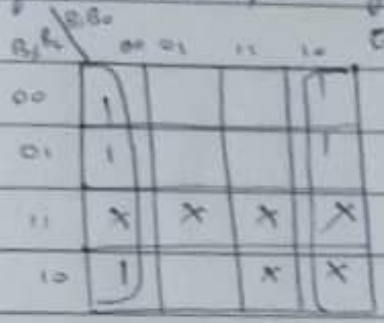
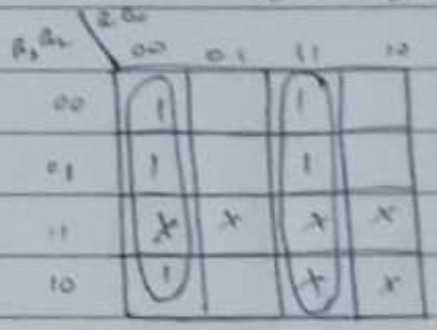
number can be one's complemented - just by inverting all bits

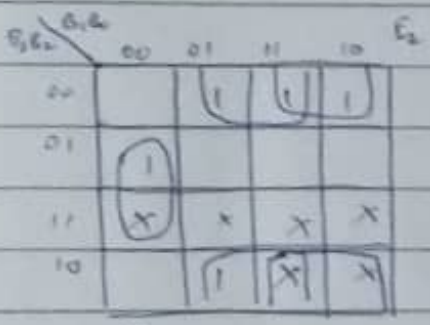
CONVERTING BCD (8421) TO EXCESS-3 CODE

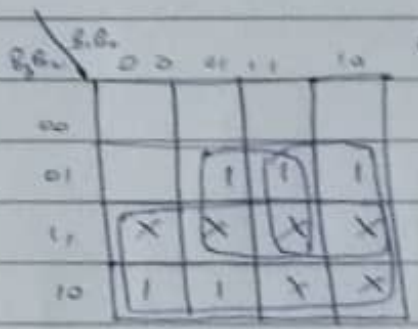
As it is clear by the name, a BCD digit can be converted to the corresponding Excess 3 code by simply adding 3 to the bit. Since we have only 10 digits (0 to 9) in decimal we don't care about the rest and mark them with a cross (X). Let B_3, B_2, B_1, B_0 be the bits representing the binary numbers where B_3 is MSB and B_0 is LSB. Let E_3, E_2, E_1, E_0 be the bits representing the excess-3 code where E_3 is MSB and E_0 is LSB. The truth table is given in the left. BCD numbers greater than 9 have been excluded (since don't care)

To find corresponding digital circuit we use









$E_0 = \bar{B_0}$

$E_1 = \bar{B_1}\bar{B_0} + B_1 B_0 = B_1 \odot B_0 = \overline{B_1 \oplus B_0}$

$E_2 = B_2\bar{B_1}\bar{B_0} + \bar{B_2}B_0 + \bar{B_2}B_1$ — De Morgan's Law

$= B_2(\overline{B_1 + B_0}) + \bar{B_2}(B_0 + B_1)$ — Distributive law

$= B_2 \oplus (B_1 + B_0)$

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$C_3 = B_3 + B_2B_0 + B_2B_1$

$= B_3 + B_2 (B_1 + B_0)$

PROCEDURE:

Check all the components for their working

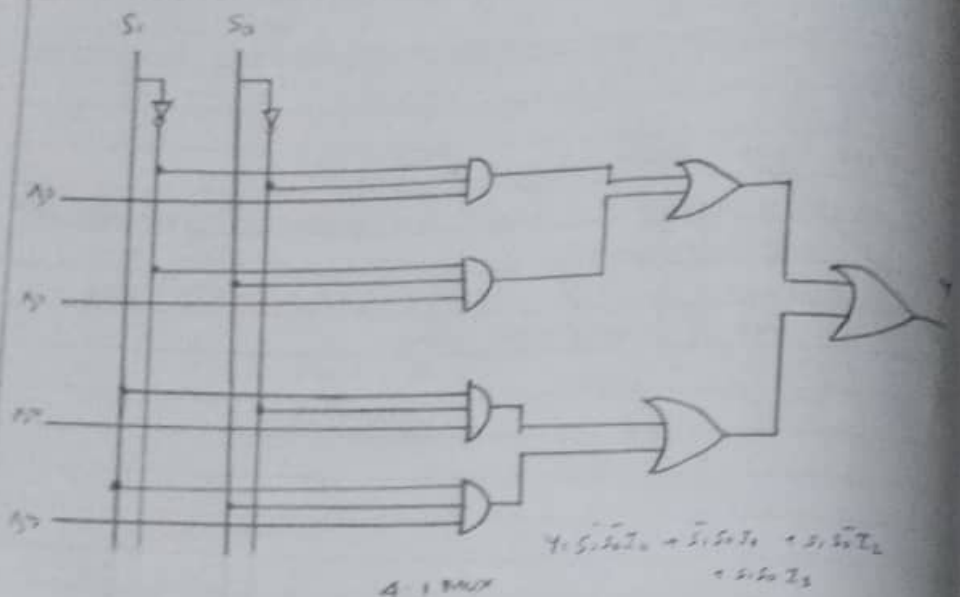
Insert the appropriate IC into the IC base.

Make connections as shown in circuit diagram.

Verify the truth table and observe the outputs

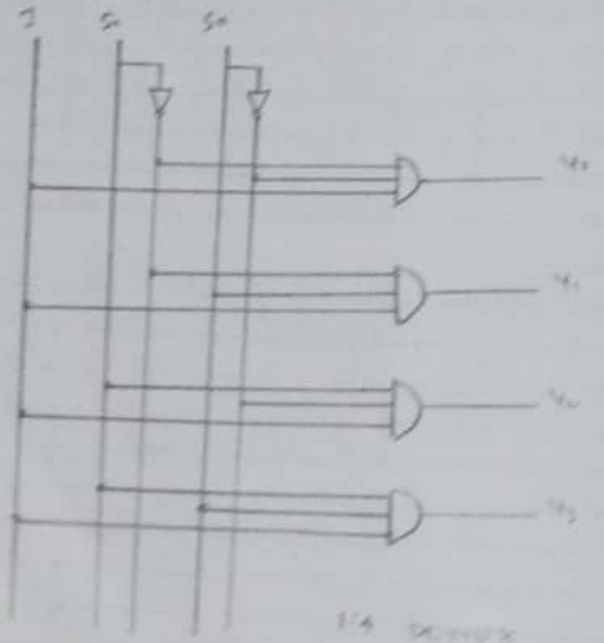
RESULT:

Binary to gray code conversion and BCD to excess-3 code conversion noticed.



$Y = S_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 S_0 I_2 + S_1 S_0 I_3$

4 : 1 MUX



1:4 DEMUX

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EXPERIMENT-4

MULTIPLEXERS AND DEMULTIPLEXERS

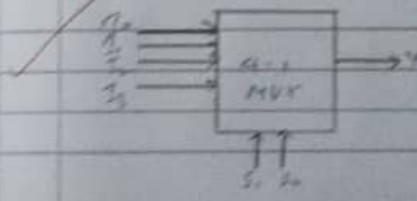
AIM: To realise multiplexers and demultiplexers using gates

COMPONENTS ACQUIRED: IC 7411, IC 7432, IC 7404, patch cords, IC trainer kit

THEORY

Multiplexers are very useful components in digital systems. They transfer a large no. of information units over a smaller no. of channels (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called data selector because the output bit depends on the circuit data bit that is selected. The general multiplexer circuit has 2^n input signals, n control / select signals and 1 output signal.

4:1 MUX



Truth Table

$\bar{E}$	S_1	S_0	Y
1	0	0	I_0
1	0	1	I_1
1	1	0	I_2
1	1	1	I_3

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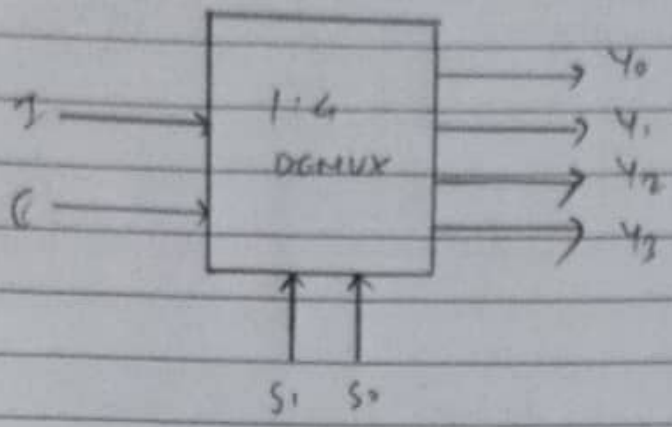
$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$

1:4 DEMUX



TRUTH TABLE

E	S_1	S_0	I	Y_0	Y_1	Y_2	Y_3
1	0	0	1	1	0	0	0
1	0	1	1	0	1	0	0
1	1	0	1	0	0	1	0
1	1	1	1	0	0	0	1
0	X	X	0	X	X	X	X

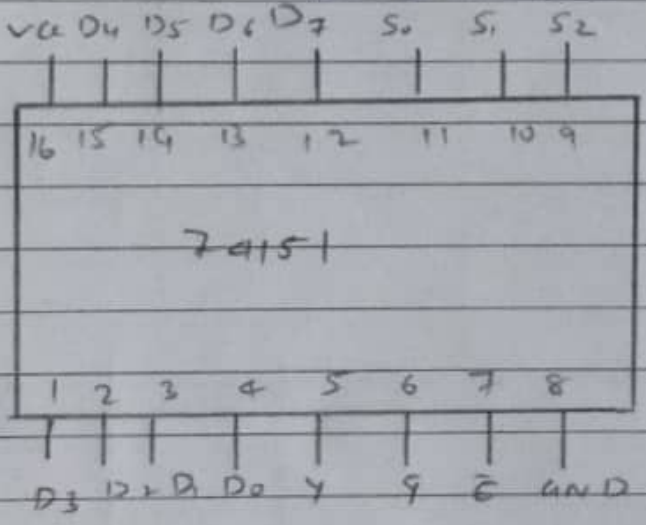
$Y_0 = \bar{S}_1 \bar{S}_0 I$

$Y_1 = \bar{S}_1 S_0 I$

$Y_2 = S_1 \bar{S}_0 I$

$Y_3 = S_1 S_0 I$

FAMILIARIZATION OF 8:1 MUX



S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

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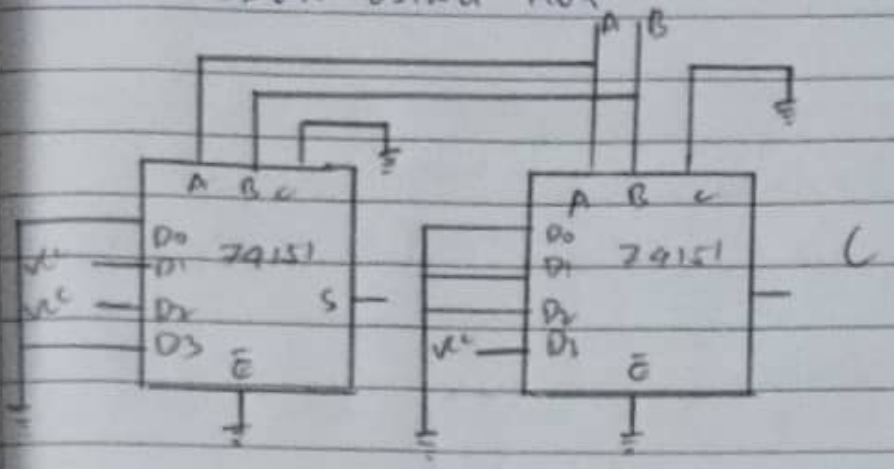
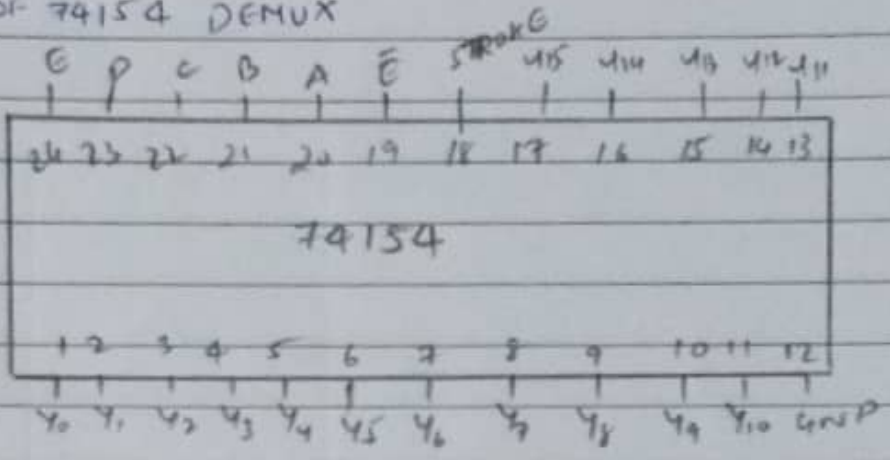
HALF ADDER USING MUX



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

REALIZATION OF 74154 DEMUX



STROBE	A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	0	1	1	0	1	1	1	1	1	1
0	0	0	1	0	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	0	1	1	1	1
0	0	1	0	0	1	1	1	1	0	1	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0

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PROCEDURE

→ Check all the components for working.
→ Insert IC and make connections as shown in the circuit diagram

RESULT:

Studied multiplexers and demultiplexers ~~Gates~~ using gates & IC

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