Cycle II

1. Flip Flops
    a. Implement Flip Flops: SR, D, T, JK and Master Slave JK Flip Flops using basic gates.
    b. Familiarization of FF ICs 7473, 7474, 7476
2. Asynchronous Counter:
    a. Design Mod 6 up counter using JK FF
    b. Design of Mod 8 down counter using JK FF
3. Synchronous Counter:
    a. Design of Mod-5 up counters using JK FF
    b. Design synchronous counter for the sequence $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0$ using T FF
4. Realization of Shift Register
    a. Serial input left/right shift register (bidirectional) using D FFs
    b. Ring counter and Johnson Counter using D FFs
5. Realization of counters using IC's (7490, 7492, 7493).