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Non-contact Electrical Measurements of Sheet Resistance and Leakage Current Density for Ultra-shallow (and other) Junctions

Vladimir N. Faifer, Michael I. Current, Wojtek Walecki, Vitali Souchkov, Georgy Mikhaylov, PhucVan, Tim Wong, Tan Nguyen, Jiansong Lu, S.H. Lau and Ann Koo

Frontier Semiconductor
1631 N. 1st Street, San Jose, CA 95112
FSM100@frontiersemi.com

Abstract

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Contact author:

Dr. Michael I. Current
Director of Technical Marketing
Frontier Semiconductor
1631 N. 1st Street, Suite 100
San Jose, CA 95112 USA
tel: 408-452-8898, ext 3731
fax: 408-452-8688
email: michaelcurrent@frontiersemi.com
net: www.frontiersemi.com

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ABSTRACT

A novel, non-contact method for determination of ultra-shallow junction sheet resistance and leakage current density has been developed based on monitoring the dynamics of photo-generated carriers by means of spatially separated capacitive probes. At light modulation frequencies of about 100 kHz, spatially resolved surface voltage signals give a direct measure of the junction sheet resistance, independent of the junction depth. At lower light modulation frequencies, the junction leakage current density is determined. Combining capacitive monitoring of modulated photo-generated free carriers with a precision wafer motion stage allows for rapid acquisition of sheet resistance and leakage data for efficient wafer-scale mapping applications.

SHALLOW JUNCTION SCALING

With gate lengths of advanced CMOS logic devices scaling to 50 nm and less, the proportional scaling of source/drain extensions over the years 2003 to 2007 calls for junction depths of 25 nm and less and sheet resistances in the range from 200 to 900 Ohm/square [1]. The continued increase in chip transistor count (heading towards 10^9 per device) has driven a strong effort to understand and constrain the sources of leakage currents and other non-functional power drains. The increased impact of short channel effects for deeply scaled CMOS transistors indicate that tight process controls (of the order of 1% or less for dose and energy) are required for source/drain extension implants in order to maintain reasonable (5% range) controls on threshold voltage and other key transistor characteristics [2, 3]. At the same time, the predominant metrology for implant process control used over the last two decades, sheet resistance measurements with 4-point probes, encounters severe challenges due to physical and electrical punch through for junctions of 50 nm and less [4]. Even with the use of "soft", non-penetrating probes, junction leakage currents continue to cause large errors in direct contact measurements due to mixing of current flows thorough the junction and into the sub-junction layers. Optical interference and reflection methods give structural information on junction depth and damage density but have limited or no sensitivity to electrical activation of shallow junction dopants and do not provide high-precision data on implant dose for implants which produce amorphous layers, such as ultra-shallow source/drain extension implants [5]. The sum of these factors point to the need for a new metrology for process control of doping process (implant and annealing) which can provide sub-1% control on implant dose for junctions of less than 30 nm and provide practical insight into conditions which lead to reduced leakage current for these ultra-shallow junctions.

PRINCIPLES OF THE MEASUREMENT

The basis of the measurement is to use photo-excitation of carriers in the junction and wafer substrate and to monitor, in a spatially resolved manner, the generation and drift of carriers with two electrodes, a transparent electrode at the center of the probe and second electrode some small distance away (Fig. 1) [6].

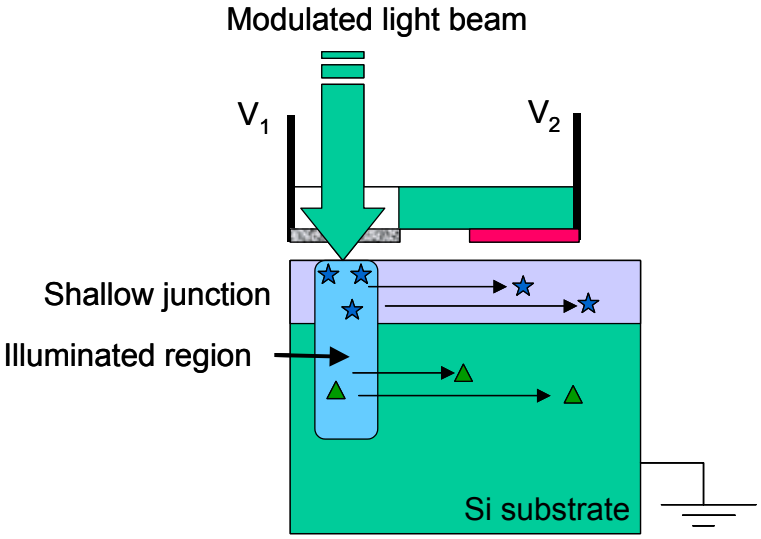

Figure 1. Sketch of the photo-excitation and drift of carriers with a modulated light source and two capacitor electrodes for monitoring the induced surface photo-voltage in a spatially resolved manner.

The analysis consists of measuring and modeling of the surface photo-voltage signals, V_1 and V_2, captured by the transparent and non-transparent electrodes when modulated light flux $\Phi(t) = \Phi_0(x,y)(1-\cos(2\pi ft))$ produces electron – hole pairs in the semiconductor material containing a surface junction, where $\Phi_0(x,y)$ is the light flux distribution at the surface of semiconductor with lateral coordinates x, y and f is a light modulating frequency [7]. The surface voltage distribution $v(x,v,t) = v_0(x,v)*\cos(2\pi ft+\varphi(x,y))$ depends mainly on drift of carriers along the surface of p-n junction. The surface voltage signals, V_1 and V_2, can be determined by the integral

$$V(t) = Const \iint_S v(x,y,t)dxdy \qquad (1)$$

The dynamics of photo-induced carrier creation, recombination and diffusion is described by the following set of continuity and Poisson's equations,

$$\frac{\partial n}{\partial t} = g_n - r_n - \nabla j_n \qquad (2)$$

$$\frac{\partial p}{\partial t} = g_p - r_p - \nabla j_p \qquad (3)$$

$$j_n = \eta_n n \nabla \psi - D_n \nabla n \qquad (4)$$

$$j_p = -\eta_p p \nabla \psi - D_p \nabla p \qquad (5)$$

$$\Delta\psi = -\frac{q}{\varepsilon\varepsilon_0}(p - n + N) \tag{6}$$

where: j_n and j_p are the electron and holes fluxes; n, μ_n, η_n, D_n, r_n, p, , μ_p, η_p, D_p , r_p are the concentration, charge and particle mobility's, diffusion coefficients and recombination rates of the electrons and holes; N is total impurity concentration in the wafer substrate; ψ is electric potential; ε_0, ε permitivity of vacuum and the semiconductor (Si);

g_n and g_p are the generation rates of electrons and holes and, for monochromatic illumination, given by:

$$g_n = g_p = \alpha\ \Phi(1 - R)\exp(-\alpha z) \tag{7}$$

where: z is the vertical spatial coordinate, measured from surface; α is the absorption coefficient; R is the reflectivity coefficient; Φ is the light flux.

Operating in the regime of low excitation levels, where vo(x,y)<<kT/q, where k is Boltzman constant, T is Kelvin temperature, q is a charge of electron, the surface voltage is proportional to the absorbed light flux. Also in the low light excitation regime, the variation of the surface charge region width, *W,* induced by illumination is smal1, which allows the use of a one dimensional Poisson equation (6) at each point. The dynamics of the photo-generated carriers are modeled with exact 2-dimensional solutions of transport equations 1 to 7, under the conditions of low light flux levels, using spatially resolved capacitive sensors sketched in Fig. 1.

For the simple case of a 1-dimensional solution, the voltage a distance, r , from the illumination point is:

$$V = A*e^{-\kappa r} \tag{8}$$

where: $\kappa = [R_S*G + i\ \omega*R_S*C_S]^{1/2}$

R_S = junction sheet resistance

G = junction conductivity

C_S = junction capacitance

$\omega = 2\pi$*light modulation frequency.

The junction conductivity, G, and leakage current density, I_o, are related by

$$G = I_o*(q/kT) \tag{9}$$

where: I_o = junction leakage amplitude

q = electron charge

k = Boltzman's constant

T = wafer temperature (K)

I = p-n junction forward bias leakage current density = I_o *$[e^{(qV/kT)} - 1]$

V = junction bias voltage.

The measurement sequence is to first analyze the amplitude and phase of the surface voltage signals under high light modulation frequencies, where the "harmonic" term, Rs*Cs, in Eq. 8 is the dominant term in the solution. This allows for a direct determination of the junction sheet resistance, Rs, independent of junction depth or leakage current effects. The analysis is then repeated for a lower light modulation frequency, where the charge decay term parameters, Rs*G, are dominant factors. Since Rs is already determined at this point, G (and I_o) can be determined directly.

MODEL SOLUTIONS

The effect of Rs on the surface voltages at various distances from the illuminated region is shown in Fig. 2. For highly conductive junctions, with low values of Rs, the value of the voltage signal in the second electrode is higher than for higher sheet resistance values.

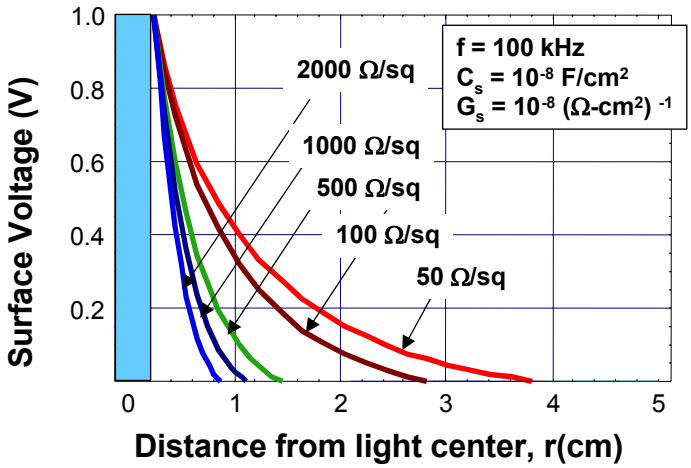

Figure 2. Effect of sheet resistance on voltage signal for 100 kHz light modulation.

The effect of junction conduction on the surface voltage ratio is stronger for low light modulation frequencies, as shown in Fig. 3.

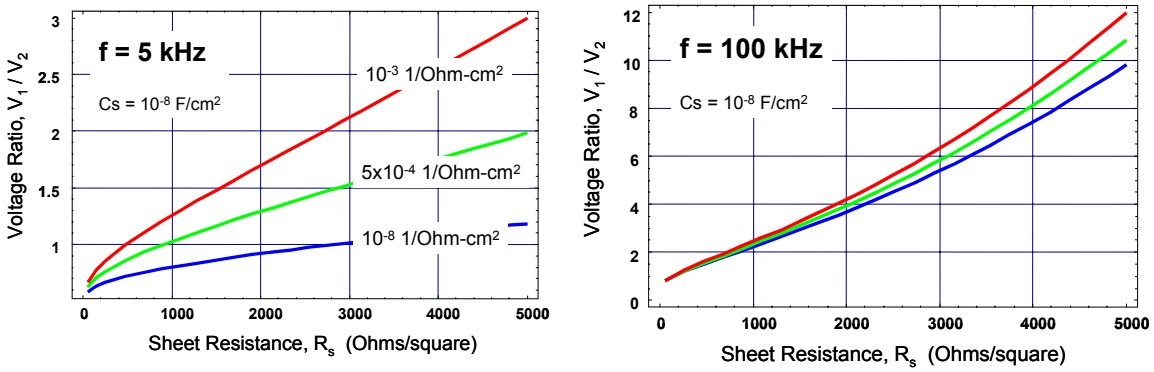

Figure 3. The effect of junction conductance on the surface voltage ratio for light modulation of frequencies 5 and 100 kHz.

REPEATABILITY

The repeatability for sheet resistance measurements is in the range of 0.05to 0.2% for well-annealed pn junctions with forward bias leakage currents less than ~10^{-3} A/cm^2. The determination of sheet resistance is independent of junction depth and leakage current for those well-annealed junctions. An example of a 30-point repeatability test for a 0.1 keV B implanted junction is shown in Fig. 4.

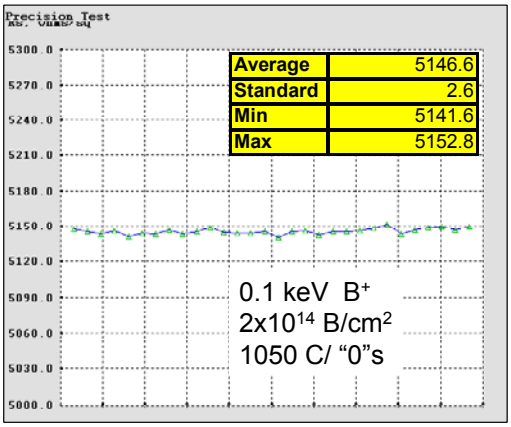

Figure 4. Repeated measurements of sheet resistance for a 0.1 keV B implanted junction annealed at 1050 C with a repeatability of ~0.05%.

MATCHING TO 4PP MEASUREMENTS FOR DEEP JUNCTIONS

Matching to 4PP measurements where the junctions are well-annealed and deep enough (generally >50 nm is sufficient) to avoid probe penetration and leakage current errors in the direct contact measurements [4] is routinely within 10%, which is consistent with 4PP tool matching without the aid of standard materials. The process range where close matching occurs for RsL and 4PP measurements has been demonstrated to extend from 5 to over 100 keV for B, P and As ions and over a dose range from 10^{13} to 5x10^{15} ions/cm^2 with anneal cycles typical of RTP "spike" and "soak" cycles (~1050 C over 1 to 10 s) resulting in a range of sheet resistance from ~100 to ~1500 Ohms/square. This corresponds to almost all implant process conditions except for the ultra-shallow junction regime.

PROCESS EVALUATIONS WITH Rs AND LEAKAGE

The addition of forward-bias leakage current density measurements to electrical activation (sheet resistance) data provides a valuable asset in rapid evaluation of implantation and annealing conditions. In the example shown in Fig. 4, an increase in anneal temperature from 800 to 1100 C results in strong reductions in sheet resistance (as expected from increased dopant activation (lower junction resistivity) and deeper junction depth).

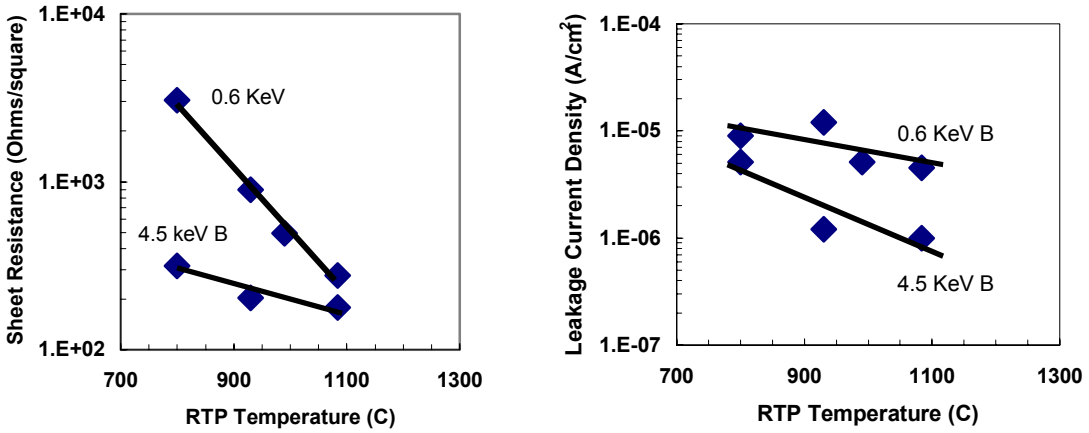

Figure 5. Sheet resistance and forward bias leakage current vs. RTP anneal temperature for low energy B implants.

The forward bias leakage current density shows a strong decrease in leakage for 4.5 keV B implants but only a modest decrease for 0.6 keV B implants for an increase in anneal temperature from 800 to 1100 C.

SUMMARY

A new photo-electrical method has been developed for non-contact evaluation of sheet resistance and leakage current for ultra-shallow junctions. The key benefit of this method is the ability to obtain separate measurements of sheet resistance and leakage current, independent of junction depth without the need for pre-measurement surface preparation. This probe has been implemented into a wafer mapping tool for evaluation of implant and annealing procedures and process controls of doping production activities.

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