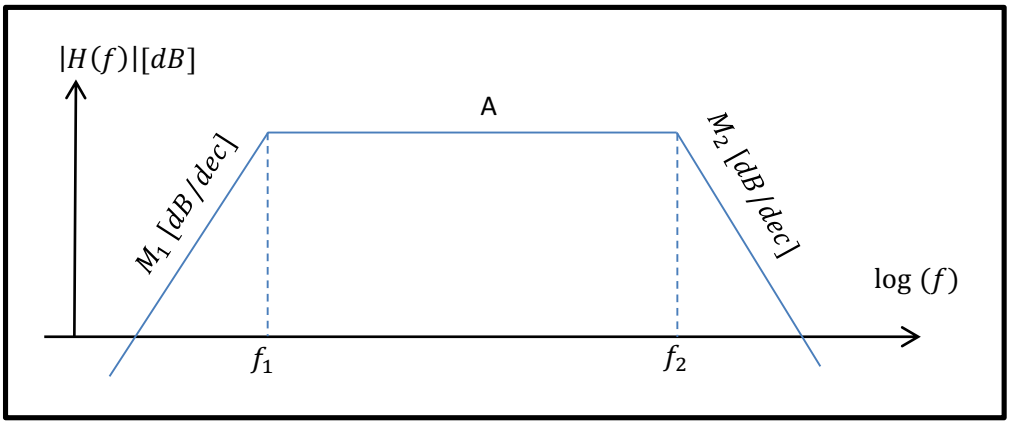
Pspice Exercise – Analog Electronic Circuits – Semester A 2017/2018

In this exercise you will design an amplifier according to a set of given requirements.

The requirements are determined using the 9 right figures of the sum of your student IDs, i.e. for two students with IDs 904357840 and 302089089 you should use 206446929 as ABCDEFGHI, and omit the 1 at the beginning. In this example A=2, C=6, H = 2 etc.

The frequency response of the amplifier is described asymptotically in the following diagram:



The parameters are as following:

- A = (35+4*D) [dB]
- $f_1 =$ (G+H+1) [KHz]
- $f_2 =$ (G+H+1)*100 [KHz]
- $M_1 = 20[\frac{dB}{dec}]$, $M_2 = -40\left[\frac{dB}{dec}\right]$ if C is odd
- $M_1 = 40[\frac{dB}{dec}]$, $M_2 = -20\left[\frac{dB}{dec}\right]$ if C is even

The amplifier should also have the following impedance characteristics:

- $R_{out} = (50 + F)[\Omega]$ if F is odd
- $R_{out} = (50 + F)[\mathrm{k}\Omega]$ if F is even
- $R_{in} = (50 + I)[\Omega]$ if I is odd
- $R_{in} = (50 + I)[\mathrm{k}\Omega]$ if I is even
- R_{in} and R_{out} values are required for $0.01 \cdot f_1 \leq f \leq 100 \cdot f_2$.

Component Selection:

- Use Pspice default BJT transistors (NPN/PNP named QbreakN and QbreakP) with $\beta = 100$.

Design Requirements:

- The sum of all resistors used may not be larger than $5[M\Omega]$.
- The sum of all capacitors used may not be larger than $1[mF]$.
- Supply voltages are $\pm 5[V]$.
- Output DC offset (DC voltage for zero input) would be $0[V] \pm 0.2[V]$.
- Required values are to be met with 5% or better accuracy.
- Use as many stages as you want.
- Total power dissipation should be lower than 0.2W.

Questions:

1. Present a table with all required transfer function values and both your IDs.
2. Present a schematic of your solution and explain stage selection, the purpose of each stage, along with small and large signal design considerations.
3. Analyze the large signal properties of the circuit and present a simulation to verify.
4. Analyze the circuit's gain for the entire frequency range under small signal assumptions. Find both knee frequencies and slopes and attach a Bode plot output simulation for the circuit.
5. Find R_{in} and R_{out} and show appropriate small signal simulations.
6. Find the total power output for the circuit and compare to simulated values.
7. Print the .out file and highlight relevant figures for calculations and requirements.

Submission Requirements:

1. The exercise should be submitted for grading by the exam date (12/2/2018), via Moodle.
2. Submission is in pairs only. Individual submission (=groups of one) may be approved by the course staff. Groups of three or more would not be approved under no circumstances.
3. Delayed submission would be approved according to university rules only (sick days, reserve duty, etc.).
4. Submission may be in Hebrew.
5. Submission includes a PDF document with answers and a folder containing all Pspice files. Pspice projects that wouldn't compile/simulate will not be graded. No handwritten submissions.
6. Please submit a single .zip file containing all files, named pspice_id1_id2.zip (i.e. pspice_904357840_302089089.zip.)