HW Set 6

Design MUX4to1 that fulfills requirements:

- Multiplexer with 4 inputs, 2 select inputs and one output.
- Use only standard CMOS cells (INV, NOR, NAND, XOR, AOI…) from gsclib090. Notice different cell sizes and topology.
- Rise/fall/delay time less than 75ps in worst case scenario.
- Use 4 similar multiplexers as load for simulation.
- Use 1.2V supply voltage.

a) Create schematic view in Virtuoso
b) Create symbol view.
c) Create test circuit and run ADE simulation. Use one input for pulse signal, all others can be DC. Find critical path – input with worst propagation delay to output and use this input for all feature measurements.
d) Measure rise/fall/delay time. Also measure rise/fall time of internal nodes on path. Did they meet the requirements? If not – tune cells sizing and measure again. Notice the extracted from Layout simulation will degrade the performance, so don't tune the circuit on the edge of requirements.
e) Create the Layout in Cadence Virtuoso.
    - Use M1 – M4 for interconnections.
    - Make the layout dense as possible. Remember area = money.
    - Input/output pins have to be on highest used metal.
f) Run LVS and DRC and pass it clean.
g) Run Quantus QRC to create extraction. (Use "Extracted simulation" file in moodle to configure the tools)
h) Run additional simulation including extracted parameters and compare to previous results.

I will release additional video tutorial to explain extracted simulation

Please include screenshots of circuit and simulation results.
Good Luck!