1. Table

Configuration		1-way	2-way	4-way	8-way	16-way
MM=512 bytes, Cache=128 bytes, Block=16 bytes	Number of sets in cache	8	4	2	1	n/a
	Number of banks in MM	32	32	32	32	32
	Number of bits for memory address	9	9	9	9	9
	Number of bits for tag	4	4	4	4	4
	Number of bits for index	3	2	1	0	n/a
	Number of bits for offset	2	3	4	5	n/a
	Number of comparisons for tag	1	2	4	8	n/a
MM=1024 bytes, Cache=128 bytes Block=16 bytes	Number of sets in cache	8	4	2	1	n/a
	Number of banks in MM	64	64	64	64	64
	Number of bits for memory address	10	10	10	10	10
	Number of bits for tag	4	4	4	4	4
	Number of bits for index	3	2	1	0	n/a
	Number of bits for offset	3	4	5	6	n/a
	Number of comparisons for tag	1	2	4	8	n/a
MM=m bytes, Cache=c bytes, Block=b bytes	Number of sets in cache	c/(b)	c/(2b)	c/(4b)	c/(8b)	c/(16b)
	Number of banks in MM	m/b	m/b	m/b	m/b	m/b
	Number of bits for memory address	Log_2m	Log_2m	Log_2m	Log_2m	Log_2m
	Number of bits for tag	log_2 b	log_2 b	log_2 b	log_2 b	log_2 b
	Number of bits for index	$log_2(c/b)$	$log_2(c/b)$ - 1	$log_2(c/b)$ - 2	$log_2(c/b)$ - 3	$log_2(c/b)$ - 4

	Number of bits for offset	$\log_2 m - \log_2 b + \log_2(c/b)$	$\log_2 m - \log_2 b + \log_2(c/b) - 1$	$\log_2 m - \log_2 b + \log_2(c/b) - 2$	$\log_2 m - \log_2 b + \log_2(c/b) - 3$	$\log_2 m - \log_2 b + \log_2(c/b) -4$
	Number of comparisons for tag	1	2	4	8	16

2. Problems 6.30 – 33

6.30

a. 128 bytes

b.

CT	CT	CT	CT	CT	CT	CT	CT	CI	CI	CI	CO	CO

6.31

a.

0	0	1	1	1	0	0	0	1	1	0	1	0

b.

Parameter	**Value**
Block offset (CO)	2
Index (C1)	6
Cache Tag (CT)	0x38
Cache hit?	Yes
Cache byte returned	0xEB

6.32

a.

1	0	1	1	0	1	1	1	0	1	0	0	0

b.

Parameter	**Value**

Block offset (CO)	0
Index (C1)	2
Cache Tag (CT)	0xB7
Cache hit?	No
Cache byte returned	0xEB

6.33

0x1788, 0x1789, 0x178A, 0x178B, 0x16C8, 0x16C9, 0x16CA, 0x16CB

3. Questions

3.1. On each memory reference, the incoming byte-address is split by the circuitry marked “0” (the high-order tag bits) and “1” (the mid-order index bits). The index bits drive the row decoders in Cache Banks 0–3 so that each bank presents the tag and data for the addressed set. Simultaneously, the tag bits are broadcast into all four tag comparators at positions 10–13, where each comparator checks (“=?”) whether its stored tag equals the incoming tag and its valid bit is set; those comparator outputs appear at 6–9 and serve as per-bank “hit” signals. On a hit in exactly one bank, that bank’s 32-bit word (buses at 2–5) is selected by the four-to-one multiplexer, whose select lines are driven by the hit signals 6–9, and the resulting output emerges at 14. Finally, the low-order offset bits (the four “offset(4)” lines) pick the desired byte out of that word. If none of the comparators asserts a hit (all signals 6–9 are zero), the logic declares a cache miss and the block must be fetched from main memory.

3.2.

3.2.1. Block size = 16 bytes

3.2.2. Set size = 64 bytes

3.2.3. Cache bank size = 256 bytes

3.2.4. Cache size = 1024 bytes

3.2.5. MM size = 4096 bytes

3.3. AAA, 3A2, 7A3, AA3, CA0, 7A4, 4A1, 5A1, CA2, 3A1, BBB, 4B5, 5B4, 6B3, 5B3, 5B5, 4B5, BBC, ABB, CBC

3.4. 5 blocks to be replaced

3.5. 13 cache misses

3.6. 7 cache hits