XILLYBUS. IP cores and design services

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# IP Core Factory — List of device files for IP core "zboard_xillybus_ip"

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## Core summary

| Name | Status | Target device family | Operating system |
|---|---|---|---|
| **zboard_xillybus_ip** ( replicate ) | | | |
| | Download | Xilinx Zynq-7000 (Zedboard) | Linux only |

Add a new core

## Device files

| Name | Direction | Data width | Expected BW | Autoset | Details |
|---|---|---|---|---|---|
| **xillybus_read_32** | | | | | |
| | Upstream (FPGA to host) | 32 bits | 128 MB/s | Yes | Data acquisition / playback (100 ms) |
| **xillybus_write_32** | | | | | |
| | Downstream (host to FPGA) | 32 bits | 128 MB/s | Yes | Data acquisition / playback (100 ms) |
| **xillybus_mem_8** | | | | | |
| | Upstream (FPGA to host) | 8 bits | 102.400 kB/s | Yes | Address/data interface (5 address bits) |
| | Downstream (host to FPGA) | 8 bits | 102.400 kB/s | Yes | Address/data interface (5 address bits) |
| **xillybus_smb** | | | | | |
| | Upstream (FPGA to host) | 8 bits | 10.240 kB/s | Yes | Command and status |
| | Downstream (host to FPGA) | 8 bits | 10.240 kB/s | Yes | Command and status |
| **xillybus_read_16_1** | | | | | |
| | Upstream (FPGA to host) | 16 bits | 16 MB/s | Yes | Short message transport |
| **xillybus_read_16_2** | | | | | |
| | Upstream (FPGA to host) | 16 bits | 16 MB/s | Yes | Short message transport |
| **xillybus_write_16_1** | | | | | |
| | Downstream (host to FPGA) | 16 bits | 16 MB/s | Yes | Short message transport |
| **xillybus_write_16_2** | | | | | |
| | Downstream (host to FPGA) | 16 bits | 16 MB/s | Yes | Short message transport |