17.4 An Ultra-Low Energy Microcontroller for Smart Dust Wireless Sensor Networks

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The rapid decreases in power consumption, size and cost along with dramatic increases in performance of communication, sensing and computation have led to the development of Smart Dust – millimeter-scale autonomous systems that form the basis of massive distributed wireless sensor networks [1]. Smart Dust motes contain digital control and processing, one or more sensors, sensor interface circuits including an ADC, wireless communication, and energy storage/power source (Fig. 17.4.1) – integrating a complete, complex system into a millimeter-scale volume. Sample applications include inventory control, smart office spaces, fingertip accelerometer virtual keyboards, defense networks that could be rapidly deployed by unmanned aerial vehicles (UAV), nodes that track the movements of birds, small animals, and even insects, and environmental networks that monitor conditions affecting crops and livestock.

Because power and energy directly relate to volume, minimizing these quantities is critical for miniaturizing wireless sensor nodes. An ultra-low energy microcontroller designed specifically for integration in Smart Dust motes is developed and consumes less than 12pJ/instruction when executing general instructions and includes special architectural features to reduce the energy consumption of common tasks.

Figure 17.4.2 shows the 16mm^3 system [2] for which the microcontroller is developed. It is composed of a micromachined corner-cube retroreflector (CCR) [3], an SOI solar cell array, an SOI micromachined capacitive accelerometer, a photosensor, an integrated oscillator, a 69pJ/bit, 1 Mbps optical receiver, a 31pJ/sample ADC [4] and a finite state machine (FSM) controller. The CCR provides passive free-space optical transmission in a one-to-many network topology at a cost of only 16pJ/bit. The FSM allows demonstration of the system components, but is replaced by the microcontroller to provide programmability and greater functionality.

The main low power architectural features [5] of the microcontroller include: highly independent subsystems that maximize the datapath sleep time; component-level clock gating performed in the decoder; processor halt mode with instantaneous oscillator power-cycling; guarded ALU inputs; multiple busses (Fig. 17.4.3); Harvard architecture to take advantage of address and data time correlation and allow separate optimization of data (8b) and instruction (17b) size; load-store RISC; no datapath pipelining because of the hardware overhead; decoder pipelining using two delayed clocks; 1 cycle per instruction operation for all instructions.

Because Smart Dust operates at relatively low sample rates and communicate infrequently with small amounts of data, the microcontroller is nominally halted and only wakes up the minimum amount of hardware to execute a task. This behavior is facilitated by a slow integrated oscillator (a few kHz) that runs continuously and operates the real time clock and five timer comparators. Two of the timers provide the sample periods for the two sensor channels. When either of the timers expires, a second main oscillator turns on at 100 kHz to drive the ADC block generating the guesses for the sequential approximation converter. Configuration registers determine the automation level of the ADC. The minimum level just powers up the sensor and precharges the ADC capacitor array before waking up the datapath, which then generates each guess, allowing other search algorithms to be explored in software. The most automated level performs a threshold comparison followed by a conversion if the threshold is exceeded, and finally stores the result in the SRAM along with a time stamp, all without invoking the datapath. A third timer invokes the transmit block, which sends the next chip (non-return to zero or Manchester encoded) of an asynchronous transmission to the CCR. During this process it automatically formats a block of memory specified by two registers into packets, allowing the processor core to specify a region of memory to be transmitted and then go to sleep. The transmit block does not require the main oscillator for most operations. The fourth timer invokes the receive block and powers up the optical receiver front end and a third 8MHz oscillator that oversamples the incoming 1Mb/s signal to extract timing. The same timer that invoked the receiver also provides the timeout signal at 1/256 of the wakeup rate. When packets with a valid CRC arrive, the receive block decodes them into one of four types: Short sync packets trigger the transmit block to fire off another chip, providing synchronous transmissions. Immediate packets contain a single instruction that is immediately fed into the instruction decoder and executed, facilitating simple remote operations such as "send your mote ID" or "send the current reading on sensor 1". Program packets are streamed directly into program memory to allow remote laser reprogramming, a critical feature for multitudes of salt grain-sized devices. Data packets stream bytes directly into data memory for manipulation by the datapath. The last timer is a software timer that wakes up the datapath.

Figure 17.4.4 shows the integrated oscillator used for the receiver and is representative of all three oscillators. It is based on a current-starved ring oscillator with a subthreshold V_t – referenced current source [6]. The oscillation frequency is adjusted from 5.6-13.7MHz by switching the ring between three and five stages and digitally trimming the current source resistor. The ring and current source can be shut down, while the state FET helps ensure that the ring powers back up in a known state and prevents the metastability that increases the time to begin oscillating. A nearly instantaneous restarting of the oscillator is achieved. The entire circuit is simulated to consume a nominal 180nW at 8MHz and 1V.

Figure 17.4.5 shows a die photo of the microcontroller core with custom 1kx8 data and 1kx17 program SRAMs that operate at 1V and are simulated to consume 0.8pJ/cycle. The core consumes 5.9μA at 1.0V and 500kHz (12 pJ/instruction) when running a test program that exercised every instruction, although on a mote it runs at 10–100kHz. Additional specifications are shown in Fig. 17.4.6.

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References:

[1] B.A. Warneke et al., "Smart Dust: Communicating with a Cubic-Millimeter Computer," *Computer Magazine*, Jan. 2001, pp. 44-51.
[2] B.A. Warneke et al., "An Autonomous 16mm^3 Solar-Powered Node for Distribute Wireless Wireless Sensor Networks," *IEEE Int'l Conf. on Sensors 2002*, Orlando, June 12-14, 2002.
[3] L. Zhou et al., "Corner-Cube Retroreflectors Based on Structure-Assisted Assembly for Free-Space Optical Communication," to be published in *IEEE JMEMS*.
[4] M.D. Scott et al., "An Ultra-Low Energy ADC for Smart Dust," *IEEE J. Solid-State Circuits*, July 2003.
[5]C. Piguet, "Low-Power and Low-Voltage CMOS Digital Design," *Microelectronic Eng*, 1997, pp. 179-208.
[6] E. Vittoz, "Micropower Techniques," *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Ed. J.E. Franca, Y. Tsividis. Prentice-Hall, 1994, pp. 77-78.

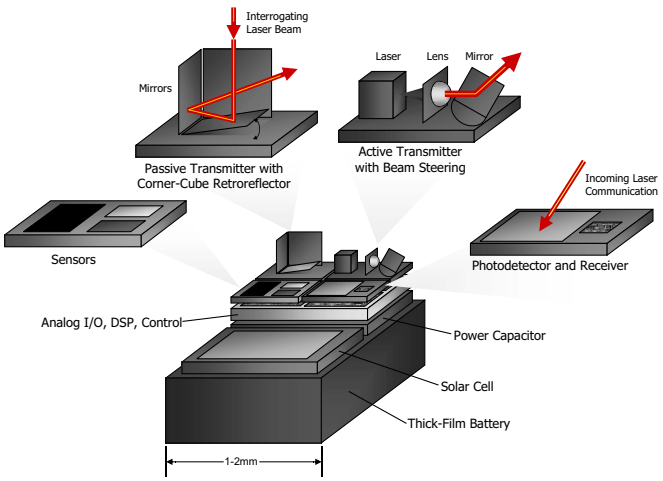


Figure 17.4.1: Smart Dust conceptual diagram.

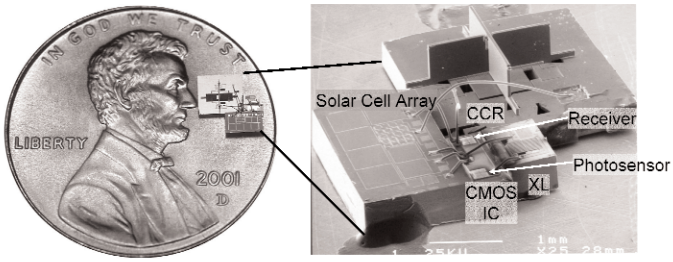


Figure 17.4.2: 16mm³ solar-powered mote with two sensors and free-space optical communication.

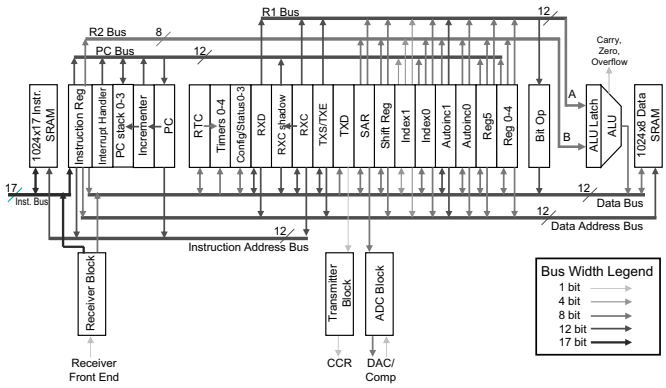


Figure 17.4.3: Microcontroller datapath showing the special registers and automation blocks.

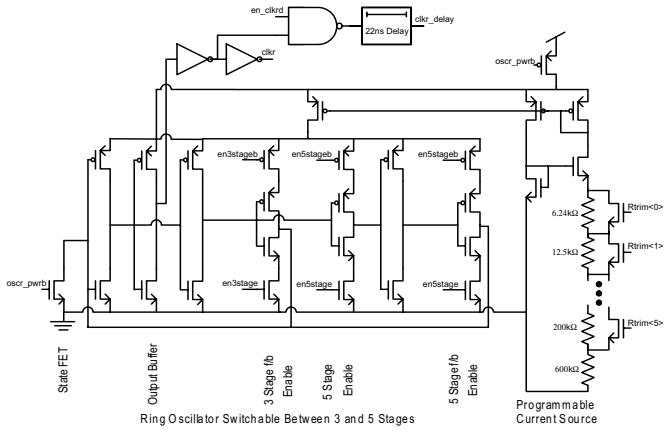


Figure 17.4.4: Digitally-trimmable integrated oscillator that consumes 160nW at 8MHz.

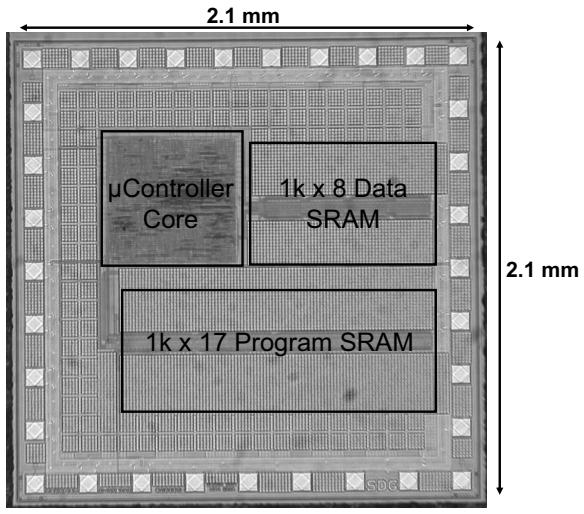
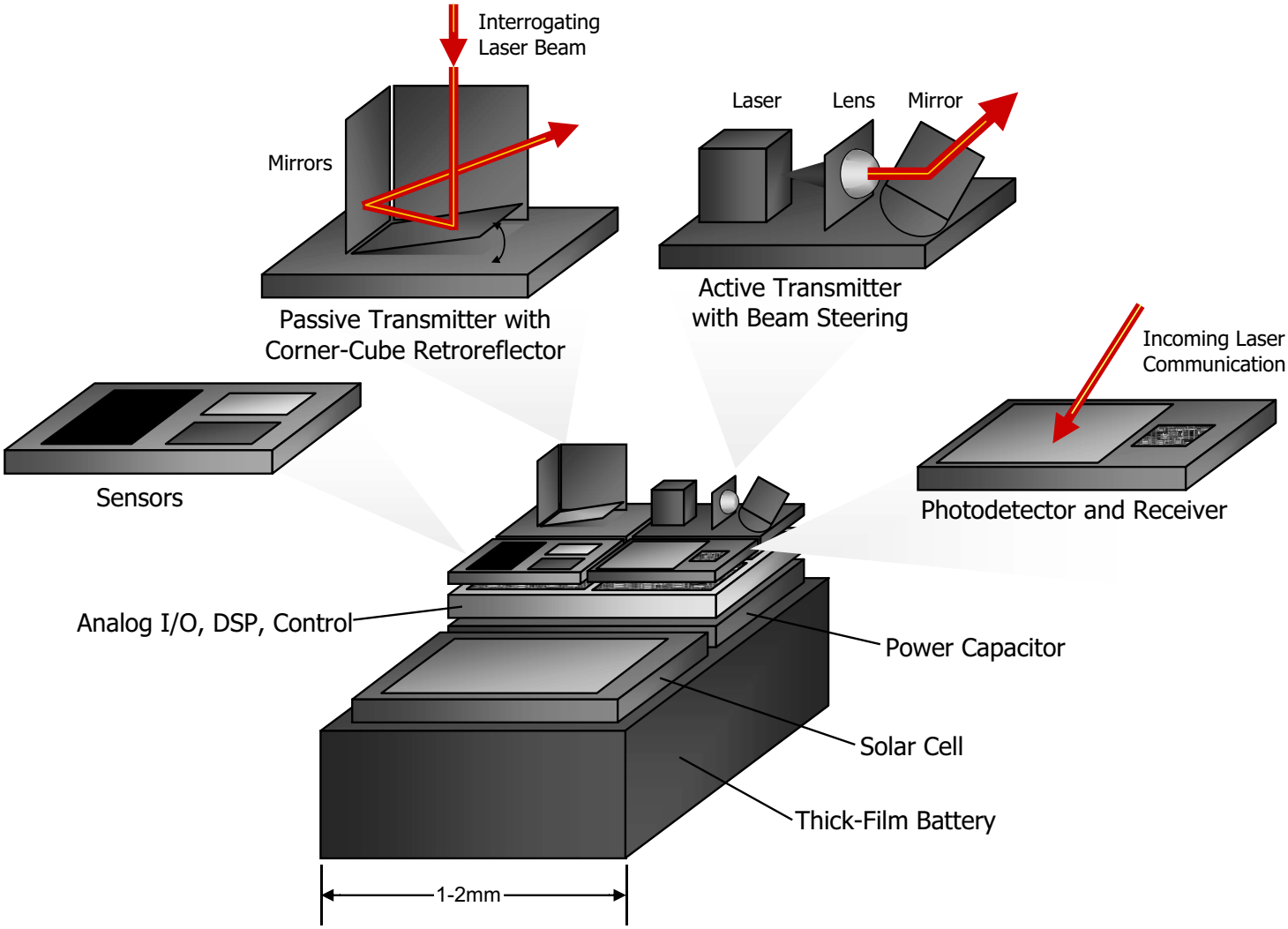


Figure 17.4.5: Die photo of microcontroller and embedded SRAM (under fill).

Core area	616 x 616 µm
Number of transistors	40,603 (214k w/ SRAM)
Gate Count	3711
Process	0.25 µm CMOS
V_t	0.55 V
V_{dd}	1.0 V
Energy Consumption	12 pJ/intruction (84,700 MIPS/W)
Leakage Current	13-20 nA

Figure 17.4.6: Chip specifications.



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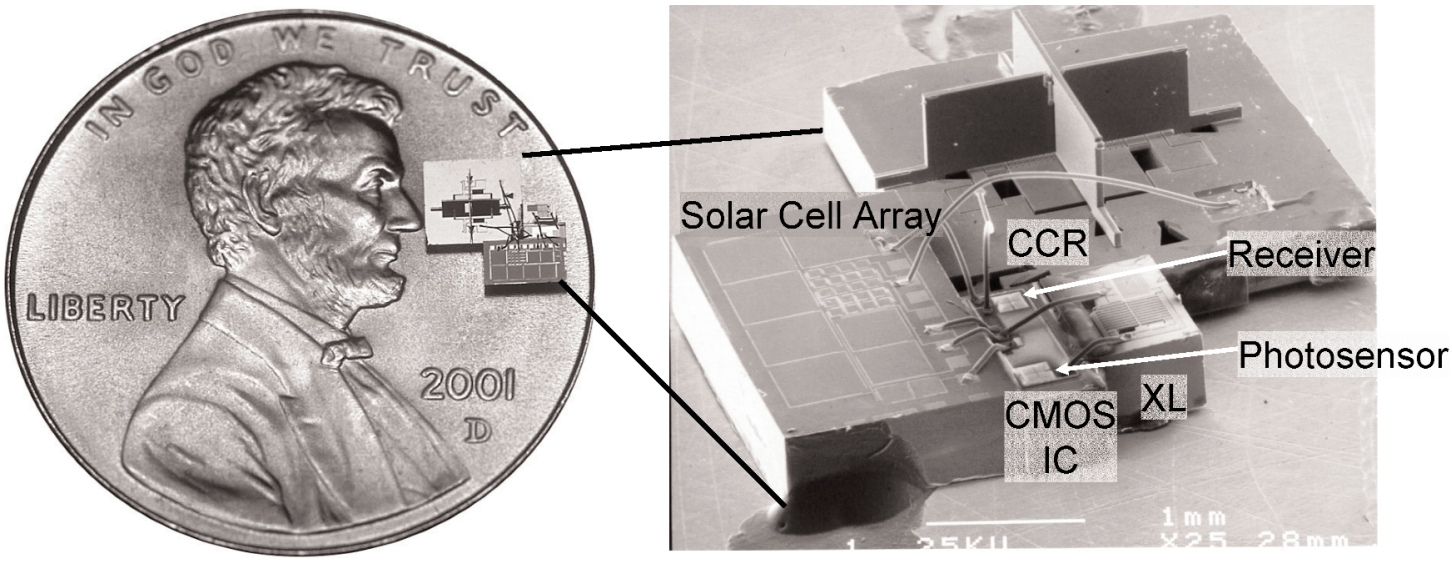

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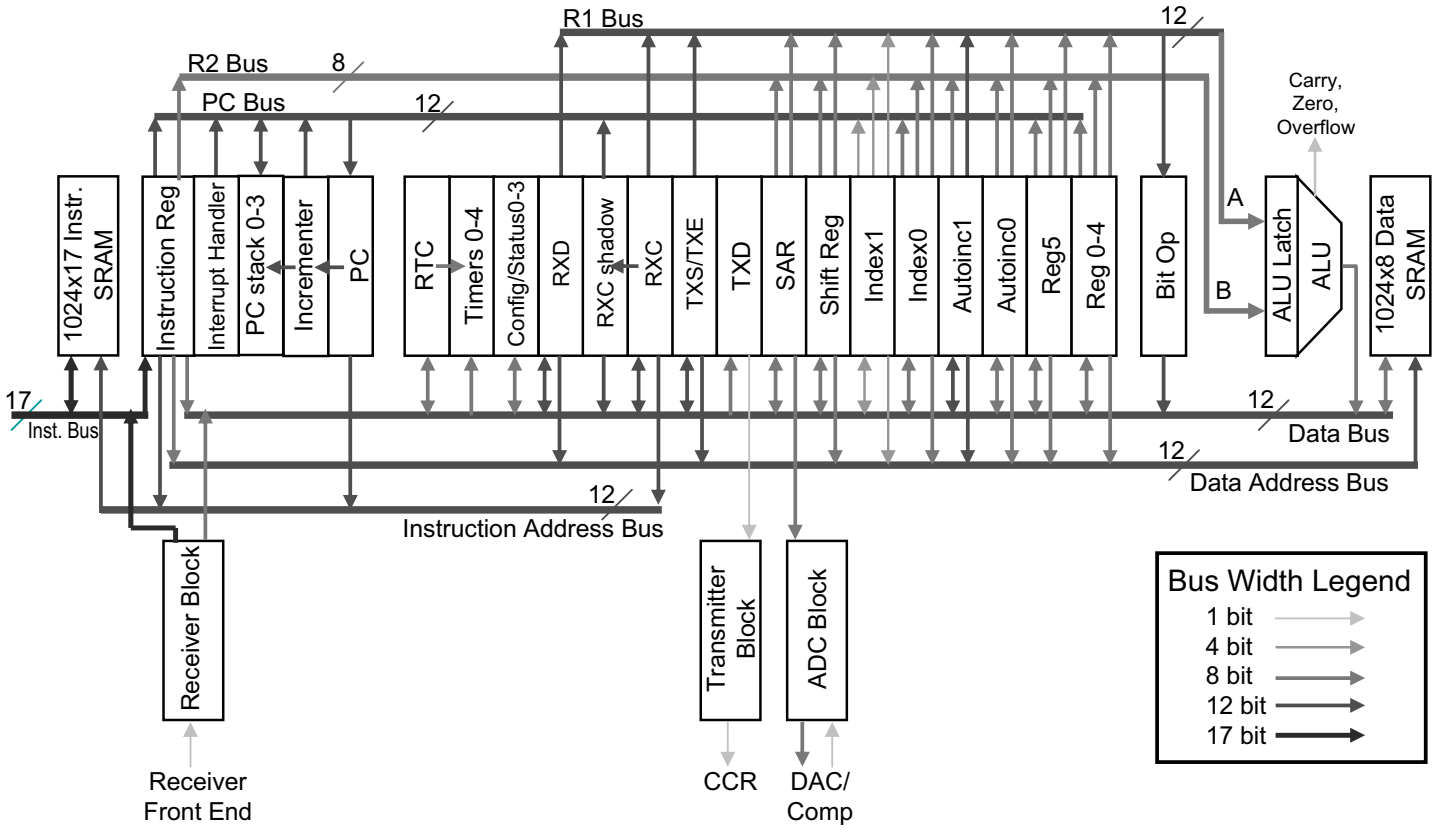

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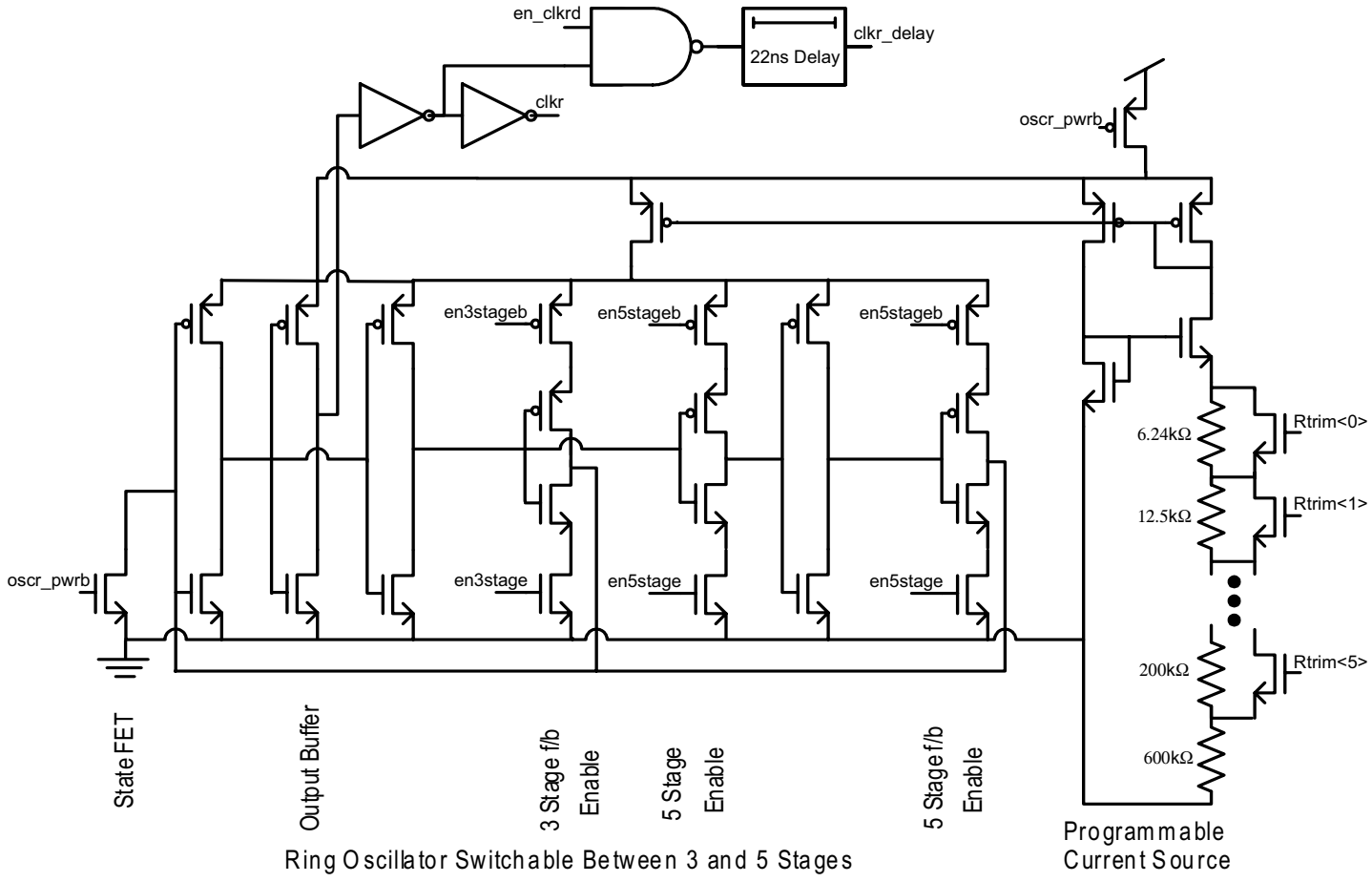

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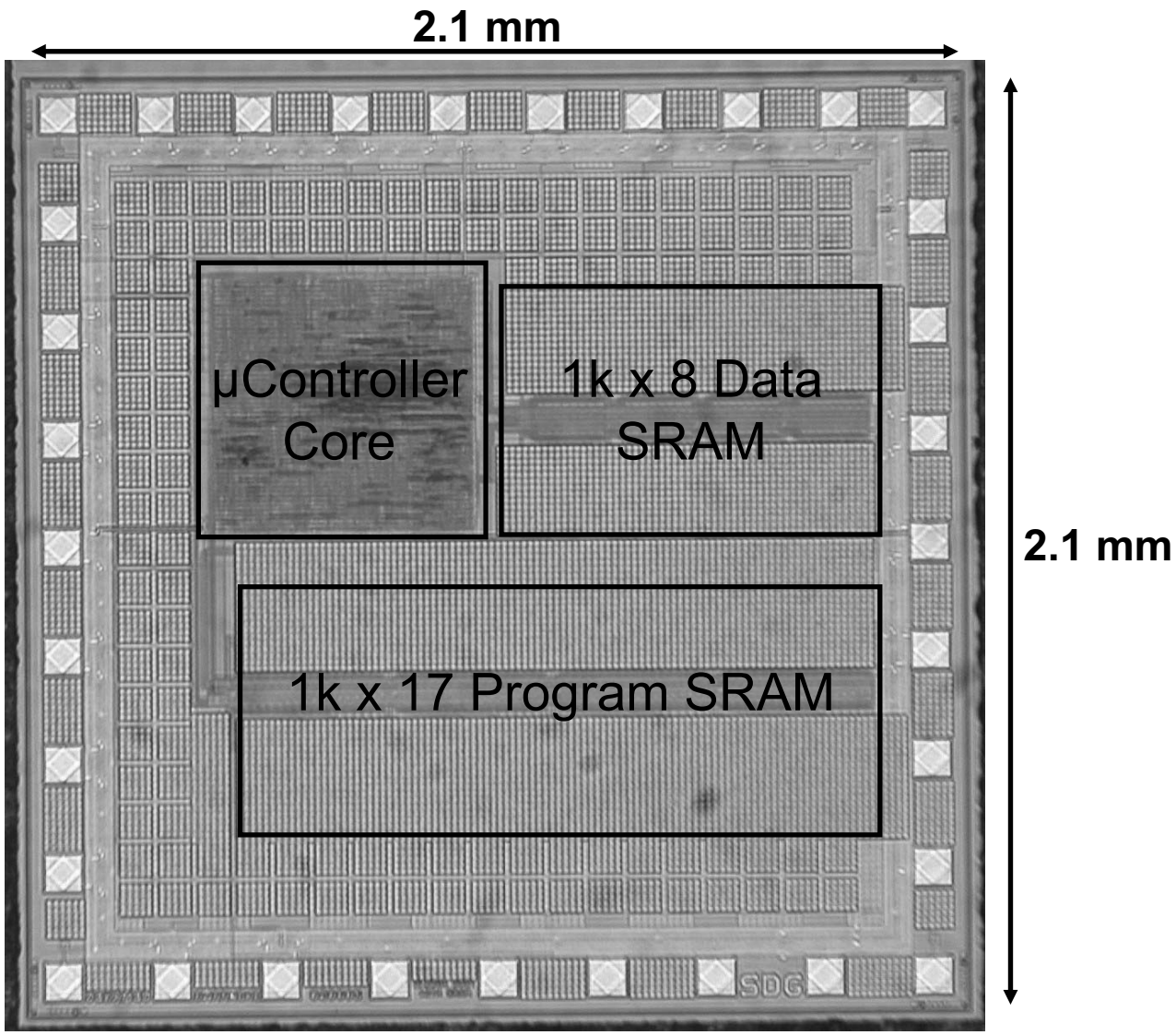

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