A Sub-2 W Low Power IA Processor for Mobile Internet Devices in 45 nm High-k Metal Gate CMOS

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***Abstract*—This paper describes a low power Intel Architecture (IA) processor specifically designed for Mobile Internet Devices (MID) with performance similar to mainstream Ultra-Mobile PCs. The design relies on high residency in a new low-power state in order to keep average power and idle power below 220 and 80 mW, respectively. The design consists of an in-order pipeline capable of issuing 2 instructions per cycle supporting 2 threads, 32 KB instruction and 24 KB data L1 caches, independent integer and floating point execution units, x86 front end execution unit, a 512 KB L2 cache and a 533 MT/s dual-mode (GTL and CMOS) front-side-bus (FSB). The design contains 47 million transistors in a die size under 25 mm^2 manufactured in a 9-metal 45 nm CMOS process with optimized transistors for low leakage. Maximum thermal design power (TDP) consumption is measured at 2 W at 1.0 V, 90 °C using a synthetic power-virus test at a frequency of 1.86 GHz.**

***Index Terms*—Low power Intel Architecture processor, mobile internet devices.**

I. Introduction

THIS paper describes a low power Intel Architecture (IA) processor specifically designed for Mobile Internet Devices (MID) with performance targeted to mainstream Ultra-Mobile PCs [1]. The design relies on high residency (over 80%) in a new low-power state in order to keep average power and idle power below a few hundred mW. The micro-Architecture is kept simple and only those features that give the best performance/watt are incorporated. The resulting processor design consists of an in-order pipeline capable of issuing 2 instructions per cycle supporting two threads, 32 KB instruction and 24 KB data L1 caches, independent integer and floating point execution units, x86 front end execution unit, a 512 KB L2 cache and a 533 MT/s dual-mode (GTL and CMOS) Front-Side-Bus (FSB). The addition of simultaneous multi-threading provide over a 36% increase in performance for a modest 19% increase in power. The design contains 47 M transistors in a die size under 25 mm^2 manufactured in a 9-metal 45 nm CMOS process with optimized transistors for low leakage packaged in a Halide-Free 441 ball, 14 $\times$ 13 mm μFCBGA. Maximum thermal design power (TDP) consumption is measured at 2 W using a synthetic power-virus test at a frequency of 1.86 GHz. A 0.65 W TDP at 800 MHz is achieved at the lowest power supply (Vmin $=$ 0.75 volts) set by the L2 cache 6-transistor bitcell under normal operating conditions; retention voltages are lower. Measured average and idle power are in the order of 220 mW and under 80 mW, respectively.

This paper is organized as follows: in Section II, the processor's micro-architectural details are presented, Section III provides a glimpse into the 45 nm CMOS technology, Section IV briefly describes the design methodology used to build this processor, Section V discusses the clock architecture, Section VI describes several low power circuit techniques used, Section VII briefly describes the L2 cache, Section VIII introduces two aspects of reducing FSB power, Section IX covers measured performance and power results and finally, in Section X, we conclude the paper.

II. Micro-Architecture

Features in this new micro-architecture are selected with low power and high performance per watt efficiency in mind. The pipeline is tailored to execute IA instructions as single atomic operations consisting of a single destination register and up to three source-registers and adheres to the Load-Op-Store instruction format. Further, using power efficient algorithms in areas such as instruction decoding and scheduling (traditionally complex circuits that are power hungry), the design achieves high performance per watt efficiency. In addition, support for Hyper-threading or simultaneous multi-threading technology (HT) is added; the instruction scheduling logic can find a pair of instructions from either the same thread or across threads in a given cycle to dispatch. HT is a feature that provides high performance per watt (typically over 36% increases in performance for a 19% increase in power) efficiency in an in-order pipeline. Moreover, the use of specialized execution units is minimized. For example, the SIMD integer multiplier and Floating Point divider are used to execute instructions that would normally require a dedicated scalar integer multiplier and integer divider respectively. Finally, other features like activity-based control of instruction issue and dispatch of operations on the FSB are added for power reduction. The processor block diagram is shown in Fig. 1; the main micro-architecture features in the front-end are: dual-decode, dual-issue, in order execution supporting simultaneous multi-threading, 32 KB instruction L1 cache with pre-decode extension, 128-entry branch trace buffer and 4 K-entry tagless Gshare predictor; this predictor uses the history of recently executed branches to predict the next one. The Floating-Point (FP) units contains 128b SIMD integer paths (2 SIMD ALUs and 1 shuffle unit), 64b FP and SIMD integer multipliers, an FP adder with 128b support for single-precision adds and a

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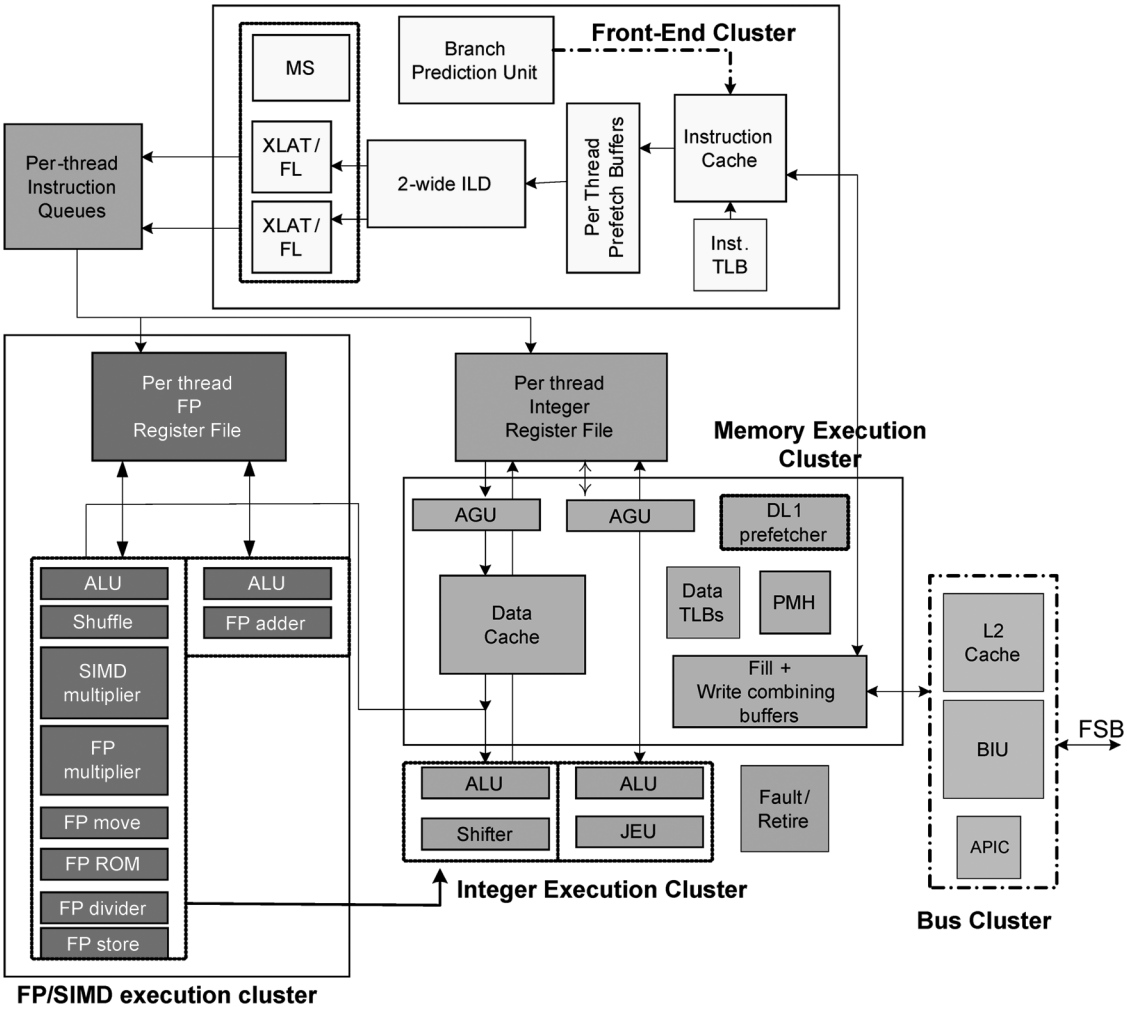

Fig. 1. Low power IA processor architecture block diagram.

Safe Instruction Recognition support to allow out-of-order commits. The integer execution cluster contains two ALUs, a shifter and a Jump Execution unit; single cycle 64b integer operations are supported. The memory execution unit contains a 24 KB write-back L1 cache with 2-level data TLB hierarchy, hardware page walker, integer store to load forwarding support, a 512 KB L2 cache with inline ECC and L2/data cache hardware pre-fetchers. Other micro-architecture features include Intel 64 Architecture support, Intel Digital Media Boost (SSE3), and Intel Virtualization technology. A detailed look at the micro-architecture can be found in [5] and [6].

Fig. 2 shows the 16-stage pipeline starting with instruction fetch of an integer macro-instruction through when the results are either committed to the register file or the data cache. The included processor shmoo (thousands of functional patterns are used) clearly show that a 2 GHz core frequency at 1 V is clearly achievable. Also note that lower frequencies (down to 600 MHz) are possible at a power supply of 0.75 V by simply dialing down the core phase-lock loop (PLL) ratio.

Several features support extended battery life including the new Intel Deep Power Down Technology [3] which allows for a majority of the CPU functionality to be powered down except for an on-die array that holds the micro-architectural state with very fast entry/exit times ($< 100\ \mu$s). Fig. 3 shows several power states (C-states) where lower power is achieved as more features are turned off from C-0 state to C-6 state. In C-0 high frequency mode (HFM) and low frequency mode (LFM), the processor can operate at its maximum frequency and its minimum frequency, respectively. In C-1 power state the core clock is power-gated and the L1 caches flushed resulting in lower dynamic power; exit latency is under 1 μs. In C-4 power state, the 2 PLLs are shut down, the L1 caches are flushed leading to further dynamic power reduction; exit latencies are in the order of 30 μs. Finally, in C-6 power state, the state of the machine is stored in an on-die SRAM (built as a 1-read, 1-write ported register file) and the core power supply is shut down resulting in the lowest power; exit latencies are in the order of 100 μs. Fig. 4 shows the power savings among all these C-states; the AVERAGE power is clearly a function of the processor's residency in these C-states; based on preliminary measurements, we estimate C-6 residency to be between 80% and 90% leading to an AVERAGE power in the order of 220 mW. IDLE power which is dominated by leakage power of the remaining powered functional units on die is below 80 mW.

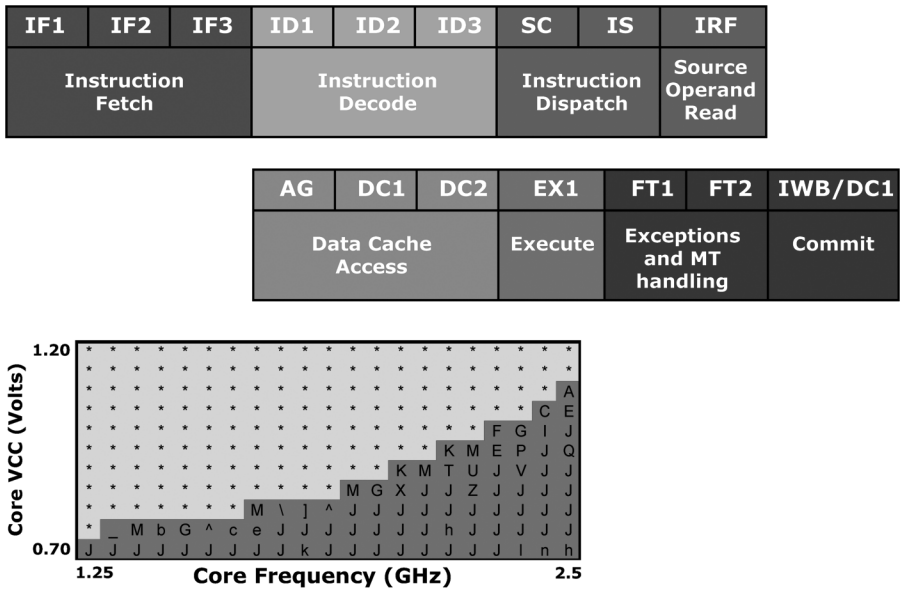

Fig. 2. 16 stage processor pipeline; processor shmoo at 90 °C shows that this pipeline is capable of operating at 2 GHz and 1 volt.

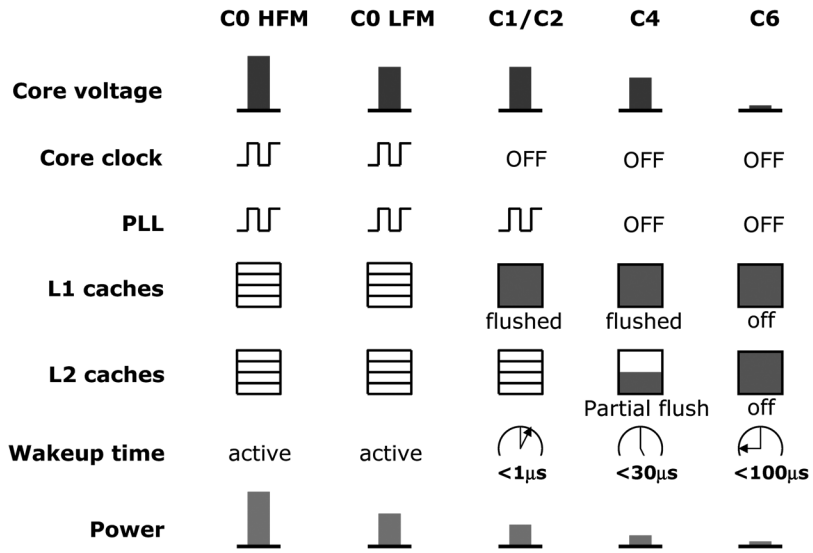

Fig. 3. Processor power C-states; C-6 residency can be as high as 80–90%.

III. CMOS Technology

This microprocessor is implemented in 45 nm CMOS technology [2] containing metal gate high-k dielectric transistors. Due to the aggressive sub-100 mW IDLE power goal, a lower leakage transistor is used where the appropriate transistor gain vs. transistor leakage has been optimized to produce a 2 GHz pipeline. In addition, nine layers of metal are used along with a very aggressive 6-transistor cache bitcell which uses local interconnect layers. Fig. 5 shows a transmission electron microscopy cross-section of the metal-gate high-k transistor and the resulting 25X to 1000X reduction in gate leakage compared to Intel's previous 65 nm CMOS technology.

IV. Design Methodology

This design uses a "sea-of-Functional-Unit-Blocks (FUB)" methodology whereby all cluster hierarchies as well as all unit-level hierarchies are flattened at the chip-level even though the logical partitioning of the chip-level RTL model is comprised of several logical clusters (Floating Point, Integer Execution, Memory Execution, Front-End, Bus Interface, and L2 Cache). A "sea-of-FUBs" methodology allowed the design to converge physically (layout, timing, noise and reliability verification) at a much faster pace since the chip was built with physical, timing, and noise abstracts; the design could be iterated more than once per week. This methodology essentially removes all logical clusters and unit-level hierarchical boundaries resulting in a physical hierarchy where an object-based parallel editing scheme is used for physical design convergence; Fig. 6 shows the die photo with the logical unit partitions. The physical database consists of 205 unique FUBs (not including repeater stations) and 41,000 FUB-to-FUB interconnects. 91% of the FUBs are designed using cell-based design techniques using

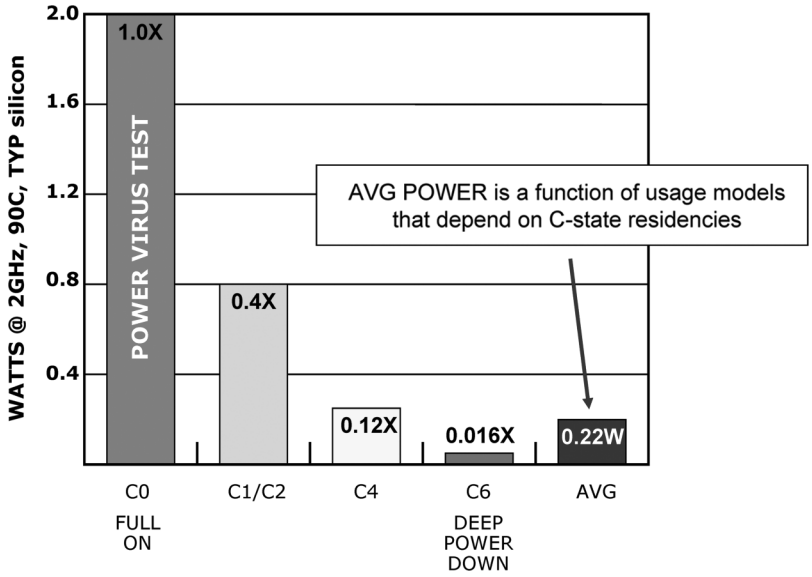

Fig. 4. Power reduction as a function of C-state; average power is a function of these C-state residencies.

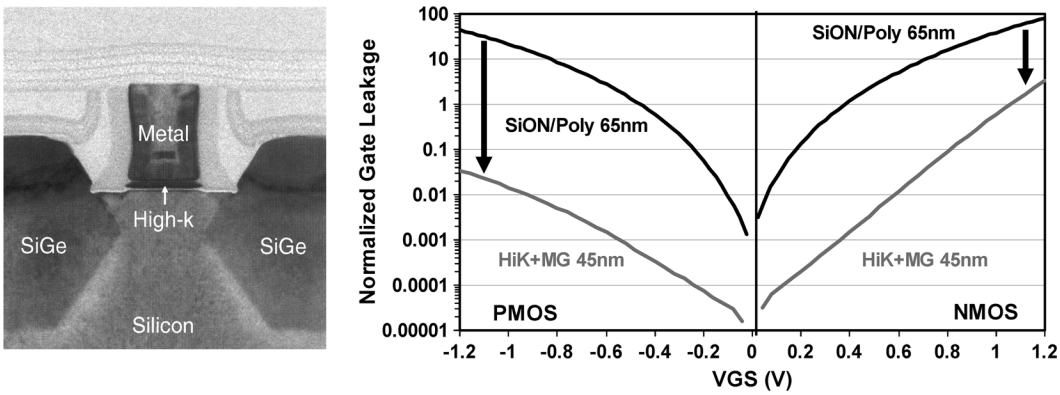

Fig. 5. Metal-gate 45 nm transistor cross section and transistor gate leakage reduction compared to 65 nm CMOS.

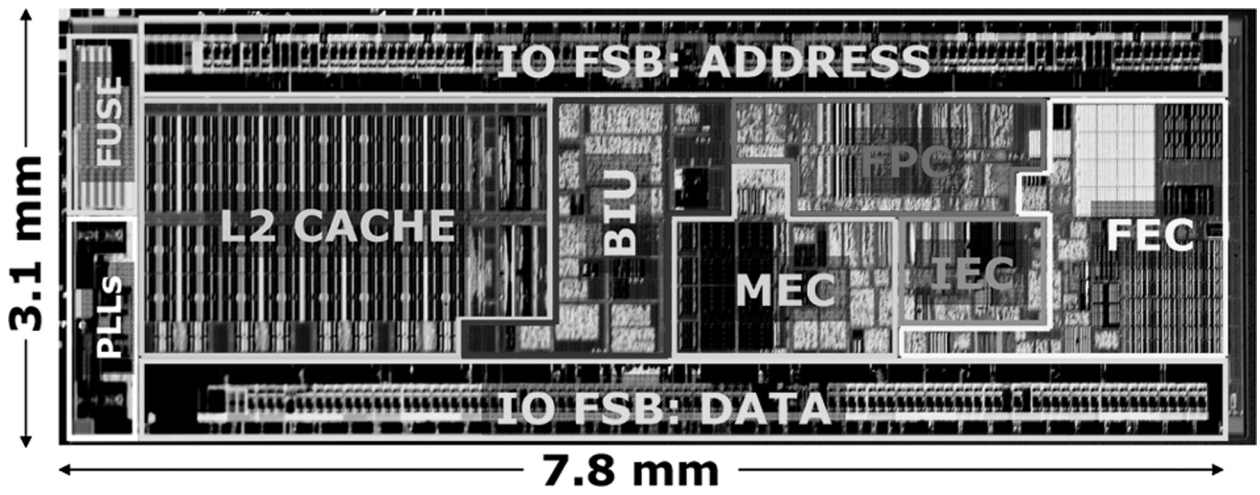

Fig. 6. Processor die photo with logic partitions highlighted.

pre-characterized standard cells with 45% using "structured data-pth" design techniques and 46% fully synthesized random logic blocks. The remaining 9% are full-custom blocks. The core contains 13.8 million schematic transistors, the Bus Interface unit contains 2.7 million and the L2 cache contains 30.7 million for a grand total of 47.2 million transistors in a 25 mm^2 die.

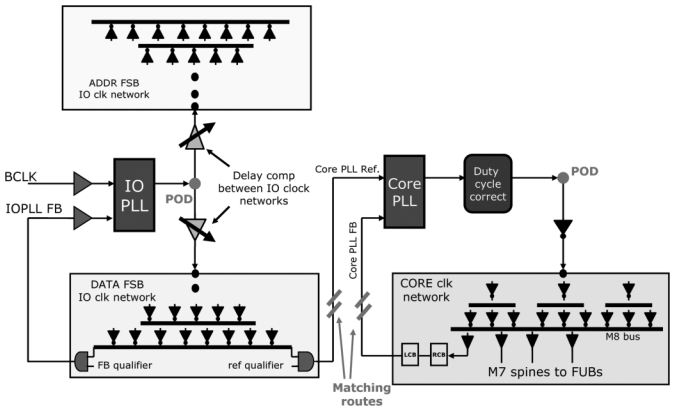

Fig. 7. Cascaded 2 PLL design.

V. Clock Architecture

The clock distribution is architected with power saving as a top priority. Clock recombination in global distribution is limited to a few critical stages after carefully studying the power/skew trade-off. Global clock routing is further reduced by 1) implementing a gridless topology that routes clock to locations only if required, 2) alignment of clock receivers to major clock spines, and 3) reducing the number of receivers on the clock network by minimizing clock cell cloning where clock tree synthesis is used. Flow automation and a cell based design approach are used to minimize implementation effort and achieve fast clock convergence. Fig. 7 illustrates the cascaded, two PLL design where the first PLL is used to generate the clocks for the double-pumped address and quad-pumped data FSB. A fuse-controlled delay line allows good delay compensation between the address bus and data bus clock distribution networks thus keeping the clock skew low. The second PLL receives a filtered 1X clock from the first PLL and multiplies up by 6X to 20X covering a range of 600 MHz to 2 GHz core clock for a 100 MHz platform clock. Fig. 8 shows the clock distribution topology. The core clock is taken to the middle of the chip and then drives three clock bays where the clock signal is buffered and amplified. The last stage of each clock bay is shorted with M8 which runs horizontally along the entire length of the 7.4 mm bay. Intermediate stages are not shorted unlike traditional clock spines. The only place where any kind of shorting may be done is the final M8 trunk and stage S10. Stage S10 inverters are shown as small dots on the floor plan. These inverters are located outside of the clock bays and are used to reduce the bay to bay clock skew if necessary based on timing analysis. The M8 trunk drives the final stage of the clock network which drives the M7 drivers. The M7 clock spines then deliver the clock to all FUB input pins. Each vertical M7 spine is a separate net. With this method, clock distribution dynamic power is kept below 7% of the total processor dynamic power with a worst case global distribution skew (1 sigma) under 6 ps including process variation. The static timing tool uses this clock skew as well as PLL jitter as a fixed budget in order to converge the MAXDELAY (set-up) and MINDELAY (hold) timing; clock skew for each path is calculated based on the Point-of-Divergence (POD) of the generating clock and the sampling clock. Typical clock uncertainty for same PLL domain paths are in the order of 20 ps for a set-up check and 50 ps for the hold check; cross-PLL domain paths could range from 120 to 150 ps.

VI. Power Saving Techniques

This processor uses Register File (RF) design style for all core arrays including the 32 KB L1 instruction cache, the 24 KB L1 data cache and the 10 KB C6 array which holds micro-architecture state during the C6 deep power down state. These use 8 T memory cells to attain better SER characteristics, high performance cache access time and lower voltage operation than traditional 6 T SRAM cells. The L1 caches implement 1 bit per byte parity and no ECC. Because RF arrays comprise over 50% of the total core area, they are an important contributor to overall chip power. Several power saving techniques are employed: fine granularity sleep on word-line drivers with double stacked PFETs with negligible wakeup times as shown in Fig. 9. The sleep signal in this WORDLINE driver is based on address decoding and adds a redundant PMOS transistor between the power supply and the word-line driver. The sleep signal is generally shared across 8 entries. When any one of the 8 entries is going to be accessed, the sleep is de-asserted. When none of the entries in a group-of-8 is being accessed, the sleep is asserted and turns off the sleep PMOS transistor resulting in lower leakage due to transistor stacking. In addition, sleep controls to allow floating of read bit-lines on the ROM arrays ($22\ \text{K}\mu\text{ops} \times 60\ \text{bits}/\mu\text{op}$) during non-access cycles are used (see Fig. 10). When the ROM is idle, the "slp" signal is asserted by the control logic. This causes the secondary pre-charge (on the intermediate bit-line) to be turned off, thereby floating the intermediate bit-line thus reducing leakage substantially; wake-up time performance impact is very small and comprehended in the cycle time analysis. This feature is not implemented on the local bit-line because leakage is already much lower due to device stacking and savings do not justify the increase in complexity. Finally, array bits on the "read-side" are architecturally pre-disposed to a value of "0" to reduce leakage power through the read stack.

VII. L2 Cache

The L2 cache is a phase-based, 8-way 512 KB design supporting single cycle throughput for both read and write operations. The design is fuse-able to 4-WAY 256 KB and extensible to 1 MB with the same the latency. It has in-line Single Error Correction Double Error Detection (SECDED) error correction mechanism (ECC) for the data and tag arrays for immunity against soft-errors and enhanced reliability. TAG, Least-Recently Used (LRU) and State bits are combined together into one array to minimize area and power. Tag and data sub-arrays are 4.5 KB and 17.5 KB, respectively with 256 cells (bit-cell area $= 0.3816\ \mu\text{m}^2$) per column with column redundancy in the data array to improve die yield. Designs for test (DFT) features include programmable built-in test (PBIST) and local direct access test (LDAT). Active and leakage power for the entire L2 including the back-side logic (BBL) blocks are 25 mW and 87 mW at 1.0 V and 2 GHz 90 °C, respectively.

Several micro-architectural features are incorporated to reduce average power of the cache. L2 activation starts in the TAG array with activation of L2grant signal at the high phase

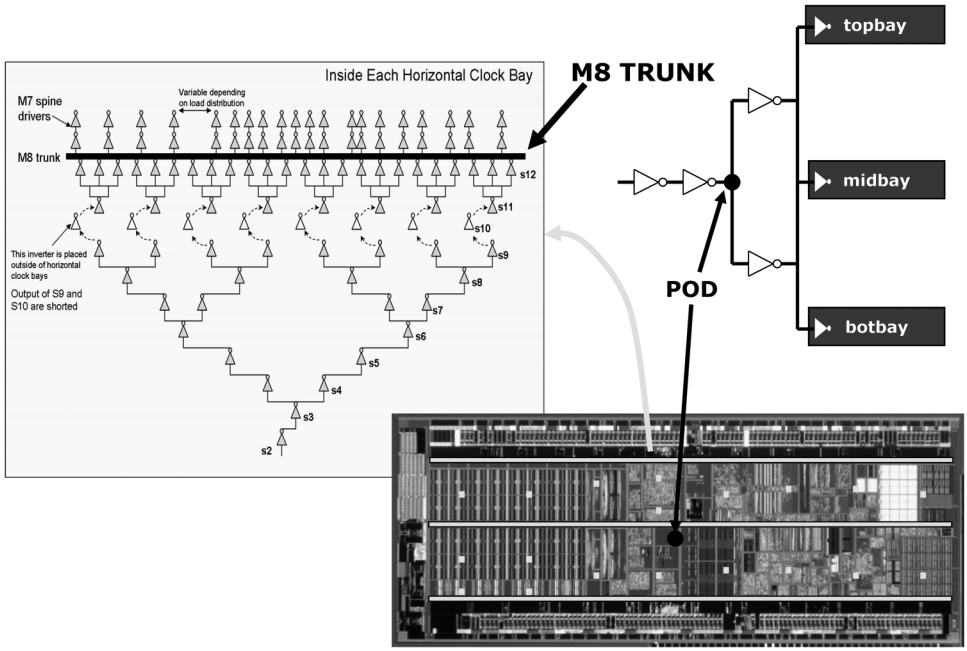

Fig. 8. Core clock distribution.

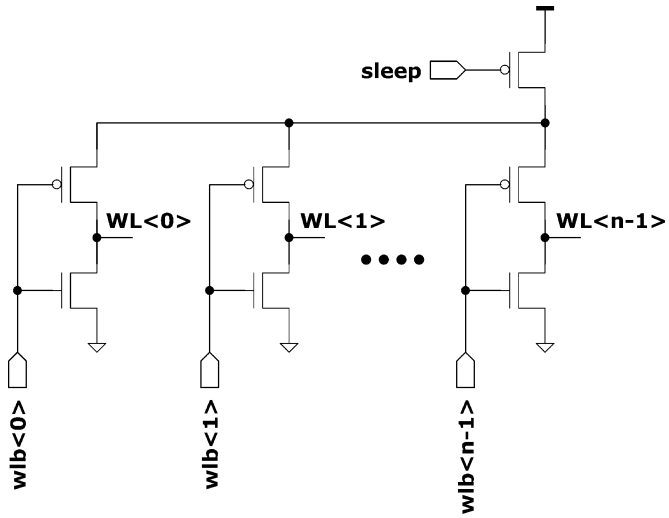

Fig. 9. Fine granularity sleep word-line driver to reduce leakage power via stacking effect.

of the clock. Similarly, data arrays remain in sleep mode until a qualified HIT signal is received from the TAG. This generates the SRAMWAKE signal for the relevant data sub-arrays and causes the memory cell to reach up to full voltage from its retention level; as a result only 4 out of 32 sub-arrays are on for any given time. The SRAMWAKE signal is held for several phases to reduce switching power on back-to-back access on the same WAY. Tag array pre-decode, word line (WL) launch, sense amplifier enable (SAEN), in-line ECC and transmit of the TRUE HIT to the core occur in 4 cycles. Data array decode, access, in-line ECC and transmit to the L1 occur in 4 cycles. During low performance operation, micro-code uses control registers in the BBL control unit to disable a pair of ways at a time. The Tag stays above retention value to maintain its invalid state while data drops below retention. During the C-6 power state, the voltage plane for the entire L2 is cut off. In addition, this phase-based design with serialized chunk access contributes to lowering the total leakage power since several blocks are shared (repeaters and ECC); the overall sequential count in the sub-array is reduced by 2X.

Average power reduction techniques include: power-gating (PG) transistors for the word-line drivers and active/sleep transistors for the memory arrays (see Fig. 11) [4]. For low-power states where the contents of the L2 cache need to be retained, the ACTIVE PFET is off and the SLEEP PFET is on allowing several levels of bias settings to set a virtual power supply to the array. These settings are configured with fuses and determined empirically. The 6-transistor bitcell has been optimized to operate and retain state at very low power supplies; over 2.5X leakage power reduction has been measured in this "sleep" state. A further 10X leakage power reduction can be attained if the sub-arrays are completely powered down; this is done on unused ways or a chopped design.

VIII. Off-Chip Drivers

A dual mode IO buffer is implemented where both legacy Gunning-Transceiver-Logic (GTL) signaling and a full CMOS swing can be supported with a fuse-able option. GTL IO is used for high performance FSB where data rates greater than 667 Mega-Transfers per second (MT/s) are required. In CMOS mode, the buffer can reliably transmit data at 533 MT/s while reducing the total FSB platform power from 200 to 500 mW as compared to GTL; this power savings is a strong function of FSB traffic. Essentially the resistance-compensated NFET pull-down impedance is reprogrammed to 55 ohms and the on-die-termination (using resistance-compensated 55 ohm PFETs) is turned off to eliminate DC power. Fig. 12 shows the dual mode

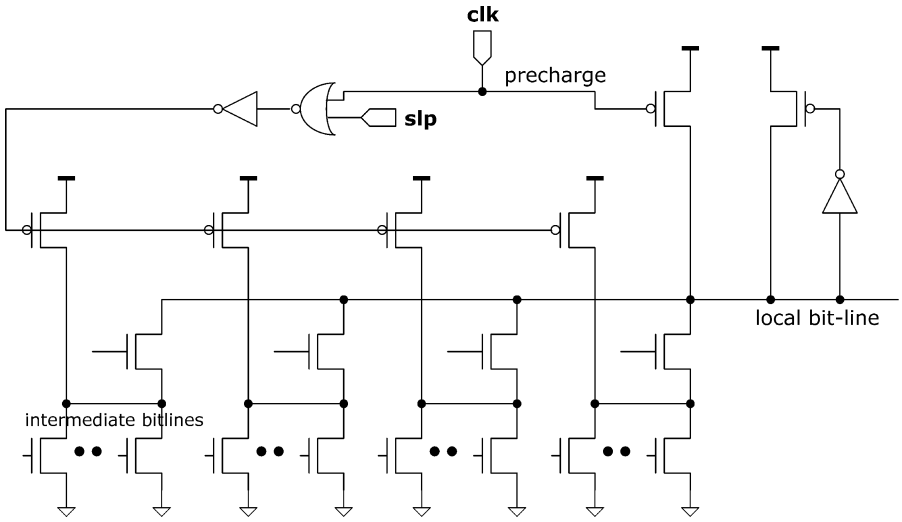

Fig. 10. ROM bitline floating scheme to reduce leakage power via stacking effect.

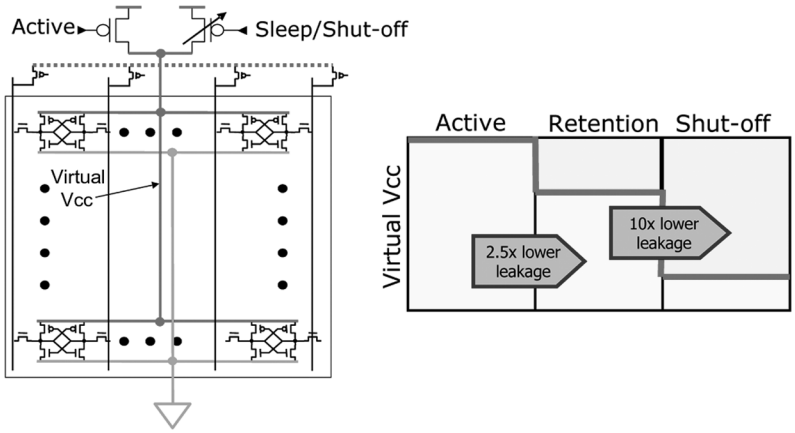

Fig. 11. L2 cache sleep circuit and shut-off (Idle) mode; resulting leakage power reduction is shown on the right.

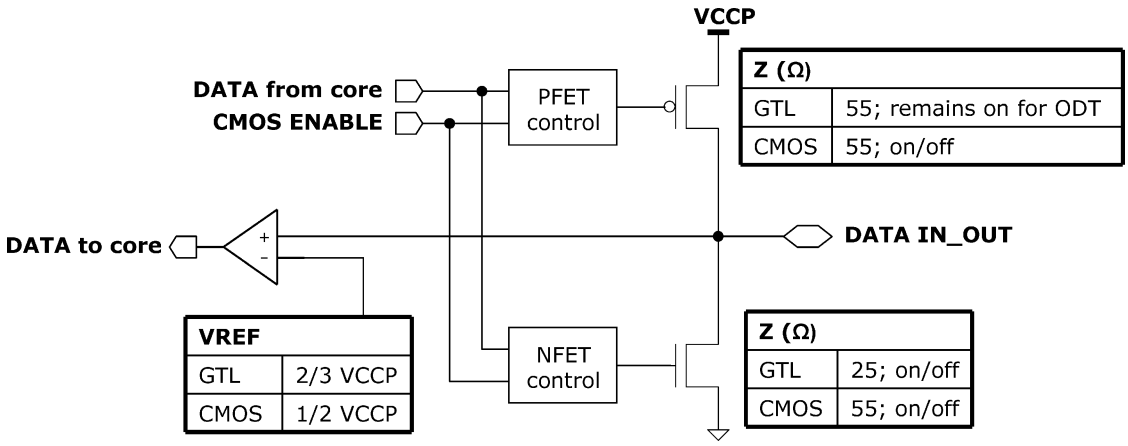

Fig. 12. GTL/CMOS dual mode FSB IO driver with On-Die-Termination (ODT) control.

buffer and receiver; note that the reference voltages of the differential input receivers are also reprogrammed from $2/3 * \text{VCCP}$ in GTL mode to $1/2 * \text{VCCP}$ in CMOS mode. For a sub-1 W platform, this power savings is very significant since its contribution is constant due to its power supply VCCP remaining at a constant 1.05 V.

FSB leakage power is further reduced by "splitting" the 1.05 V VCCP power supply and only keeping 21 pins "alive" during the C-6 power state. As a result, as shown in Fig. 13, the IO leakage power contribution to idle power can be reduced by 2X to 3X across several process corners; this is critical in achieving an idle power below 80 mW.

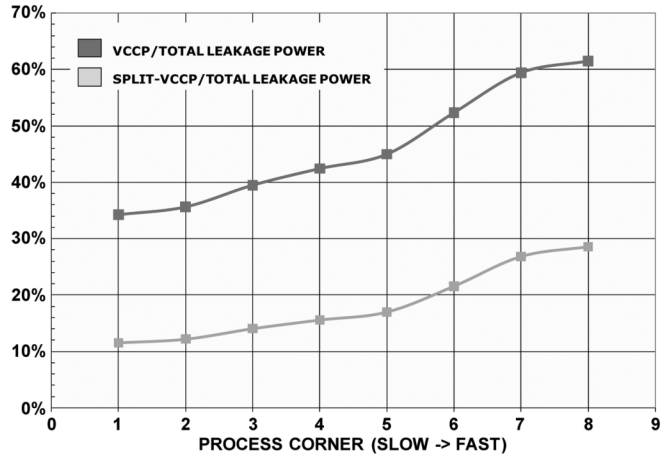

Fig. 13. Split FSB power supply leakage reduction in C-6 state.

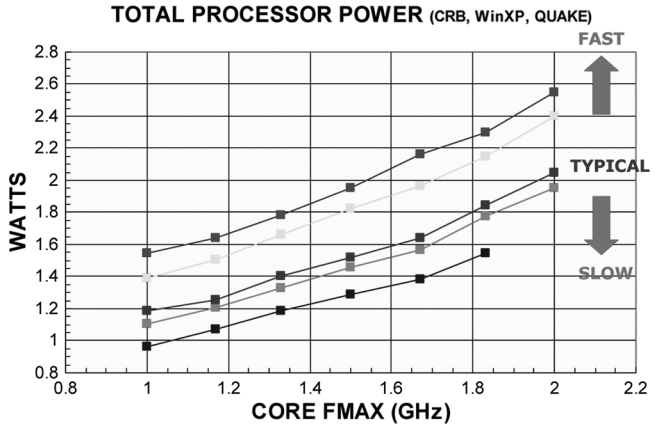

Fig. 15. Total power as a function of core frequency and process corner measured in a reference platform running QUAKE for 30 minutes.

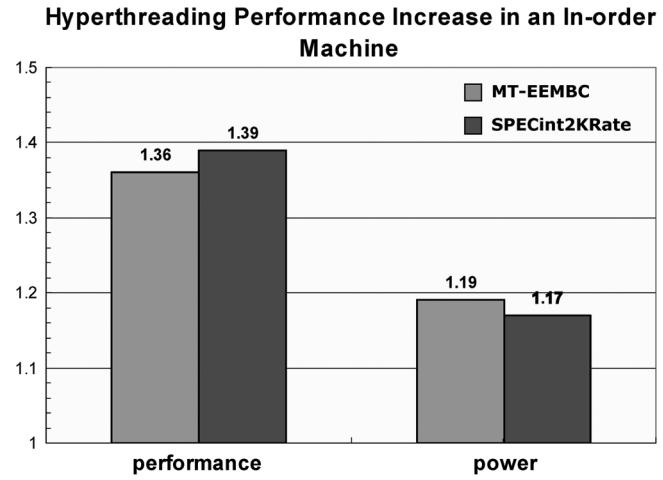

Fig. 14. Simultaneous multi-threading performance gain and its power increase relative to single-threaded performance/power.

IX. Performance and Power

Simultaneous multi-threading (MT) results for the EEMBC and SPECint2KRATE benchmarks for this 2-issue, in-order pipeline are shown in Fig. 14 where a 36% to 39% improvement is measured at an increase of 17% to 19% in power. These measurements are obtained on a custom reference design with a 533 MT/s FSB, 1 GB of DDR memory and a custom chipset. TDP power measured at various core frequencies and process corners while running the game QUAKE in the same reference platform is shown in Fig. 15.

X. Conclusion

A new micro-architecture compatible with Intel's CORE2 DUO processor is presented in 45 nm CMOS technology. This micro-architecture has been optimized for Mobile Internet Devices by carefully adding performance features that are power-efficient; a two-issue, in-order pipeline supporting simultaneous multi-threading achieved the best performance/power results. Various power management techniques have been used to lower dynamic and leakage power. Architecturally, a new C-6 power state is used where its core power supply is shut-down resulting in very low leakage power. As a result, average and idle power are substantially reduced. Addressing dynamic power reduction, various techniques are used: a non-gridded clock distribution to minimize dynamic clock power, register file and 6 T bitcells are optimized to operate reliably at the lowest core power supply, pervasive use of traditional clock gating, and the availability of a CMOS FSB. Addressing leakage power, word-line driver gating and floating bit-lines have been used along with complete shut-down of unused L2 cache sub-arrays. Finally, a split VCCP FSB power supply has been introduced to further reduce idle power. This processor is suitable for MIDs given the range ($\sim$0.65 W to 2.0 W) of measured TDP power on real world applications. 2 GHz core frequencies can be achieved at 1.0 V and 90 °C.

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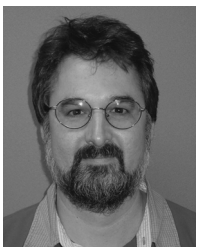


Gianfranco Gerosa (M'77) received the B.S.E.E. degree from the Georgia Institute of Tecehnology, Atlanta, GA, in 1977, the M.S.E.E. degree from the Ohio State University (OSU) in 1980, and the Ph.D. degree in electrical engineering from OSU in 1982.

He has 25 years of experience in the semiconductor industry. He started his career at Intel Corporation as a device engineer in Portland Technology Development working on 1.2 μm CMOS technology. He moved on to circuit design related activities on various memory product projects at Motorola. In the 1990s, he was involved in the design of a family of PowerPC microprocessors in a joint venture with IBM. He led the PowerPC603 integration team where he was responsible for integration, PLL design, clocking, IO buffer design, and ESD protection. Later, he took the role of design manager for the PowerPC750 RISC microprocessor. He rejoined Intel to work on new Intel Architecture (IA) microprocessor developments in Austin, Texas; he was part of the path-finding and technology readiness effort for a low power IA core design in 45 nm CMOS which eventually became Intel's ATOM processor product. He manages the L2 cache and analog (PLL, IO, fuses, digital thermal sensing) design teams. He has 12 issued patents, and he has contributed to over 20 refereed papers related to chip design, circuit design, and ESD protection; two are full-length journal papers on the PowerPC 603 and PowerPC 750 RISC microprocessors.

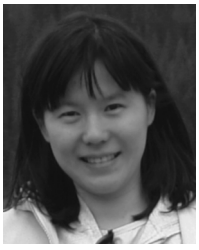
Dr. Gerosa was a member of the ISSCC's digital subcommittee (1997–1999) where he co-chaired several clocking/logic sessions, and he was a 1998 JSSC guest editor.

Steve Curtis received the Bachelors degree in electrical engineering from the University of Michigan, and the Masters degree in electrical engineering from Cornell University, Ithaca, NY.

He has been with Intel more than 12 years. He is responsible for power estimation, methodology, convergence and post-silicon bin splits for the CPU design team of Intel's Ultra Mobility Group based in Austin, TX. Previously, he was responsible for custom circuit blocks and key components of physical integration methodology on a Pentium 4 project. He joined Intel, Hillsboro, OR, in 1996 as a custom circuit designer in the Integer Fireball Execution data-path responsible for timing convergence. Prior to joining Intel, he worked for Motorola in Scottsdale, AZ, as a logic and circuit designer of custom ASICs.

Michael D'Addeo received the Bachelors degree (*cum laude*) in electrical engineering from Northeastern University, Boston, MA, and the Masters degree in business management (MBA) from Walden University, Baltimore, MD.

He started off in semiconductor process engineering in photolithography and has worked in the areas of physical design and full-chip integration of microprocessor products at Digital Equipment Corporation and Motorola. He has worked at Intel since 1999 and he currently manages CPU integration for low power IA in Austin, TX. He holds several US patents related to low power circuits and layout reliability.



Bo Jiang received the B.S. degree in physics in 1991, the M.S. degree in 1995, and the Ph.D. degree in 1997 in electrical engineering, from the University of Texas at Austin.

She started her career at Advanced Materials Group in Motorola, Austin, TX, working on development of advanced memory technologies using ferroelectric materials and high permittivity dielectrics. She moved on to circuit design and joined Intel in 2000. She worked on SRAM design, register file design and clock distribution for several microprocessor and SOC design projects at Intel, including the low power IA family of products that became Intel ATOM processors. She currently manages the low power IA clocking team in Ultra Mobility Group.

Belliappa Kuttanna is the chief architect of the ATOM processor. He is a Senior Principal Engineer and he has been with Intel for 9 years. He has been in the semiconductor industry for 17 years. Prior to joining Intel, he worked on several PowerPC designs while with Motorola and a SPARC CPU design with SUN Microsystems. He is currently working on the definition of future ATOM-based products. He has 21 issued patents.

Feroze Merchant received the B.S. degree in electronics engineering from the University of Bombay, India, in 1992, and the M.S. degree in electrical and computer engineering from the University of Southern California (USC), Los Angeles, in 1995.

He has 13 years of experience in the semiconductor industry. He has worked on several microprocessor projects at Intel including the Pentium Pro, Pentium 4 and most recently the ATOM processor. He led the design of several Register File (RF) and ROM structures on the ATOM microprocessor, including design of the Level 1 caches. His current work focuses on ultra low voltage processor design for variation sensitive circuits such as RF, level shifters, latches and flip-flops. In addition, he manages the Register File design team and the CPU front-end design team on Intel's next generation (32 nm) ATOM microprocessor project.

Binta Patel received the Bachelors of Engineering in Electronics degree from MIET-Nagpur University, India, in 1989, and the M.S.E.E. degree from Polytechnic University New York in 1991.

She has 15 years of experience working in the Semiconductor Industry; while at IBM for eight years, she worked on various types of dynamic circuit topologies, register files, adders and caches for PowerPC processors in 90 nm CMOS and SOI technologies. In 2000, she joined Intel to work on a new Intel Architecture (IA) microprocessor development in Austin, TX; she contributed to path-finding work on various circuits for cache and execution units. Later, she joined the low power processor team to work on PLLs and front side bus (FSB) IO in 45 nm CMOS; she led the effort to add a CMOS-only mode to the existing GTL FSB IO as well as other low-power features to the PLLs and IO. This design eventually became the ATOM processor. Currently, she is working on low power 32 nm PLL clock architecture for SOCs and a new low power thermal sensor scheme. She has five issued patents.

Mohammed H. Taufique received the B.S.E.E. and M.S.E.E. degrees in 1992 and 1994, respectively, from the University of Texas at Austin.

He has 14 years of experience in SRAM and Cache circuit design. He joined Motorola's Fast Static Ram (FSRAM) Division in 1994 and designed several generations of Asynchronous, Late-write and Double-Data-Rate stand-alone SRAM. He then joined Motorola's Somerset Design Center to work on the L1 cache for a PowerPC microprocessor. He joined Intel Corporation in 2000 to design SRAMs for Intel's first DSP core code-named FRIO. In 2001, he joined the mobility group as the technical lead for L2 Cache and later on managed the circuit team that designed the L2 cache for the ATOM processor. Currently, he is managing the SRAM and FUSE circuit team for next generation 32 nm low power core and the SOC. He has several papers and patents in the field of his expertise.

Haytham Samarchi received the B.S. degree in physics in 1985 from Virginia Commonwealth University, Richmond, VA, and the M.S. degree in electrical engineering in 1987 from the University of Virginia, Charlottesville.

He joined Intel Corporation in 1999 where he held various microprocessor design and management positions and recently managed the Atom processor design project to high volume production. Prior to joining Intel, he spent nine years with ROSS Technology, Inc., holding circuit design and management positions for the company's SPARC microprocessor products. Prior to joining ROSS Technology, he spent three years with Seattle Silicon Corporation in the hardware design group.