13.2 A 45nm 3.5G Baseband-and-Multimedia Application Processor using Adaptive Body-Bias and Ultra-Low-Power Techniques

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System on Chip (SoC) integration is the theme of the first integrated 3.5G baseband and multimedia applications processor fabricated using a low-power digital and analog design platform and 45nm process technology [1]. This SoC supports mobile standards: HSUPA/HSDPA, WCDMA, EDGE/GPRS/GSM and applications such as MPEG-4 video streaming, Java and MP3 audio. The high-performance multimedia, multiprocessor engine includes an 840MHz ARM1176, a 480MHz TMS320C55x DSP, and a 240MHz image processor.

Targeted at mobile, battery-operated SoCs, TI's 45nm low power (LP) process (Fig. 13.2.1) employs 193i lithography tools and includes an optimized PNO gate dielectric, a dual damascene Cu metal stack with a thick top Cu level and an Al level for pad passivation, power and signal routing, and an ultra-low K dielectric for routing levels. The targeted 25% performance over the 65nm LP process is achieved without increasing Ioff as increases in Igate and Igidl over the 65nm technology are offset by reduced subthreshold leakage (Isub). The performance boost is achieved through strain techniques, Tox reduction, and source/drain optimization using a millisecond anneal. By maintaining the same Ioff as the 65nm technology, previously developed power management techniques are reused. RF components (CMOS inductors and varactors), capacitors, resistors, and MIM capacitors are supported; in addition to drain extended CMOS and a 30Å gate oxide for high voltage support.

The needs of digital and analog libraries, and RF components strongly influenced the development of the LP process. For example, metal level thickness is optimized based on the library architecture. The 45nm LP library contains multiple gate length cells for performance-power optimization and achieves greater than 2× the density of the 65nm library. The library supports ultra-low power techniques including adaptive voltage scaling [2] and adaptive body-bias. A full suite of compiler memories has been developed using custom 6-T SRAM bits as small as $0.25\mu m^2$, a custom ROM bit, and an electrically programmable fuse bit. Standard and complex IOs such as MDDR and USB2.0 are also supported.

The power management (PM) architecture of this SoC consists of multiple independently controlled power domains, split-rail SRAMs and ROMs, multi-gate length cells, dynamic voltage/frequency scaling (DVFS), and adaptive voltage scaling (AVS). Building on these previously published PM techniques [2-4], the second generation SmartReflex performance and power management technology adds adaptive body-bias and a global/local blocking memory architecture (Fig. 13.2.2). SmartPriMer, a methodology for power management integration and protocol control, is used to automatically create a Unified Power Format (UPF) [5] compliant specification and PM RTL.

Adaptive Body-Bias (ABB) modulates the body voltage of transistors based on the process distribution [6] and consists of forward body-bias (FBB) for performance boost and reverse body-bias (RBB) for power reduction. In applications when more performance is demanded at the higher DVFS Operating Performance Point, FBB is used to reduce the effective V_t, thereby increasing system throughput. Since the performance is limited by cold silicon, FBB is only applied to these devices. FBB is not applied to all silicon since this unnecessarily increases leakage power on devices already capable of providing the required performance. When lower power is required, RBB increases the effective V_t, hence reducing leakage power. Since the worst-case power occurs on hot silicon, RBB is applied only to these devices. RBB is not applied to all silicon since this decreases performance on devices that already dissipate lower leakage power. Measurements from an ABB testchip confirm the benefits of FBB and RBB (Fig. 13.2.3). This ABB approach achieves an optimal balance of performance and power with circuit techniques alone, eliminating the need for additional LVT or HVT logic transistors.

The device has 16Mb of SRAM and ROM in ~250 instances, making leakage reduction in both the memory arrays and the memory periphery logic critical to overall SoC active power. Periphery leakage power reduction is accomplished by separating the periphery power supply from array power supply. In this way, the core logic voltage is applied to the non-bit cell portion of the memory thus reducing power while the array power is controlled separately to ensure bit stability [2]. Additionally, segmenting the memory array into multiple blocks allows for array leakage reduction (Fig. 13.2.4). Individual blocks are put into a low leakage power state, providing a 2× leakage reduction when that block is not being accessed. Finally, during sleep state, the supply voltage is scaled down to provide leakage reduction without losing the contents of the memory.

PM implementations are becoming increasingly complex and invasive, and impacting SoC design from system definition, to RTL, to verification, to physical design. It is essential to simplify the PM implementation and flow, thus avoiding custom hand-crafted deliverables for each SoC. The solution must be user friendly, simplify the PM design, reduce development time, and ensure correctness without compromising flexibility to meet a variety of product requirements. SmartPriMer, a tool developed to address this objective, has been successfully applied to this SoC for the control of ABB and memory bias control.

First the PM architecture is defined in the power management specification and input to SmartPriMer with the non-PM RTL (Fig. 13.2.5). The tool then automatically provides three key functions for PM integration: 1) RTL for power domain insertion and protocol control, 2) power management state controllers, and 3) a full suite of PM verification and assertion checks. SmartPriMer generates synthesizable PM RTL code allowing RTL that originally did not contain any power management to be part of a power managed design. One standardized power sequence protocol is used across IPs and PM architectures. Furthermore, RTL code is automatically generated for the ABB, SRAM, and bandgap state controllers and power sequence protocol controllers. These controllers are provided along with a verification suite to be used by the SoC team to validate correct integration at the SoC level. Finally, a UPF specification is generated that contains power-aware design information understood by UPF compliant tools for consistent semantics across all phases of design and verification.

A 45nm SoC using an LP process and library optimized for mobile applications and ultra-low power techniques is described. This device contains over 16Mb of memory, 10 Mgates of logic, and many analog IP's, achieving more than 2× area reduction from the prior technology node. The low-power optimized process technology, combined with DVFS and ABB, is expected to boost the 45nm SoC performance to ~155% of the 65nm baseline enabling next generation multimedia applications. The active power dissipation of the 45nm SoC is decreased to 37% of the 65nm, for the same performance. Shown in Fig. 13.2.6, the ultra-low power techniques used in this SoC provide three orders of magnitude of total power reduction from the maximum application workload to deep sleep with less than 150μW of power.

References:

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[4] H. Mair, et al., "A 65-nm Mobile Multimedia Applications Processor with an Adaptive Power Management Scheme to Compensate for Variations," *VLSI*, pp. 224-225, June 2007.

[5] Accellera, "Unified Power Format (UPF) Standard", v.1.0, Feb. 22, 2007. Accessed on Nov. 9, 2007, <http://www.accellera.org>.

[6] J. Tschanz, et al, "Adaptive Frequency and Biasing Techniques for Tolerance to Dynamic Temperature-Voltage Variations and Aging," *ISSCC Dig. Tech. Papers*, pp. 292-293, Feb. 2007.

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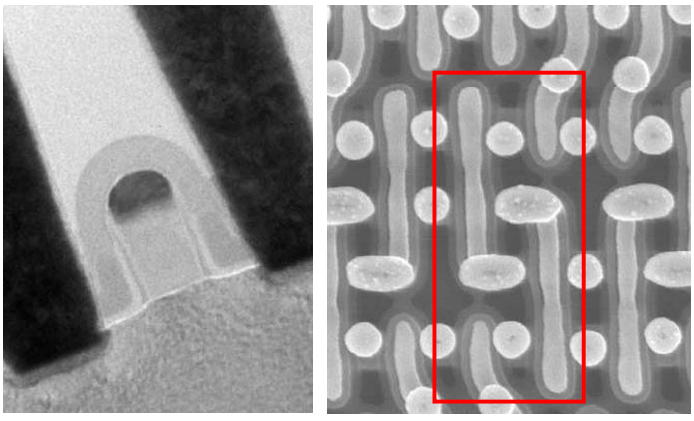


Figure 13.2.1: 45nm NMOS transistor and 0.25μm SRAM bit.

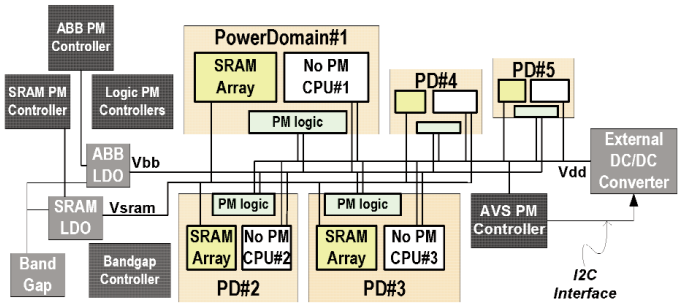


Figure 13.2.2: SoC power management architecture.

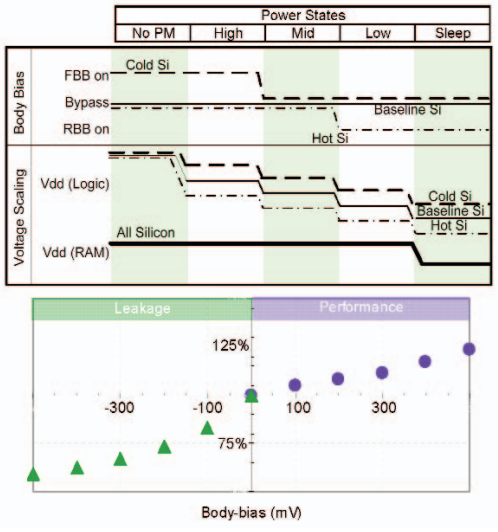


Figure 13.2.3: Adaptive Body-Bias and Adaptive Voltage Scaling configuration with mode and process, and measurements from a testchip.

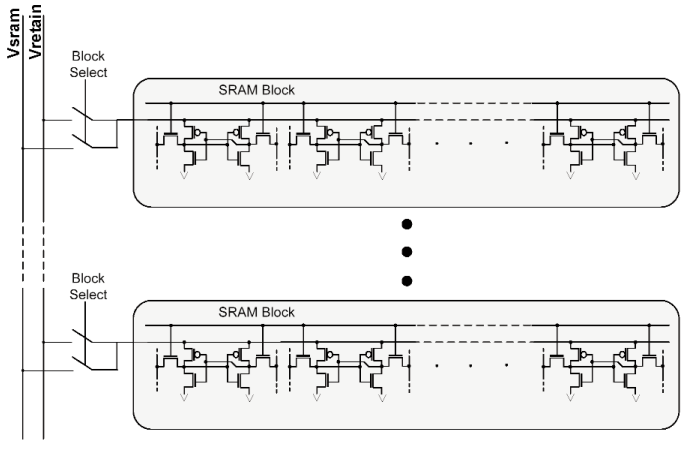


Figure 13.2.4: SRAM architecture for array leakage reduction.

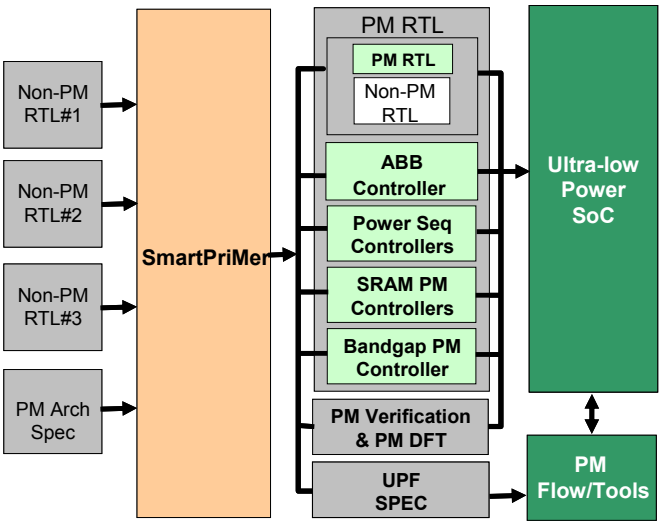
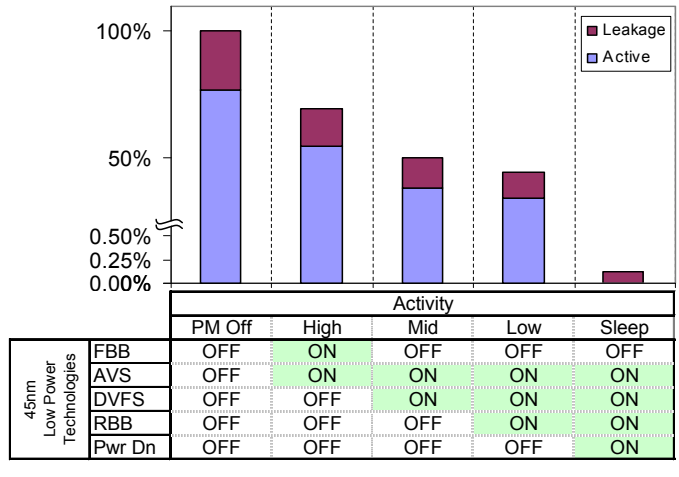


Figure 13.2.5: SmartPriMer power management protocol/controllers auto-generation.



45nm Low Power Technologies	Activity: PM Off	High	Mid	Low	Sleep
FBB	OFF	ON	OFF	OFF	OFF
AVS	OFF	ON	ON	ON	ON
DVFS	OFF	OFF	ON	ON	ON
RBB	OFF	OFF	OFF	ON	ON
Pwr Dn	OFF	OFF	OFF	OFF	ON

Figure 13.2.6: 45nm low power techniques provide three orders of magnitude total power reduction from maximum application workload to deep sleep.

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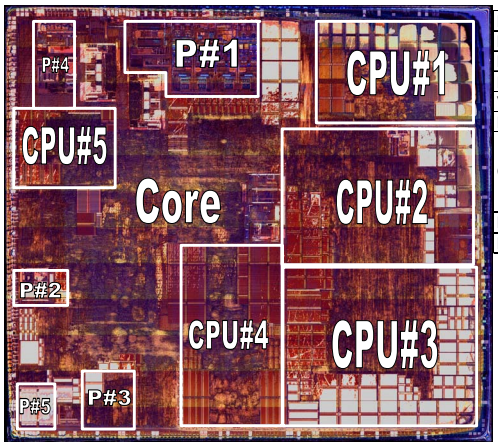

Process	45 nm
Logic Gates	10 M
Memory	16 Mb
Performance	840 MHz
Voltage	1.2-0.8V
Package	Flip chip
Cores	1176
	320C55x
	DBB
	ISP
MHz scaling	155%
Power scaling	37%

Figure 13.2.7: 45nm integrated 3.5G baseband and multimedia applications processor die micrograph.

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