High Performance Ultra-Low Energy RRAM with Good Retention and Endurance

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Abstract

High performance novel RRAM of 0.3 μW set power (0.1 μA at 3 V), 0.6 nW reset power (-0.3 nA at -1.8 V), fast 20 ns switching time, ultra-low 6 fJ switching energy, large 7×10^2 resistance window for 10^4 sec retention at 125°C, and 10^6 cycling endurance were measured simultaneously. This is the first time that the switching energy of new non-volatile memory is close to existing Flash Memory.

Introduction

The Charge-Trapping Flash (CTF) non-volatile memory (NVM) device [1]-[5] has the lowest switching energy among various new NVMs, but the degraded 10^4 endurance at highly scaled device is the basic physical limitation according to *ITRS* [1]. The fast switching RRAM [6]-[12] has high potential for down-scaling beyond Flash Memory, if the high switching current and power can be lowered. Besides, larger than 10^5 endurance for solid-state disc (SSD), large high- to low- resistance state ratio (HRS/LRS) for multi level cell (MLC), simple forming free and diode-driven operation are also required. To address these issues, we previously reported an ultra-low power RRAM using covalent-bond-dielectric/ metal-oxide of $GeO_x/SrTiO_3$ (GeO/STO) [12]. Good 85°C retention and stable 10^5 cycling endurance were reached based on the new hopping conduction mechanism [13]. However, further performance improvement is related to the defect control by O_2/Ar. In this paper, we report an ultra-low 6 fJ switching energy RRAM with fast 20 ns time and large 10^6 endurance. Low switching current of setting 0.1 μA at 3 V to LRS and resetting -0.3 nA at -1.8 V to HRS are obtained. The very small reset current can be driven by a Schottky diode rather than using a large transistor. These excellent performances were achieved using $GeO_x/Hf_{0.38}O_{0.39}N_{0.23}$ (GeO/HfON), where the HfON has been used for high performance CTF NVM [4]-[5] due to the significantly higher trap density and deeper trap energy than those of HfO_2. The high density traps are vitally important for defect-assisted hopping conduction from measured negative temperature coefficient (TC) [13], rather than the positive TC by metallic filament conduction in metal-oxide RRAM [9]. Such negative TC generated by hopping conduction is also known in highly defective GaAs [14] used for THz detector. The traps in HfON are related to Hf-N bond from shifted energy of x-ray photoelectron spectroscopy (XPS), since no RRAM function can be measured in similar GeO/HfO_2. This suggests the mechanism for LRS due to hopping via Hf-N traps and oxygen vacancies in GeO. The electron injection is the key to break weakly linked hopping conduction as verified by direct device measurement. This is the first time the switching energy of new NVM device near existing Flash Memory with >10^5 endurance for potential SSD application.

Experiments

For embedded integration, the Ni/GeO/HfON/TaN device was fabricated on SiO_2-isolated p-type Si substrates, which has the similar Metal-Insulator-Metal (MIM) structure of DRAM capacitors [15]-[16]. The 100 nm TaN was first deposited by PVD and patterned to form the bottom electrode. Then various thick HfON and GeO insulators were deposited by PVD. After that, the 50 nm Ni was deposited and patterned to form the top electrode. For comparison, similar MIM devices were also fabricated by replacing the HfON dielectric with HfO_2 or AlON. The formed device was measured by set/reset, cycling endurance and retention to 125°C, under the similar CTF NVM test conditions [2]-[5].

Results and Discussion

A. Set/Reset Characteristics:

Fig. 1 shows the swept *I-V* characteristics of Ni/GeO/ HfON/TaN device. Large HRS/LRS memory window of 9×10^2 (0.2 V read), low self-compliance set current of 0.1 μA at 3 V (0.3 μW), reset -0.3 nA at -1.8 V (0.6 nW) are reached at the same time. Since no metal in GeO, the low set power is ascribed to electron injection created defects in HfON and GeO from lower work function bottom TaN (4.6 eV) rather than the top Ni (5.1 eV). This is quite different from the metallic filament in metal-oxide RRAM [9]. Here the HfON has been used for CTF NVM [4]-[5] due to the high trap density and deep trap energy. We further replaced the HfON by AlON, since high performance CTF device can also be reached [2]-[3]. As shown in Fig. 2, similar asymmetric *I-V* switching behavior is also found in Ni/GeO/AlON/TaN RRAM, but the set current and HRS/LRS memory window are worse than Ni/GeO/HfON/TaN device. We also replaced the HfON by HfO_2 in a similar MIM device structure. In sharp contrast, as shown in Fig. 3, no memory function in Ni/GeO/HfO_2/TaN device can be measured up to ±6 V, indicating the importance by adding N into HfO_2. The asymmetric *I-V* and very small reset current can be driven by a Schottky diode that also has the asymmetric *I-V* characteristics shown in Fig. 4. Such configuration can form the cross-point 3D NVM with very high density. This device has acceptable set and reset distribution shown in Fig. 5, which is due to low switching energy by hopping conduction.

B. Conduction Mechanism:

The very small set and reset currents are further analyzed. As shown in Fig. 6, the low HRS and LRS currents are governed by Schottky emission and space-charge-limited current (SCLC), respectively. To investigate the conduction mechanism, we also measured the temperature dependence on HRS and LRS currents. As shown in Fig. 7, the increasing HRS current is well predicted by Schottky emission from $ln(I)$-$V^{1/2}$ analysis in Fig. 6. The increasing LRS current with temperature gives a negative TC and opposite to the positive TC in metal-oxide RRAM [9]. An activation energy (E_a) of 0.40 eV is obtained from $ln(R)$-$1/kT$ plot shown in Fig. 8. The negative TC and close E_a values with previous highly defective Si [13] suggest the LRS related to hopping conduction via defects. We have used XPS to analyze the defects. As shown in Fig. 9, the peak energy of Hf-N shifts from the energy position of stoichiometric Hf_3N_4, indicating forming vacancies ($V_{Hf\text{-}N}{}^{n+}$) and dangling bonds. Similar non-stoichiometric GeO_x and O-vacancies ($V_{Ge\text{-}O}{}^{2+}$) were also found by XPS. Thus the hopping conduction is related to the N-vacancies in HfON and O-vacancies in GeO_x. To study the reset mechanism, a very low current compliance of 1 pA is applied during reset (Fig. 10). However, no reset action can be found since the measured resistance is still at LRS. This result indicates that the reset is directly due to the current injection via electrode. The injected electrons can break the weakly linked hopping conduction pass at ultra-low energy:

$$V_{Ge\text{-}O}{}^{2+}+2e^{-}+Ge\text{-}O\rightarrow Ge\text{-}O^{*};\quad V_{Hf\text{-}N}{}^{n+}+ne^{-}+Hf\text{-}N\rightarrow Hf\text{-}N^{*} \quad (1)$$

C. Retention & Endurance:

This hopping conduction mechanism is shown in Fig. 11 that also explains the record lowest switching power, good retention of large 7×10^2 HRS/LRS for 10^4 sec retention at 125°C (Fig. 12), fast switching time of 20 ns (Fig. 13) and excellent 10^6 cycling endurance (Fig. 14). The good retention is because the reset can only be disrupted by injected electrons to annihilate the hopping conduction pass. The excellent endurance is due to the fast 20 ns time and low 6 fJ switching energy with less stress to GeO/HfON. Such ultra-low energy to form hopping pass is close the 3 fJ energy ($E=Q\times\Delta V$) of Flash memory with small 500 electrons storage at the typical Program/Erase voltage of 20/-20 V (Fig. 11). Table 1 compares RRAM devices. This new device has the record lowest 6 fJ switching energy, fast 20 ns switching time and 10^6 endurance among various RRAM [6]-[12].

Conclusions

A novel ultra-low energy RRAM has been realized for the first time, which has 6 fJ switching energy and 10^6 endurance. These excellent NVM performances were achieved by using the hopping conduction in highly defective HfON and GeO.

Acknowledgments

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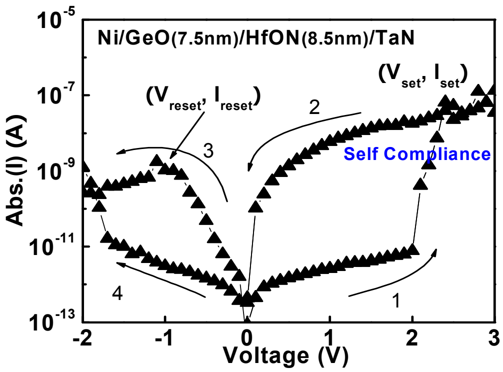

Fig. 1. Swept *I-V* curves of Ni/GeO/HfON/TaN RRAM. The arrows indicate the bias sweeping direction.

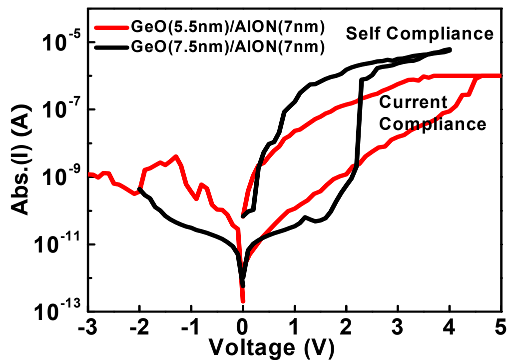

Fig. 2. Swept *I-V* curves of Ni/GeO/AlON/TaN RRAM. The arrows indicate the bias sweeping direction.

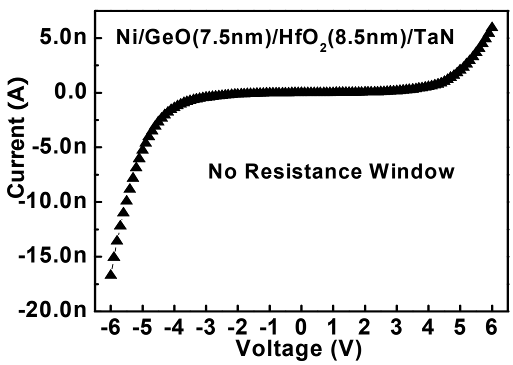

Fig. 3. *I-V* curves of Ni/GeO/HfO_2/TaN RRAM. No resistance window can be found.

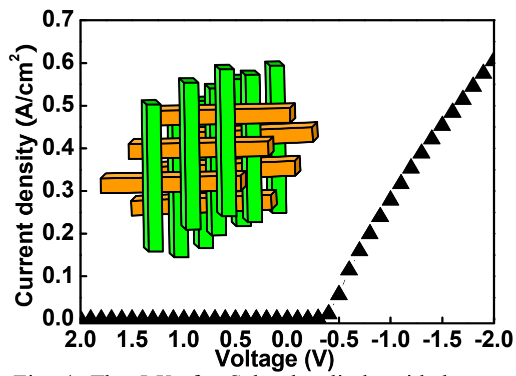

Fig. 4. The *I-V* of a Schottky diode with low reverse current and asymmetric *I-V* behavior, similar to our RRAM, and useful to drive the device for 3D NVM.

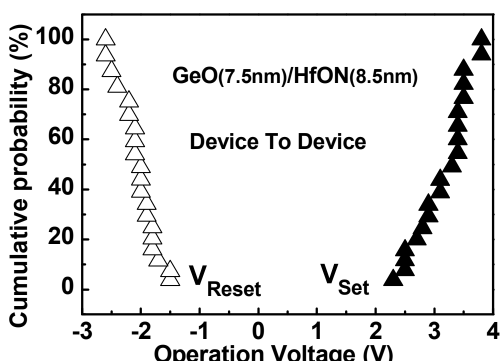

Fig. 5. V_{SET} and V_{RESET} distributions of GeO/HfON RRAM devices.

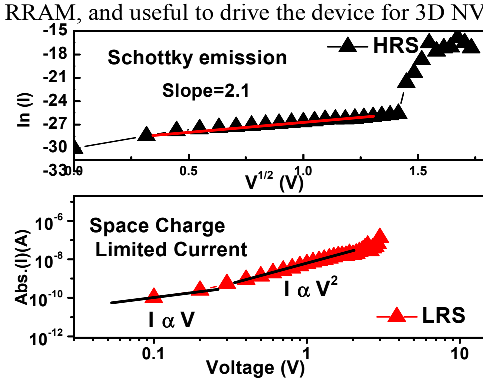

Fig. 6. *I-V* of (a) HRS and (b) LRS by fitting with Schottky emission and SCLC conduction mechanisms.

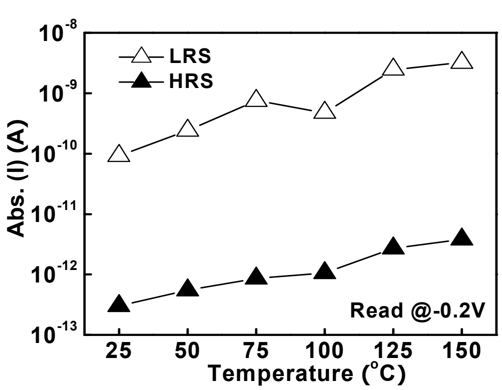

Fig. 7. Temperature dependent HRS and LRS of Ni/GeO/HfON/TaN RRAM and showing negative TC.

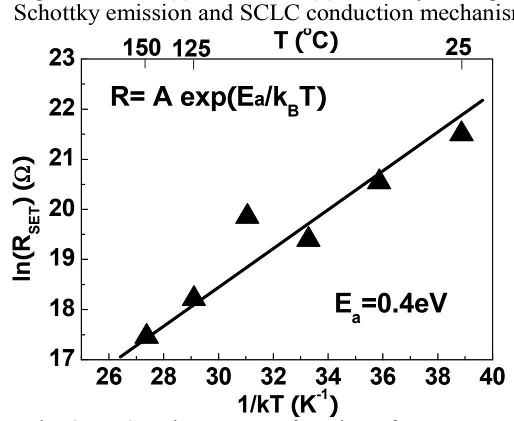

Fig. 8. LRS resistance as a function of temperatures.

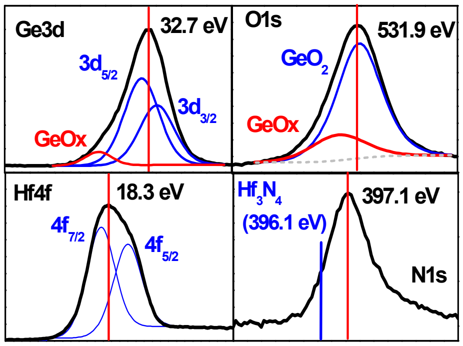

Fig. 9. The XPS spectra of Ge 3d, O 1s, Hf 4f and N 1s core level in GeO/HfON.

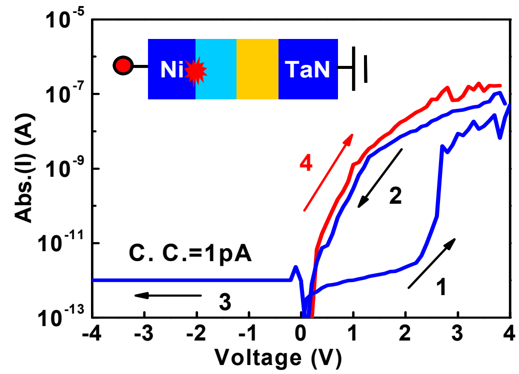

Fig. 10. *I-V* curves of Ni/GeO/HfON/TaN RRAM with 1 pA current compliance during reset but still at LRS.

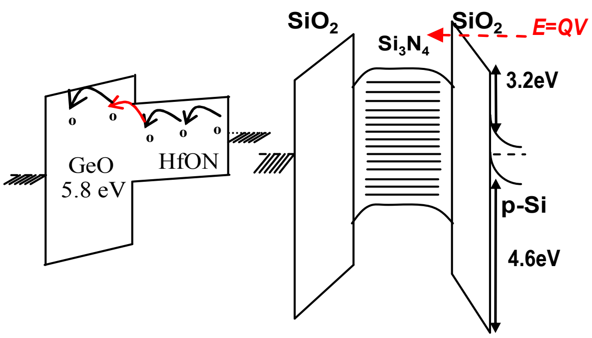

Fig. 11. Band diagrams of Ni/GeO/HfON/TaN RRAM and Charge-Trapping Flash MONOS NVM devices.

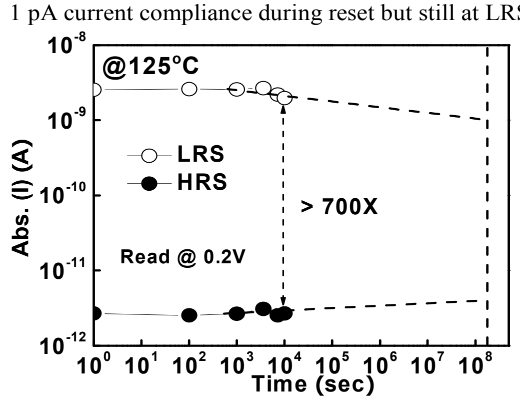

Fig. 12. Retention of Ni/GeO/HfON/TaN RRAM at 125°C.

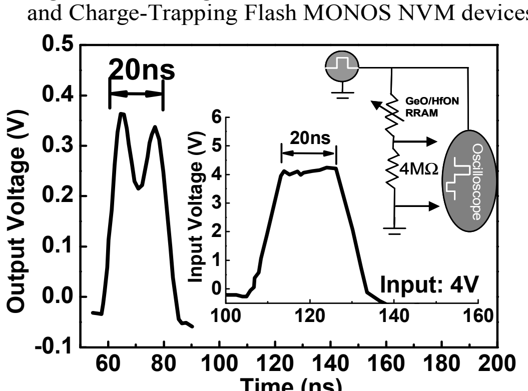

Fig. 13. Voltage waveform of a fixed resistor series connected to the Ni/GeO/HfON/TaN RRAM, under an input voltage pulse of 4 V for 20 ns.

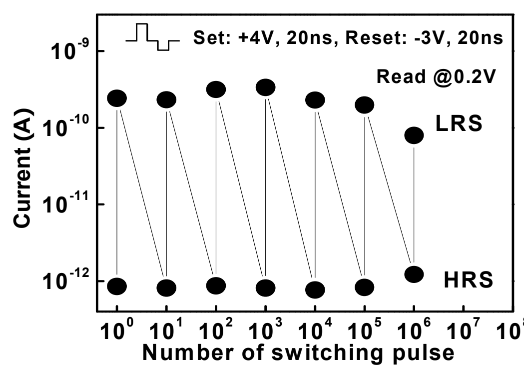

Fig. 14. Endurance of Ni/GeO/HfON/TaN RRAM. Stable switching to 10^6 cycles at 20 ns is obtained.

Dielectric	Cu-MoOx [6]	ZnO [7]	Al/PCMO [8]	NiO [9]	Al/PCMO [10]	GeO/STO [12]	**GeO/HfON**
T/B Electrode	Pt/Cu	TiN/Pt	Pt/W	Au/n-Si	Pt/Pt	Ni/TaN	**Ni/TaN**
I_{SET} @ V_{SET}	100mA, 2V	3mA, 0.9V	-1mA, -3V	0.6mA, 3.9V	1mA, -4V	-3.5uA, -1.1V	**0.1uA, 3V**
I_{RESET}, V_{RESET}	-80mA,-1.5V	-4mA, -1.2V	1uA, 3V	5mA, 1.4V	10uA, 4V	0.1nA, 0.13V	**-0.3nA, -1.8V**
Initial HRS/LRS	20	$3x10^2$	$5x10^2$	~ $2x10^2$	~10	$>10^5$	**$9x10^2$**
Retention HRS/LRS @10^4s	15, 85C	$2.9x10^2$, 25C	$4.9x10^2$, 125C	—	—	10^5, 85C	**$7x10^2$, 125C**
Cycles, pulse	10^6, 1us	—	10^6, 1us	—	10^4	10^6, 50ns	**10^6, 20ns**
$P_{SET, RESET}$	200, 120mW	—	3mW, 3uW	—	—	4uW, 16pW	**0.3uW, 0.6nW**

Table 1. Comparison of device integrity data for various RRAM devices.