Hierarchical Power Distribution and Power Management Scheme for a Single Chip Mobile Processor

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ABSTRACT
A hierarchical power distribution methodology that enables more than dozen power domains in a chip and a power management scheme using 20 power domains are described. This method can achieve very low leakage current in the partial active mode of a single chip mobile processor. The single chip mobile processor embedded three CPU's that is baseband processor, application processor, and multi-media processor. In the "waiting for calling" mode of the mobile handsets, application processor and multi-media processor part can be power-off. This chip can power off these power domains although the some of baseband parts are actively operating.. Many new techniques for multiple power domains in the chip are described.

Categories and Subject Descriptors
B.7.1 [Types and Design Styles]:

General Terms: Design.

This paper describes the output of two projects.

(1) Fundamental circuits research on hierarchical power domain = joint research by Hitachi, Ltd. and Renesas Technology Corp.[4]

(2) LSI design for one chip mobile processor = joint development by NTT DoCoMo Inc. and Renesas Technology Corp.[5]

DAC 2006, July 24–28, 2006, San Francisco, California, USA.

Keywords
VLSI, power domain, partial power off, mobile processor.

1. INTRODUCTION
Presently, cellular phones are used not only for voice communications, e-mail, and web browsing, but also for more advanced functions such as video telephony and 3D Java games. Therefore, a high performance application processor, for example SH-Mobile[1], is typically embedded in a cellular phone in addition to the baseband processor. In the baseband processor, dual mode operation is required supporting both the high-performance WCDMA service and the GSM/GPRS service which is generally available worldwide. Therefore, present cellular phone handsets are implemented by mounting two or three processors, being managed of their power activity in each usage case and hence to maximize the battery life. Though a single chip integration of application and baseband processor(s) is obviously attractive, a novel scheme that can control the power inside the chip is required to realize the integration.

2. CHIP OVERVIEW
Figure 1 shows a micro photo of the chip. In the chip, 3 domains are defined. Each domain has a CPU, which runs a different OS. Therefore, this system architecture runs multiple OS's on heterogeneous multi-CPU cores. The major reason why we designed a 3-domain architecture in the chip is to (1) maximize the reuse of huge software assets of conventional cellular phones by keeping the same system architecture; (2) enable separate system development in cellular phone design; (3) introduce different efficient power shut down schemes according to the cellular phone use for the reduction of leakage power consumption; (4) reduce the conflicts between each subsystems; and (5) support separate dynamic clock frequency changes for each domain for the reduction of dynamic power consumption.

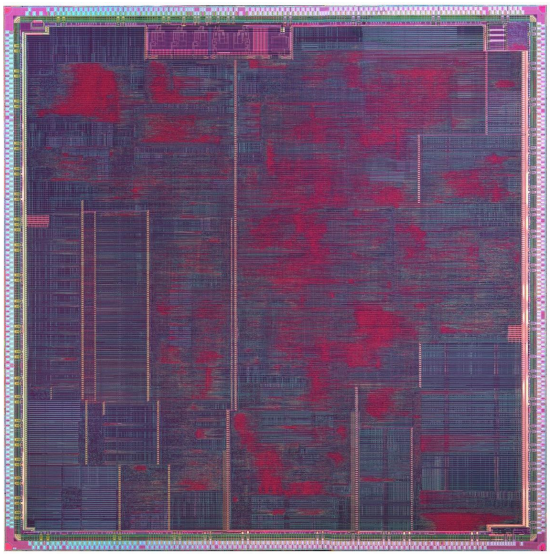


Fig.1 Photo of the Chip

3. POWER DOMAINS

3.1 Problems for Many Power Domains

One chip integration can achieve the high performance, small package size, low cost, low dynamic power consumption. However, the static power consumption that is caused by the leakage current may increase. If the system is organized by multi-chip, some of unused chips can be totally power off which reduce the leakage current. Then, partial power off scheme that enables to cut down the leakage current of unused part of the chip is very important in this integration. The chip introduced 20 power domains, which can achieve the detail partial power off inside the chip to cut down the leakage current even when some of the chip part is actively working.

Problems occurring by increasing power domains are: (1) routing problems of global nets and clock trees, (2) integrity of shutdown elements that should be inserted between power domains and (3) stability of VDD/GND lines of active domains while transitions of the power state of the other domains.

3.2 Common Power Domain

The CPD(Common Power Domain) is introduced to avoid problem (1). This domain is shaped like slits with proper spacing and defined as a mostly powered on domain. Introducing this concept [4,5], we can place repeaters to transmit global nets and buffers consisting clock trees by utilizing CPD area as stepping-stones.

Addressing problem (2): signals from a domain which may be power off should be transmitted through special circuits called µI/O [2]. To minimizing the overhead of µI/Os to be inserted, we adopt hierarchical structure in power domains [4,5]. There are some relationship between each power domains in the point of their functionalities. Exploiting such relationships, we defined hierarchical relation between power domains as shown in Figure 3. We could omit the µI/Os on the nets from higher to lower hierarchy because a higher domain will not be powered off while lower one is powered on.

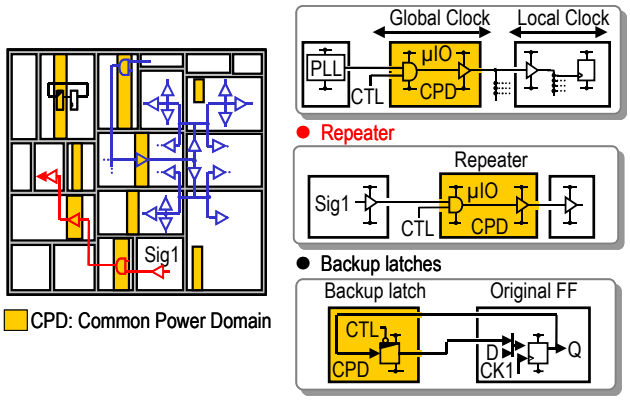


Fig. 2 Common Power Domain

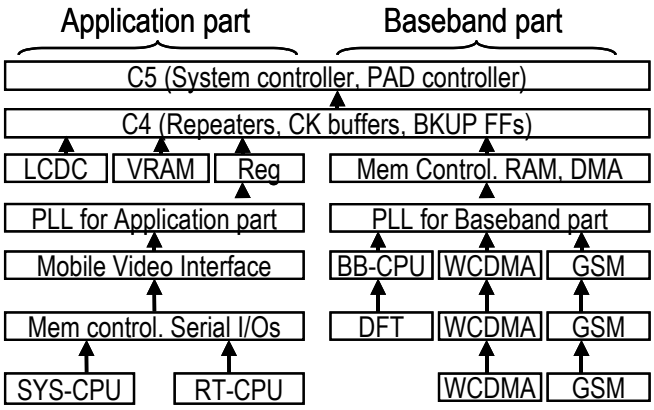


Fig. 3 Hierarchical Structure of Power Domains

3.3 Power Switch Design

Figure 4 shows the power switch (PSW) configurations for the power domains, the CPD, and the SRAM. There are three global power lines: VDD, VSS, and VSSM_CPD. The VSSM_CPD is the power-gated ground line for the CPD. The power lines are laid out in a horizontal stripe across the chip. Local power lines for each power domain (VSSM_PDx) are also laid out in a horizontal stripe on the same layer but dedicated to each power domain. The power switches for each power domain are placed on two opposite sides of the each power domain vertically across the chip. Those for the CPD are placed along two sides of the chip in the vertical direction. The SRAM has its own embedded dedicated power switches for achieving low-leakage retention mode [3].

The power switch consists of a thick-gate-oxide high-Vth NMOS that is used for I/O circuitry. The I/O supply (VCC) of 3.3 V is applied to the gate of power switches to provide sufficient on-resistance even under a low-voltage supply for core circuitry (VDD). In 90-nm processes, the gate-tunneling current is not negligible. It becomes about 10 % of the total leakages at room

temperature. However, the power switch suppresses both the sub-threshold and gate-tunneling currents well. The leakage reduction ratio was about 1/4000 for a power domain with one million gates.

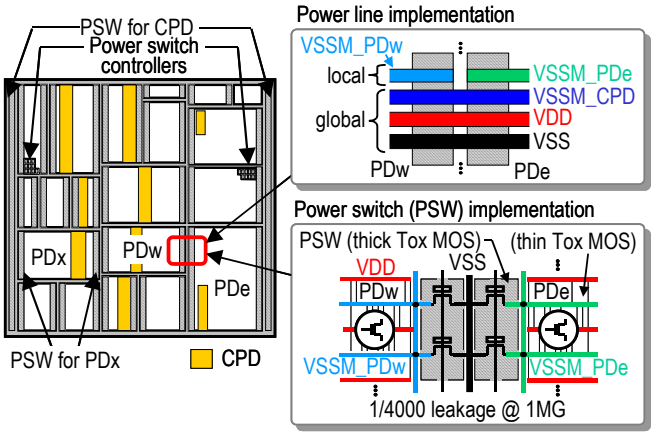


Fig.4 Power Line and Power Switch Implementation

3.4 Reduce Rush Current

Turning on the power switches may cause a large rush current on the power line. Figure 5 shows the power switch controller (PSWC). A fast transition time between the power-off and on states without a rush current was achieved by using a newly developed precise gate-voltage sensing scheme in combination with a low-slew-rate driving scheme [2]. The precise gate-voltage sensing scheme detects a 90 % drive of the gate of power switches to the VCC voltage by a dynamic comparator. It effectively reduces the time margin. The dynamic comparator was used to make process migration easy, to lower the PSWC's standby current, and to minimize area overhead. A power domain with one million gates had a 3.9-us recovery time and a 53.8-mA rush current under worst rush-current condition. To resolve problem (3),

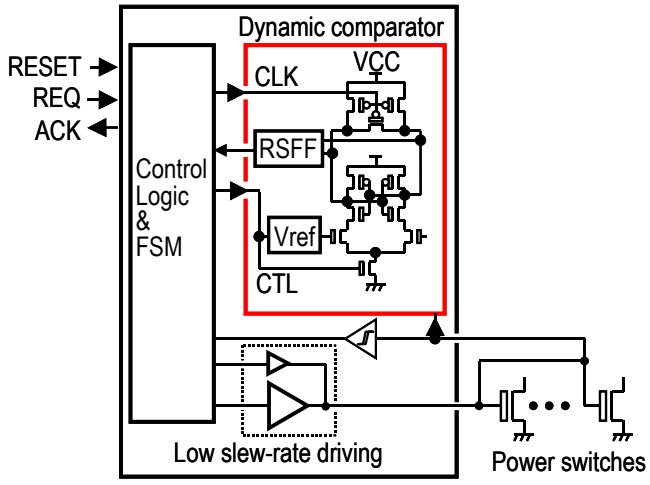


Fig. 5 Power Switch Controller Circuits

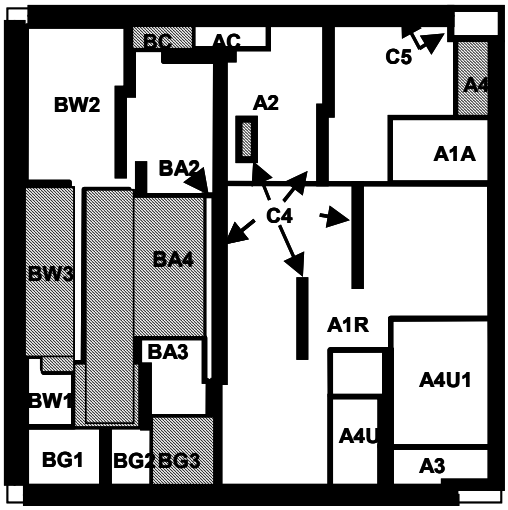
we not only developed new design of power switch itself to minimize rush current [4] but also established a sequential power on scheme.[5] When SYSC processes a power on request for several domains, it issues the power on signal to the corresponding power switches one-by-one and waits for the ready signal from it. This logic is designed as domino-logic, which establishes minimum wakeup time satisfying VCC/GND stability.

4. RESULTS

Figure 6 shows some examples of activating power domain in scenes of mobile phone usage. In this situation, the mobile handsets are in the scene of "waiting for calling". In this scene, the only part of baseband part should be working. Other parts like application processor part and multi-media part can be power-off. Then, the measurement results of leakage current in this scene correspond to a handset in waiting for a call; a leakage current of 299μA @ RT is achieved, although the leakage current of the all power domain of the chip is 849μA.

The chip was implemented to partition a single SoC into 20 power domains, and on-chip voltage monitors (VMONs) were implemented in several power domains for measuring the power supply drop due to the rush current. A voltage drop in the order of mV was successfully measured by the VMONs, which convert the local supply voltage fluctuation into the frequency-modulated oscillation, and outputted to the chip external. Figure 7 shows the measurement results with the worst-load-case voltage drop in the TEG and that in the single chip mobile processor. It revealed that the voltage drop was negligible.

Figure 8 shows the domain partition on the chip. The chip is fabricated in a 90nm, 8M(7Cu+1Al), CMOS dual-Vth low-power process technology. Supply voltages are 1.2V(internal) and 1.8/2.5/3.3V(I/O). It integrates total 181M transistors, 13.5M Gate logics and 20.2 Mbit memory. Die size is 11.15mm x 11.15mm.



Shaded Power Domains are ON

Fig.6 Partial Power Off Scene

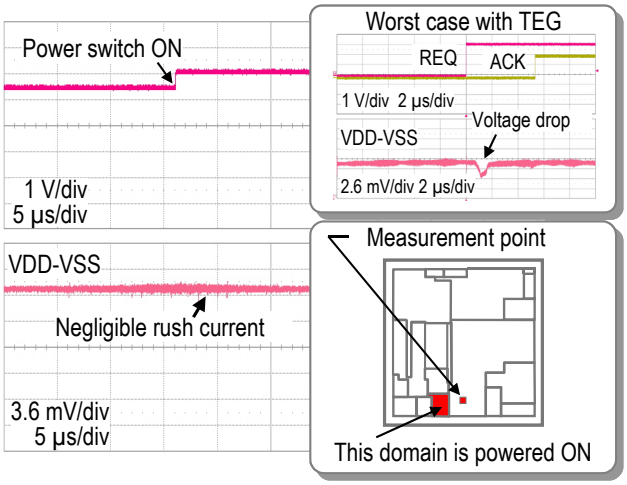


Fig. 7 Measured Rush Current

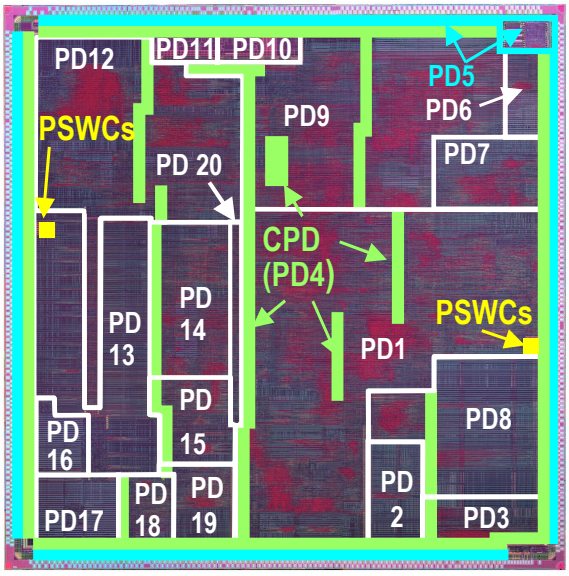


Fig. 8 Power Domain Structure of the Chip

5. CONCLUSION

A single chip integration of three CPUs and many IP's, which are baseband processor, application processor, and multi-media processor was described. One chip integration can achieve the high performance, small package size, low cost, low dynamic power consumption. However, the static power consumption that is caused by the leakage current may increase. It is because if the system is organized by multi-chip, some of unused chip can be totally power off which reduce the leakage current. Then, partial power-off scheme which enable to cut down the leakage current of unused part of the chip is very important. The chip introduced 20 power domains which can achieve the detail partial power off inside the chip to cut down the leakage current according to the practical mobile handsets scenes like "waiting for calling," etc. To minimize the complexity of handling many power domains in the chip, we developed the hierarchical power domains which corresponds to the chip system behavior. A power supply noise by the rush current which may be caused by the switching on power domains may be problems, because power on sequences are performed even when some of parts of the chip are operating. Some of techniques to reduce such rush current are described. The measured rush current in the chip was negligible small. These techniques achieve the detailed level partial power-off scheme. The measured leakage current in the specific scene of the mobile handsets can be reduced to 299µA although the total leakage current of the chip was 849µA.

6. REFERENCES

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