Architectural and Circuit Design Techniques for Power Management of Ultra-Low-Power MCU Systems

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***Abstract*— A holistic power saving concept for ultra-low-power microcontroller (MCU) systems involving application requirements, system architecture, and circuit design techniques is presented. The key of this concept is a digitally enhanced low dropout regulator (LDO) supplying the MCU digital core. By making use of known system power information, the LDO digitally adapts its maximum current drive capability up to 2.56 mA while its quiescent current is as low as 650 nA in light load conditions. In this way, the power management overhead is drastically reduced when operating at low clock speeds enabling system energy savings of 31% at 1 MHz. At the same time, a drastic reduction of the LDO output capacitance enables ultra-low-power consumption during sleep and energy efficient wake-up, resulting in system energy savings up to a factor of 4.6.**

***Index Terms*— Digitally enhanced analog, energy harvesting, fully integrated voltage regulator, power management unit, ultra-low-power microcontroller.**

I. Introduction

ULTRA-LOW-POWER microcontroller (MCU) systems serve as the brain for most of today's small-scale battery-powered and energy-harvesting applications such as smart sensor and control devices [1]. The requirements for such systems are rather different compared with performance/cost-driven main stream MCU applications. Instead of optimizing the processing speed, the goal is to minimize the system energy consumption and in turn to maximize the battery lifetime while maintaining the processing power needed for the application.

Typical ultra-low-power applications periodically wake-up to acquire and process sensor data. For the vast majority of time when being idle, the MCU system is set into a low-power sleep mode. This periodic operation is reflected in the measured power consumption profiles shown in Fig. 1. Here, two examples, a smoke detector [2] and a glass break detector [3], represent both ends of the broad range of application scenarios. The overall energy consumption of the MCU system can be defined as the sum of the following three components:

$$E_{\text{total}} = P_{\text{active}} \cdot t_{\text{active}} + P_{\text{sleep}} \cdot \left(t_{\text{cycle}} - t_{\text{active}}\right) + E_{\text{wake-up}}. \quad (1)$$

The major design challenge is to achieve minimum energy consumption within each power mode as well as for transition between modes. Due to fundamental design tradeoffs, these requirements, however, cannot be optimized concurrently. Instead, a sweet spot for system energy consumption needs to be found, which strongly depends on the application scenario. For example, some applications like a smoke detector spend most of their time sleeping and thus require ultra-low-power consumption during sleep. Other applications such as a glass break detector wake up very frequently making an energy-efficient wake-up critical.

A power management system adapting to the needs of different applications should be highly flexible. Therefore a mixed-signal approach is required to address both the system-level and the circuit-level challenges necessary to minimize energy consumption in both the analog and digital domains. In modern CMOS processes particularly, the increasing leakage current becomes a limiting factor for battery lifetime of

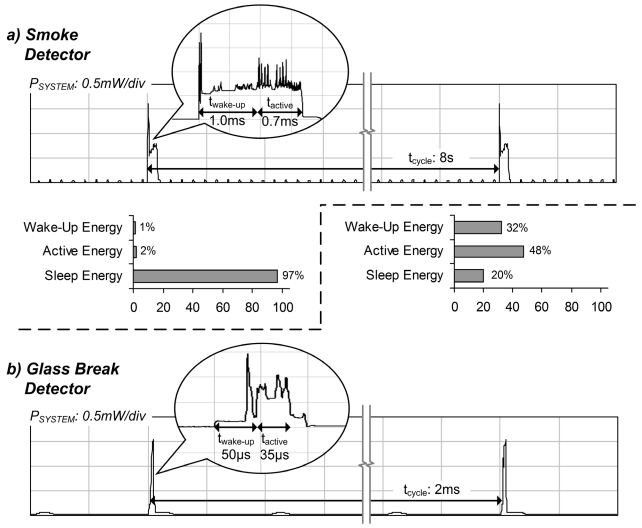

Fig. 1. Measured power consumption profile of (a) a smoke detector [2] and (b) a glass break detector application [3] at $V_{\text{DD}} = 3.0$ V and temperature = 25 °C.

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ultra-low-power applications and has to be addressed by the power management as well.

Power management techniques known from mobile application processors, which generally combine a switching regulator with power gating for leakage reduction [4], are not best suited here. We will discuss in the following why they target a different class of applications with a different sweet spot for system energy consumption.

This paper will examine power management techniques and the related tradeoffs for ultra-low-power MCU systems. It thereby follows a top–down approach. After briefly introducing the MCU system in Section II, the system power contributors and the related system tradeoffs are analyzed. This includes the power consumption during sleep in Section III, the energy required for switching between power modes in Section IV, as well as the energy and performance scalability in active mode in Section V. Based on this discussion of system energy consumption and the individual contributors, the discrete load adaptive LDO scheme is introduced in Section VI. It is thereby emphasized how the digital enhancement technique can reconcile the challenges of both system architecture and circuit design. After discussing the LDO implementation details in Section VII, measurement results are provided in Section VIII showing the LDO performance both in standalone and in applicative conditions supplying the MCU digital core.

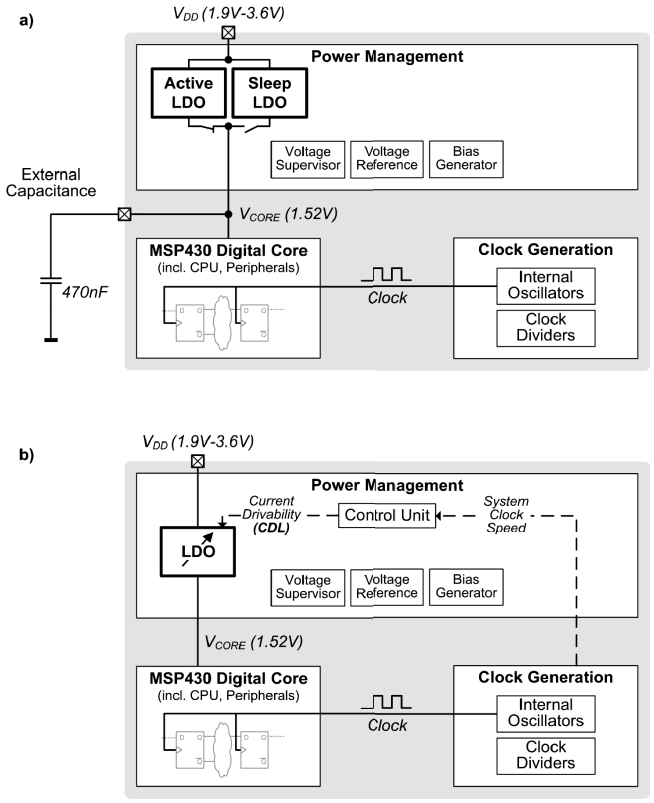


Fig. 2. Ultra-low-power MCU systems with (a) a state-of-the-art power management unit using two separate LDOs and (b) a system power-aware power management unit using a digitally enhanced LDO.

II. System Architecture

The investigations presented in this paper are based on two very similar ultra-low-power MCU systems, designed for small scale battery-powered and energy-harvesting applications (see Fig. 2). The power management of a commercially available MCU system has been adopted here for experimental purposes. Both MCU systems comprise a 16-bit MSP430 CPU, analog/digital peripherals as well as embedded ferroelectric RAM (FRAM) memory for fast write capability. To react to environmental changes, an energy-aware power management and clock generation unit dynamically adapts the performance and power consumption of the MCU system. The one MCU system depicted in Fig. 2(a) uses a state-of-the-art power management solution [1]. Here, the digital core is supplied by two separate low dropout regulators (LDOs) for active and sleep mode, respectively. Both LDOs are compensated by an external capacitance of 470 nF. For the other MCU system depicted in Fig. 2(b), the digital core is supplied by a single digitally enhanced LDO [5]. By exploiting the correlation between system clock speed and system power demand, this LDO digitally adapts its maximum current drive capability. To achieve fast and energy-efficient wake-up, this LDO does not need any external capacitance. It instead relies on the intrinsic capacitance of the MCU digital core amounting to overall 3nF. As no additional capacitance is required, neither on-chip nor off-chip, the system costs are, as a positive side effect, minimized. For both MCU systems, the supply voltage V_{DD} ranges from 1.9 to 3.6 V, determined by battery voltage over lifetime. The core supply voltage V_{CORE} is 1.52 V, decided as trade-off between speed/performance requirements on the one side and active power considerations on the other side. Both test dies are fabricated in a 0.13 μm digital CMOS process.

III. Power Saving Techniques During Sleep

Since typical ultra-low-power applications wait the vast majority of time for the next trigger event, power consumption during sleep significantly contributes to the overall energy consumption (see Fig. 1). To minimize power consumption during sleep, the presented MCU systems support fine-graded sleep modes, in which the system is gradually disabled. Fig. 3 gives an overview of power consumption and power savings in the different sleep modes and will be discussed in the following.

In the most elementary sleep mode, in the following referred to as low-power state, the CPU operation is stopped by gating the system clock. The clock generation unit including the on-chip oscillators is disabled. As depicted in Fig. 3, the system power consumption in the low-power state is thus dominated by leakage caused by the MCU digital core as well as power management overhead. To minimize the power overhead, the power management unit is set into a low-power state. State-of-the-art MCU systems for this purpose make use of multiple LDOs [6], each optimized for a dedicated load condition, resulting in a slow and complex transition between system operating modes. With increasing leakage current in modern CMOS technologies, the system power savings in this basic sleep mode become more and more

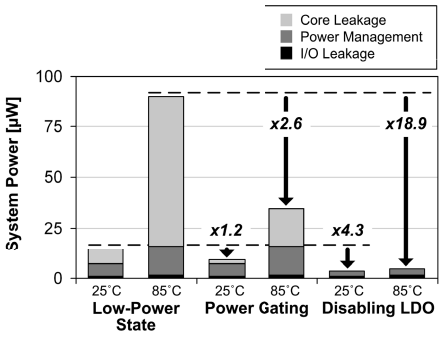


Fig. 3. Measured/estimated power consumption of the MCU system during sleep at $V_{\mathrm{DD}} = 3.0$ V.

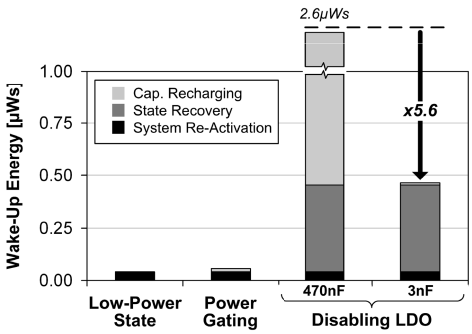


Fig. 4. Measured/estimated energy required for wake-up of the MCU system from the low-power modes at $V_{\mathrm{DD}} = 3.0$ V and $T = 25$ °C.

limited, particularly at high temperature. As depicted in Fig. 3, the leakage caused by the MCU digital core contributes to 50% of the power consumption at room temperature, while the percentage significantly increases to 81% at 85 °C.

The most efficient strategy for leakage avoidance is to switch-off the MCU digital core, either completely or partially [4]. The conventional approach widely used today for mobile application processors is power gating. In this mode, the MCU digital core is switched-off with the help of large power switches inserted into the digital supply rail. The sizing of these switches has to be chosen as tradeoff between leakage reduction during sleep and performance/speed degradation [7]. For state retention of the internal configuration registers, these systems use dedicated retention flip-flops, which remain powered during sleep and continue to cause leakage current. Moreover, the power management unit including the LDO must remain active during sleep adding its quiescent current budget to the total power consumption. Due to these shortcomings, this mode is not realized in the power diagram of the presented MCU system. Fig. 3 shows instead the estimated system power consumption of such a mode exhibiting a leakage reduction by a factor of 1.2–2.6 compared with the low-power state.

An alternative approach to switch-off the MCU digital core is to utilize the on-chip integrated voltage regulator. By considering typical application scenarios, two major system states of ultra-low-power MCU systems can be identified, which can be leveraged for system architecture decisions. In active mode, the processor provides high processing performance while leakage current is only of limited concern. During sleep mode in contrast, the system power consumption needs to be minimized, while commonly only a real-time clock remains active. The fine granularity potentially offered by power gating is thus only of limited benefit for the majority of typical ultra-low-power application scenarios. Instead, the LDO can be completely disabled in sleep mode, thereby using its pass-transistor as power switch. The power consumption in this mode is depicted in Fig. 3. As a high voltage drop is a desired feature of every LDO design, the pass-transistor can be sized significantly smaller than a power switch resulting in a highly improved leakage reduction. This approach, moreover, does not only significantly reduce the leakage of the MCU digital core, but also the power management overhead (see Fig. 3). The major portion of the power management unit (including the LDO) is disabled in this sleep mode. Only a continuous supply voltage supervisor remains active. Since a fast writable FRAM memory is available here, this can be used to store critical register states for being rewritten during next wake-up [1].

In conclusion, disabling the LDO reduces the power consumption during sleep by a factor of 4.3 at room temperature and by a factor of 18.9 at high temperature when compared with the basic low-power state. Compared with power gating, this approach does not only achieve lower power consumption during sleep but also simplifies the system partitioning. No overhead for additional power switches and retention flip-flops is required. The number of supply boundary crossing signals requiring level-shifters and isolation cells is drastically reduced.

As many ultra-low-power applications need a time-base to periodically trigger a wake-up event, a separate subregulated power domain for real-time-clock operation including a low frequency oscillator might remain active adding a power consumption of only 1.8μW (at $V_{\mathrm{DD}} = 3.0$ V and room temperature).

IV. Efficient Switching Between Power Modes

With the benefit of lower power consumption during sleep, another aspect of system energy optimization arises. Each wake-up from sleep mode takes time and needs additional energy. Fig. 4 shows the energy required for wake-up from the previously discussed sleep modes. It consists of three components, which will be discussed in the following.

First, both the power management and the clock generation unit need to be reactivated, depending on the sleep mode either partially or completely. This takes time and needs power resulting in energy lost from the battery (see Fig. 4).

Second, in case the LDO is disabled, not only the power management and clock generation unit need to be reactivated but also the LDO load capacitance needs to be recharged. For the MCU system with an external LDO load capacitance of 470 nF, the energy required for recharging clearly dominates the overall wake-up energy (see Fig. 4). Lowest capacitance at the LDO output is preferred to enable an energy efficient wake-up. As depicted in Fig. 4, the wake-up energy is in this way reduced by a factor of 5.6 for a 3 nF in comparison

with a 470 nF LDO capacitance configuration. In contrast, this LDO load capacitance reduction is in strong contrast to the voltage regulator needs. As will be further discussed in Section VI, the absence of an external capacitance greatly affects the LDO design [8]. The LDO has to be faster and thus needs higher quiescent current when being active.

Third, in case of disabling the LDO, power is removed from the MCU digital core. When exiting from this sleep mode, the system therefore behaves similar to a power-on reset condition. Usually, the energy required for saving and recovering the system state from nonvolatile memory is rather high in flash-based systems. In contrast, FRAM memory offers a $1000\times$ faster write capability at $100\times$ lower energy compared with a typical flash-based system [1], [9]. The usage of FRAM memory in this way enables an energy-efficient data and state retention during sleep (see Fig. 4).

In conclusion, there is a fundamental tradeoff between saved energy during sleep and additional energy required for wake-up. A break-even time can be defined for which it is beneficial to enter a sleep mode with lower power consumption but also higher wake-up overhead, e.g., disabling the LDO instead of setting the power management into low-power state. This tradeoff strongly depends on the sleep time and thus on the application scenario. To experimentally determine the break-even time, Fig. 5 shows the measured energy consumption of the MCU system for a periodic sensor data analysis versus cycle time both at room and high temperature. In this experiment, the MCU system periodically wakes up to perform a sensor data analysis taking 152 clock cycles at an operating speed of 8 MHz. When idle, the MCU system is set into a sleep mode, either into the low-power state or into a complete shutdown with the LDO being disabled. By sweeping the cycle time, i.e., the time between the wake-up events, the break-even point can be determined.

For very short cycle times (<1 ms), the energy consumption is dominated by power consumption in active and wake-up mode. In contrast, it becomes dominated by power consumption during sleep for extended cycle times (>10 s). For comparison, the dashed line represents the system energy consumption for an ideal sleep mode with zero power consumption during sleep and zero energy required for wake-up. For the MCU system with an external LDO load capacitance of 470 nF, the break-even time is 239.3 ms at room temperature. By using a fully integrated LDO with a load capacitance of 3 nF, this time is drastically reduced to 37.8 ms. At high temperature, the break-even time shifts to shorter periods due to increasing leakage current amounting to 30.8 ms for an LDO with external load capacitance and 4.7 ms for a fully integrated LDO, respectively.

The dashed area in Fig. 5 highlights the savings at different wake-up frequencies for a 3 nF in comparison with a 470 nF LDO capacitance configuration. These experimental results are in good agreement with the theoretical considerations, when combining the power consumption during sleep as shown in Fig. 3, the required energy for wake-up as shown in Fig. 4, and the active power consumption as shown by the dashed line in Fig. 5. In conclusion, a fully integrated LDO with a small load capacitance is highly beneficial for a large range of

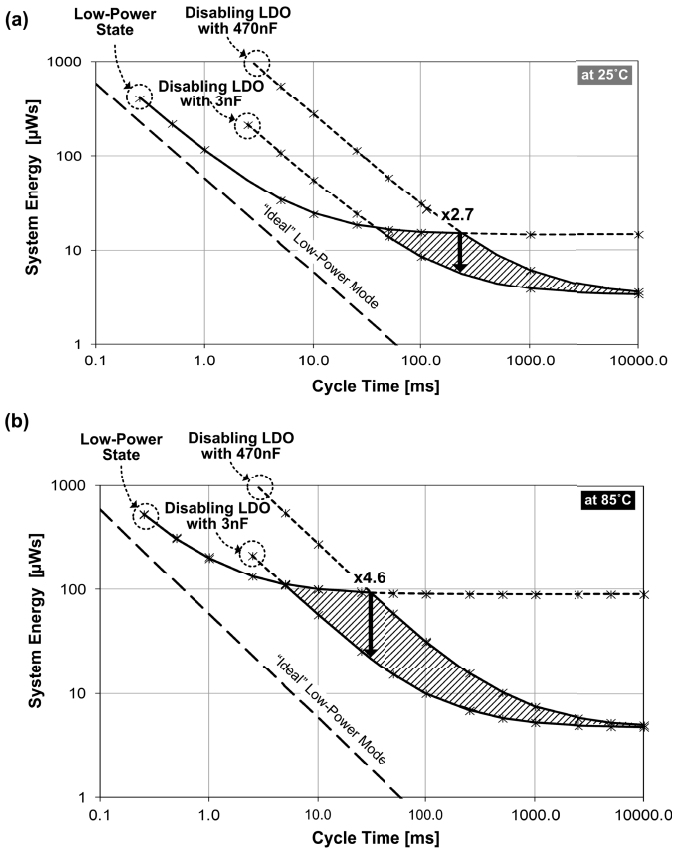


Fig. 5. Measured system energy consumption per cycle for periodically performing a sensor data analysis (taking 152 clock cycles at a clock speed of 8MHz) versus cycle time at $V_{\mathrm{DD}} = 3.0$ V. The dashed area highlights the savings at different wake-up frequencies for a 3 nF in comparison with a 470 nF LDO capacitance configuration at (a) room temperature, and (b) high temperature.

ultra-low-power applications. Thereby, system energy savings of up to a factor of 2.7 at room temperature and up to a factor of 4.6 at high temperature can be achieved, which directly translates into an extended battery lifetime.

V. Energy/Performance Scalability

In active mode, the system power consumption is increased by more than three decades compared with the sleep modes. It seems obvious that faster code execution should help to save energy. However, in many ultra-low-power applications, the speed of processing is gated by external events (e.g., analog settling times). To avoid wasting energy by running idle, the best the system can do is to adapt to the speed of such events.

Fig. 6 shows the measured system energy consumption of the demonstrator systems shown in Fig. 2 for performing a sensor data analysis versus clock speed at $V_{\mathrm{DD}} = 3.0$ V and room temperature. For this experiment, the code is executed from the on-chip static RAM (SRAM) memory; the system clock is provided from external. For the demonstrator systems, no dynamic voltage frequency scaling techniques are employed. Instead, the core supply voltage V_{CORE} is 1.52 V, decided as trade-off between maximum speed/performance requirements on the one side and active power considerations on the other side. When considering the energy consumption of the MCU digital core only, as indicated by the shaded area in Fig. 6, the energy

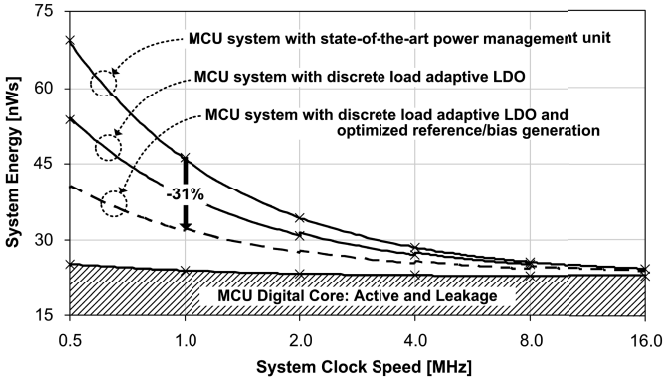


Fig. 6. Measured system energy consumption for performing a sensor data analysis (taking 152 clock cycles) versus system clock speed at $V_{DD} = 3.0$ V and temperature $= 25$ °C.

per cycle is thus basically independent of the clock speed. It is dominated by the active switching energy while the energy overhead introduced by leakage can be neglected for the operating frequency range of interest. This is in contrast to the energy overhead introduced by the power management unit. A state-of-the-art power management unit, as introduced in Fig. 2(a), must be laid out for worst-case power requirements at maximum performance level. Its power consumption does not scale with the system operating speed and hence becomes dominant when operating at low clock speed, i.e., when being active for a longer time period. It contributes to 47% of the total system power consumption when operating at a clock speed of 1 MHz. To solely determine the clock speed by application requirements without sacrificing system energy consumption, the power management unit clearly needs to be optimized for all potential speed requirements.

The above-described picture changes for an MCU system employing dynamic voltage frequency scaling. When focusing on the MCU digital core only, a minimum energy point can be identified in the subthreshold regime when operating at very low clock speeds [10]. However, when considering the overall MCU system, particularly including the power management overhead, the minimum energy point moves to higher system operating speeds and supply voltages. Although this is a very interesting aspect of system energy optimization, it would go beyond the scope of this paper.

VI. Discrete Load Adaption Scheme

According to the above discussion, the LDO must combine a high current efficiency under all load conditions with a small integrated capacitance at the LDO output to enable a highly flexible and energy-efficient system operation. At the same time, the LDO output voltage must remain within a certain tolerance window (here $+30/-70$ mV) under all operating conditions to guarantee fault-free operation of the MCU digital core. In this context, the rapid load current transients presented to the LDO when starting and stopping system operation add another level of complexity [8].

State-of-the-art LDOs are not optimized for such application requirements. First, the absence of a large external capacitance presents several design challenges for stability and transient behavior of an LDO, leading to an increased quiescent current demand [8]. Most of the known fully integrated LDO topologies use some form of Miller compensation to establish an internal dominant pole and suffer from stability issues in low load conditions [11]. In addition, the LDO quiescent current dominates the overall system current when operating at low digital current consumption (see Fig. 6). For this reason, some MCU systems use multiple LDOs [6], each optimized for a dedicated load condition, resulting in slow transition times between these load conditions. In [12], the quiescent current of a single LDO is scaled by sensing the load current. Due to reaction time of the sensing loop, this LDO requires a large capacitance to suppress large transient undershoots.

To reconcile these contradicting LDO design requirements, a discrete load adaptive LDO scheme was first proposed in [5] and will be presented in the following. By making use of known system power information, this LDO digitally adapts its maximum current drive capability. While for a stand-alone LDO, the actual load is unknown, this is different for an LDO supplying a digital core as part of a fully integrated MCU system. Once the system is active, the current consumption of the MCU digital core is clearly dominated by the dynamic switching of the CMOS logic gates. The leakage current in contrast can be neglected for the operating frequency range of interest. The LDO load current can thus be predicted as

$$I_{\mathrm{LOAD}} \cong \sum_{i=1}^{k} (\alpha_i \cdot C_i) \cdot f_{\mathrm{CLK}} \cdot V_{\mathrm{CORE}} \tag{2}$$

where $(\alpha_i \cdot C_i)$ is the effective switching capacitance, f_{CLK} is the system clock speed, and V_{CORE} is the core supply voltage. While some of these parameters are hard to determine (i.e., the effective switching capacitance), other parameters can be easily determined on system level during operation. As the clock speed in a fully integrated system is known from the settings of the internal oscillators, this information is used here to digitally adapt the maximum LDO current drive capability. The LDO quiescent current in turn scales linearly with the maximum current drive capability (with an offset of 100 nA for the bias network). As evident from the system block diagram in Fig. 2(a), a simple control unit is used here to map the clock speed information into a required discrete LDO drive capability level. By using a look-up table approach, it can be chosen from six discrete, binary scaled current drive levels (CDLs) as introduced in Fig. 7. In the lowest level (CDL1), a quiescent current of 650 nA is needed, while in the highest level (CDL6) the quiescent current is 17.7μA and a load current of up to 2.56 mA can be provided. In this way, the current efficiency remains above 97% over two decades of load current (see Fig. 7). As a positive side effect, a dedicated low-power LDO required in the state-of-the-art power management unit becomes redundant.

For the discrete load adaptive LDO scheme, in conclusion, the actual analog feedback loop gets enhanced by employing digital information. This information (namely about system clock speed) is known in advance, which allows the LDO to get prepared for the new load conditions rather than need to react. During MCU operation, the system clock speed may

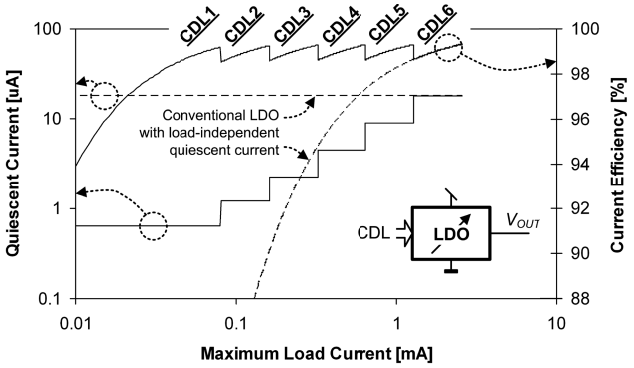


Fig. 7. Measured LDO quiescent current at VDD = 3.0 V, T = 25 °C and current efficiency $I_{\mathrm{Load}}/(I_{\mathrm{Load}}+I_{\mathrm{q}})$ versus maximum load current. Compared with a conventional LDO with load-independent quiescent current (dashed lines), the current efficiency is highly improved in light load conditions.

change within one clock cycle (60 ns at maximum speed) by switching the clock source or setting a clock divider. This is the worst-case time for setting the LDO to a new drive level (CDL) and thus being prepared for new load current requirements. For highest system flexibility, arbitrary and instantaneous switching between any levels is allowed while keeping the output voltage within the tolerance window necessary to guarantee fault-free operation of the MCU digital core (+30/−70 mV).

By employing the discrete load adaptive scheme, the energy required for executing a certain code can be strongly reduced for low clock speeds (see Fig. 6). The dashed line shows the estimated energy consumption when the power optimized reference and bias generation circuitry is used not only during sleep but also in active mode. In this way, the energy per cycle becomes almost independent of the clock speed. The clock speed can now be solely determined by application requirements without sacrificing system energy consumption.

VII. LDO Circuit Implementation

Fig. 8 shows the LDO circuit implementation that is based on the multiple-loop topology presented in [13]. This LDO topology achieves high gain and large bandwidth by combining two stages in two control loops: A slow folded-cascode (EA_1) with high gain and a pole P_0 at its output is combined with a fast, low gain voltage follower (VF_1). The voltage follower is formed by the common-gate transistors M_{CG1} and M_{CG2}, the current mirror M_{CM2}, the resistor R_1 as well as the pass-transistor M_{PASS}. The two control loops are combined at M_{CG1}. The LDO topology is compensated by an active feed-forward compensation scheme [14], which can be best shown by considering the LDO open-loop transfer function $H(s)$. It results from superposition of the transfer function of the slow feedback loop as well as that of the fast feedback loop. An open-loop analysis thereby requires the cut of both feedback loops

$$H(s) = -\frac{\left(\left(A_{\mathrm{v,EA1}}+1\right)\cdot A_{\mathrm{v,VF1}}\cdot A_{\mathrm{v,PASS}}\cdot\left(1+\frac{s}{\left(A_{\mathrm{v,EA1}}+1\right)\cdot\omega_{p0}}\right)\right)}{\left(1+\frac{s}{\omega_{p0}}\right)\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}. \tag{3}$$

The overall open-loop transfer function $H(s)$ possesses three poles and one LHP-zero, which arises due to the summation of the two feedback loops. The first dominant pole P_0 is associated with the output of the folded-cascode. By introducing a capacitance at this node, the pole is designed to reside at very low frequencies. The fast feed-forward path introduces a LHP-zero Z_0 to the LDO open-loop transfer function $H(s)$. The hereof arising positive phase shift is used to shape the LDO frequency response, in particular to cancel the negative phase shift of the first dominant pole P_0. Evaluating the numerator of the open-loop transfer function $H(s)$ yields the frequency of the zero

$$\omega_{z0} = \left(A_{\mathrm{v,EA1}}+1\right)\cdot\omega_{p0} \cong A_{\mathrm{v,EA1}}\cdot\omega_{p0}. \tag{4}$$

A second dominant pole P_1, located at the LDO output, widely moves with load current due to changing output impedance of M_{PASS}. It ranges between P_0 in no load condition and P_2 in maximum load condition. The pole P_2 is defined by R_1 and the gate capacitance of M_{PASS}. In this way, the LDO loop stability becomes a free design parameter. The pole P_2 can be pushed to higher frequencies by reducing the resistance R_1, thereby improving loop stability at high load. This, however, comes at the cost of an increased LDO quiescent current. As evident from the simulated bode-plot shown in Fig. 9, this trade-off is here balanced in favor of low LDO quiescent current, accepting a worst-case phase margin of 30°. Due to the pole-zero cancellation, this topology, however, does not need further frequency compensation to ensure proper phase margin under all load conditions [14].

The unmatched pole-zero cancellation is also well evident in the LDO transient response. The fast voltage follower (VF_1) allows the LDO to instantaneously react to load changes but with limited gain only. Subsequently, the output level slowly settles back to the accurate DC level determined by the slow folded-cascode (EA_1) providing high gain. As an LDO designed for supplying digital circuits aims to maintain the output voltage within a specified tolerance window, a slow settling at the LDO output can, however, be tolerated for this application.

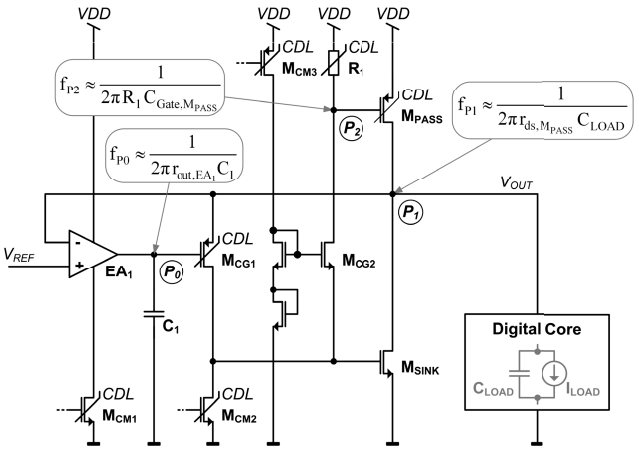


Fig. 8. Simplified circuit diagram of the LDO. The current mirrors M_{CM1}, M_{CM2}, and M_{CM3}, the common-gate transistor M_{CG1} and the resistor R_1 are controlled depending on the current drive level (CDL).

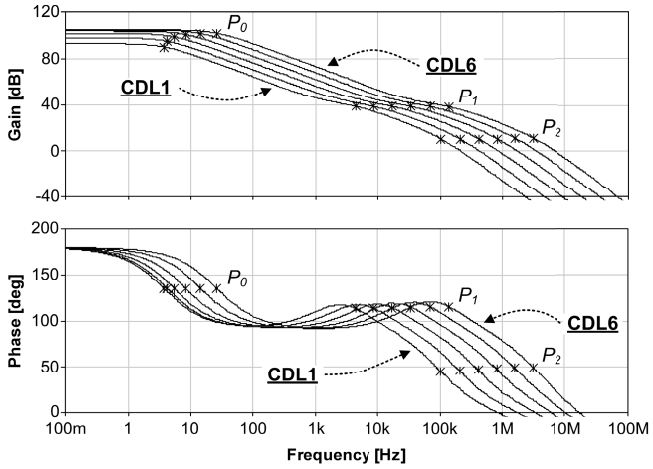


Fig. 9. Simulated Bode-plot for each CDL at the respective maximum load current. The bandwidth of both LDO control loops is adapted while stability for each CDL is ensured.

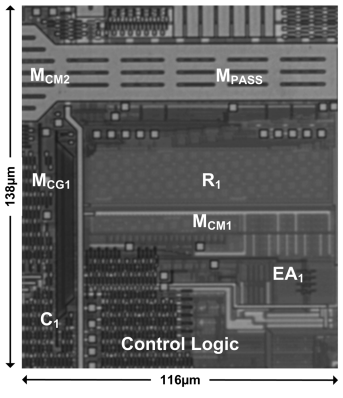
For the discrete load adaption scheme, both the folded-cascode and the voltage follower are biased depending on the drive level (CDL) by adapting the mirror ratio of M_{CM1}, M_{CM2}, and M_{CM3}. In this way, the bandwidth of the LDO control loop is adapted. As shown in Fig. 9, all relevant poles move simultaneously ensuring loop stability for each CDL. To maintain the operating points of the circuit, the active width of M_{CG1} and M_{PASS} as well as the resistance of R_1 are adapted. Care is taken in the switch design to avoid dynamic effects such as charge injection and feed-through of the digital control signals. In this way, the LDO output voltage is kept within the specified tolerance window while switching the LDO CDL.

VIII. Experimental Result

The LDO is implemented as part of a complete ultra-low-power MCU system in a 0.13 μm digital CMOS process. Both supply voltage range (V_{DD} = 1.9–3.6 V) and output voltage (V_{CORE} = 1.52 V) are determined by system operating conditions as introduced in Section II. To guarantee a fault-free operation of the MCU digital core, the output voltage must remain within a tolerance of +30/−70 mV. Reference voltage and bias current are provided by an on-chip reference circuit, employing sampling techniques for ultra-low-power consumption [9]. For the majority of time, the high accuracy reference is disabled, and the bias voltages are stored on sampling capacitors. To ensure stable bias conditions, the sampling capacitors are frequently refreshed, thereby enabling the high accuracy reference only for a short time. For test purposes, DC load current profiles with fast rise and fall times of 1 ns can be generated on-chip. The die micrograph is shown in Fig. 10; the LDO occupies an area of 0.016 mm^2. Its key performance parameters are summarized in the table. The presented, digitally enhanced LDO achieves a figure-of-merit (FOM) of 8ps following the definition in [8]. Moreover, owing to the discrete load adaption scheme, the contribution of the LDO to the overall system power consumption is smaller than 3% down to clock speeds of less than 0.5 MHz. For system energy optimization considerations (e.g. selecting the optimum clock frequency for the application), its contribution can therefore be neglected.

Fig. 11(a) shows the measured LDO behavior when a DC load current step from 0 to 2.56 mA is applied under worst-case conditions (V_{DD} = 1.9 V, Temp = –40 °C) while the LDO is in the highest CDL6 with a quiescent current of 17.7μA. The transient voltage errors of –27 mV and +15 mV (black curve) are well within the tolerance window. For comparison, when applying a load current step from 0 to 0.08 mA only, the LDO is unnecessarily fast, and the tolerance window is not utilized (gray curve). As evident from the measurement in Fig. 11(b), the LDO can thus be slowed down to the lowest current drive level CDL1 achieving a quiescent current of 650nA. Fig. 11(c) shows the measured LDO behavior when switching between the lowest and the highest current drive levels (CDL1 and CDL6, respectively) at no load current under worst-case conditions for this experiment (V_{DD} = 3.6 V, T = 85 °C). By keeping the load current constant for demonstration purposes, it can be distinguished between the output voltage fluctuation induced by the LDO load current response as well as by the drive level adaption. While the output voltage is ideally expected to remain constant, transient voltage errors of –6 mV and +14 mV can be nevertheless observed, caused by internal settling effects when switching the LDO drive level. After the drive level switching, the LDO instantly achieves its new load current drive capability as demonstrated by Fig. 11(d). Here the drive level is switched while simultaneously a load current step from 0 to 2.56 mA is applied. The maximum transient voltage errors of –32 mV and +17 mV are well within the limits. These experiments also prove the LDO stability under worst-case operating conditions.

Fig. 12 shows the measured LDO transient behavior when the digital core is operated at an alternating clock speed of 0 and 16 MHz with an active current consumption of 840μA under nominal conditions (V_{DD} = 3.0 V, T = 25 °C). As shown in the inset, the digital core activity causes a voltage ripple of only 14 mV. As an LDO designed for low quiescent current is too slow to react to single current spikes, the



	CDL1	CDL6
Technology	0.13µm	
Active Area	0.016mm²	
Temperature Range	-40°C - 85°C	
Supply Voltage Range	1.9V - 3.6V	
Nom. Output Voltage	1.52V	
Load Capacitance	3nF	
Maximum Load Current	0.08mA	2.56mA
Quiescent Current	0.65µA	17.70µA
DC Offset (sim. 3σ)	19mV	10mV
Line Regulation	1.4mV/V	1.3mV/V
Load Regulation	<10µV/mA	<10µV/mA
Load Tran. Undershoot	27mV	27mV
Current Efficiency	99.2%	99.3%
FOM*	0.008ns	

*) Adopted from [8]: $FOM = \frac{C_{LOAD} \cdot \Delta V_{OUT}}{I_{LOAD}} \cdot \frac{I_{q(min)}}{I_{LOAD}}$

Fig. 10. Chip micrograph showing the digitally enhanced LDO. The LDO is implemented as part of a complete ultra-low-power MCU system in a 0.13 μm digital CMOS process.

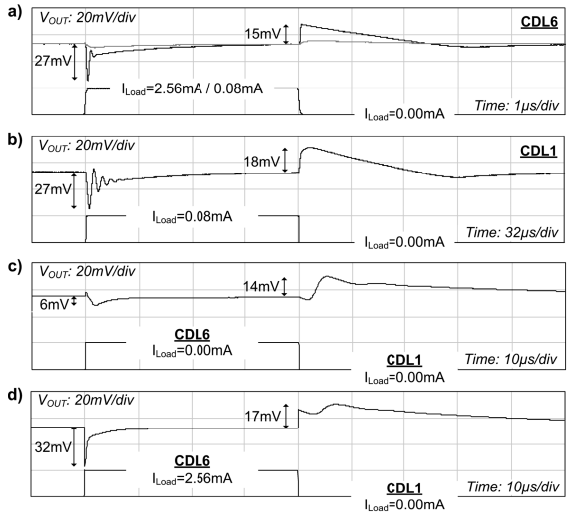


Fig. 11. Measured LDO transient behavior in response to a worst-case load transient step (a) in the highest current drive level CDL, and (b) in the lowest current drive level CDL1; as well as when switching between the lowest and highest drive levels (c) at no load current, and (d) while simultaneously applying a worst-case load current step. The upper curve always shows the LDO output voltage; the lower curve shows the load current.

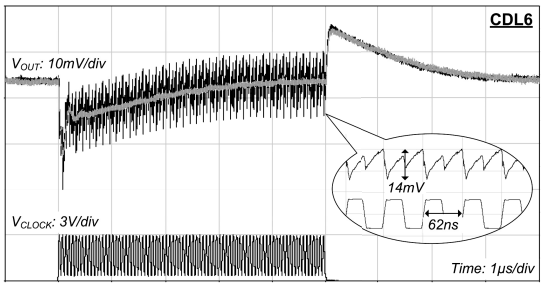


Fig. 12. Measured LDO transient behavior while the MCU digital core is operating at an alternating clock speed of 0 and 16 MHz (black curve). The gray curve shows a similar DC load current step.

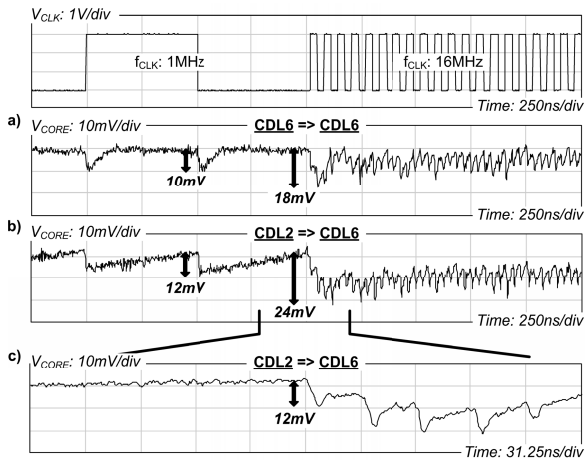


Fig. 13. Measured LDO transient behavior while the MCU digital core operates at an alternating clock speed of 1 and 16 MHz at $V_{DD} = 3.0$ V, $T = 25$ °C. The discrete load adaption scheme is (a) disabled for demonstration purposes, and (b) enabled to exploit the LDO quiescent current benefits at low clock speeds, with (c) showing a zoom of the dynamic drive level adaption.

charge needed during one clock cycle is mostly supplied from the internal capacitance of 3 nF. To limit this voltage ripple, a certain minimum on-chip capacitance is consequently required. For comparison, a DC load current step from 4 to 840μA is applied (gray curve). The average LDO output voltage and the maximum errors in both cases are the same. This proves that the experiments shown in Fig. 11 represent worst-case conditions not only for DC load conditions but also for applicative conditions when supplying the MCU digital core.

To prove highest system flexibility, experiments with LDO operation for arbitrary and instantaneous switching between any levels are shown in Fig. 13. To begin with, the dynamic LDO drive level adaption is disabled for demonstration purposes. Instead, the LDO is constantly operated in the highest drive level CDL6 with a quiescent current of 17.7μA. Fig. 13(a) shows the measured LDO transient behavior while the MCU digital core operates at an alternating clock speed of 1 and 16 MHz. The increasing load current requirements cause a maximum transient voltage error of 18 mV. Clearly, the LDO is unnecessarily fast when operating at a clock speed of 1 MHz. The output voltage is able to fully settle back to its nominal value in response to the current spike occurring at each clock edge. In contrast, the dynamic LDO drive level adaption is enabled for the experiment shown in Fig. 13(b). Here, the MCU digital core operates at an alternating clock speed of 1 and 16 MHz while the LDO is in the drive level CDL2 with a quiescent current of 1.2μA and in the drive level CDL6 with a quiescent current of 17.7μA, respectively. Switching the CDL and increasing load current requirements cause a maximum transient voltage error of 24 mV, which is well within the maximum LDO tolerance window of $+30/-70$ mV. It is worthwhile to note that the voltage ripple caused by the digital activity is almost independent of the drive level selection. This experiment in this way once more shows that the charge needed during one clock cycle is mostly supplied from the internal capacitance of 3 nF.

IX. Conclusion

We have shown that power management in all system conditions, addressed in the context of the application, is a key requirement for lowest energy systems. A holistic design approach thereby outperforms the traditional circuit design based on analog/digital partitioning and leaves much more flexibility for system energy optimization. The key is a digitally enhanced LDO with multiple CDLs, controlled depending on the power demand of the MCU digital core. By combining high LDO current efficiency under all load conditions with a small integrated capacitance at the LDO output, this regulator enables a highly flexible and energy-efficient system operation. In this way, the presented power management solution combines ultra-low-power consumption during sleep with an energy efficient wake-up enabling system energy savings by up to a factor of 4.6. It is highly flexible thereby maximizing the battery lifetime for a broad range of application scenarios while achieving lowest system cost.

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