Devices operating in the subthreshold region show a reduction in energy because the switching activity decreases with supply voltage. However, the propogation delay increases in this region and this gives rise to leakage currents which cause energy dissipation. There exists an optimal operating point in the subthreshold region at which devices can operate. This point can be found through a minimum energy analysis technique in which the energy is plotted against the supply voltage as the voltage is scaled down. Wang and Chandrakasan implemented this idea in a FFT processor to demonstrate how devices can operate in subthreshold regions. Logic elements have to be specifically modified to be catered for subthreshold operation to avoid leakage current. Parallel leakage is a major contributor to leakage current and it occurs when the idle current is comparable to the drive current in circuits. This effect can be mitigated by having reducing or balancing the number of parallel devices in the pull up and pull down path to avoid leakage. Devices should avoid being stacked as this reduces the effective drive current of each transistor in a stack.

RAM blocks usually contain six transistor (6T) scheme to enable reading and writing of data. Wang and Chandrakasan have demonstrated that subthreshold conditions make read and write operations harder as they place a sizing constraints on the transistors used. There are also other considerations such as bitline leakage that comes into effect when operating in this region. Therefore, an alternative structure to the RAM is needed to address this problem. In the FFT processor, the RAM uses tristate inverters to create a latch and this is used for write operations. The read operation uses parallel tristate gates and a hierarchical read bitline to mitigate parallel leakage.

Therefore, it can be observed that operating in the subthreshold region can help in energy savings but only if the logic is suitably catered for it. Designers might have to construct subthreshold libraries if they want their devices operating in this region. The gains in the long run are satisfactory as it results in an energy efficient device. The subthreshold FFT chip that was made was found to be ``350 times more energy efficient than the low-power microprocessor implementation’’.