Over the years researchers have come up with different techniques to mitigate energy loss due to memory. Recently, a proposal for an adaptive cache structure has been raised for mobile processors. The L2 cache has been found to have access patterns that are not correlated or balanced and therefore there is scope to dynamically adjusting the cache to match the application using it. The compiler does an offline analysis of the application before run-time to determine parameters such as global average miss rates and access rates. Cache access is also monitored during run-time and the run-time information in conjunction with the offline material is used to enlarge or decrease the size of the cache dynamically depending on the need. This proves useful as memory is used much more efficiently. Also, the leakage power is reduced as there are fewer idle cells. This technique was found to give a 13% - 29% reduction in power consumption (using benchmark programs) but there was a small trade-off for speed and area to incorporate this.

Another technique to reduce power is memory compression. Here, a part of the data in volatile memory is compressed in order to reduce the number of logic elements that have to be self-refreshed when a device is turned into a low power state. Rest of the memory can be powered off and therefore the battery life is extended. When there is a request to put a device into a low power state, the memory compression logic takes blocks from a designated memory, compresses it using a compression algorithm and then stores these blocks back to memory. A decompression procedure is followed when the device is in the active state. The compression logic can be implemented in hardware or software and induces some overhead on the battery while performing compression but the power saved by compressing data outweighs this overhead.

Non-volatile memories are another area of interest for power reduction and even in performance enhancement. Resistive Random Access Memory (RRAM) is a piece of memory that could be used as a substitute for SRAMs on mobile devices. It was found that an RRAM with a crosspoint structure that uses a diode as a select cell reduces leakage current. This is because the resistance goes up as voltage decreases and the leakage current paths are cut-off. This structure is also area efficient as multi-layered structures can be made. Investigation is still going into this area as peripheral circuit design is harder if RRAMs are used but it could be used as a technique to reduce energy and power.

Many other techniques can be used to reduce power. An Intel processor for mobile devices reduces the leakage power in the L2 cache. The data arrays in the cache continue to be in the ‘sleep’ mode until a ‘Hit’ signal is generated. Even when there is a hit, only the relevant data array is charged so that it can be activated while the other arrays continue to be in the low power mode. This is a memory partitioning technique and is widely used to mitigate leakage power.