Department of Computer Science & Engineering,
National Institute of Technology Rourkela

3rd Sem B.Tech (End-Semester Examination, Autumn 2022-23)

Subject:**Digital System Design** Subject Code:**CS-2001**

Full Marks:**50** Duration:**3 Hours**

Answer all questions. This paper contains one page.

Figures at the right margin indicate marks. All parts of a question must be answered at one place.

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1. (a) Construct a JK flip-flop using a D Flip-flop, a 2-to-1 line multiplexer and an inverter. [3]

   (b) Design a Mod-5 ripple counter using T flip-flops. [3]

   (c) An 8×1 Multiplexer has inputs A, B, C connected to the selection inputs S_2,S_1,S_0. The data inputs I_0 through I_7 are as follows: [3]
   $I_1 = I_2 = 0$, $I_3 = I_5 = I_7 = 1$, $I_0 = I_4 = D$, $I_6 = D'$. Determine the boolean function.

   (d) State the difference between a Mealy and Moore machine. [1]

2. (a) Design a sequential circuit with D Flip-Flops, A and B, and one input x. [5]
   When x = 0, then the state of the circuit remains the same. When x =1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats..

   (b) Write the Verilog description (Dataflow) of a two to 4 line Decoder. [3]

   (c) Show the characteristic equation of complement output of J-K FF. [2]

3. (a) Design a four input priority encoder with inputs D_0 to D_3. Input D_0 have the highest priority and D_3 have the lowest priority. [4]

   (b) What is state reduction and state assignment? Explain with an example. [3]

   (c) It is necessary to generate six repeated timing signals T_0 through T_5 using. Design the circuit using a counter and a decoder. [3]

4. (a) Design a sequence detector using T flip-flop to detect the sequence 1100 using Melay machine. One bit overlapping is permitted. [6]

   (b) Draw the logic diagram of a 4 bit synchronous down counter using JK FF . [3]

   (c) How many flip flops are required to generate 6 states in a twisted ring counter? [1]

5. (a) Carry out the following flip-flop conversions. [4]

      i. T to D

      ii. SR to JK.

   (b) Design a one input, one output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's compliment at the output. The circuit can be reset asynchronously to start and end the operation. [4]

   (c) Draw the timing diagram for a 4 bit PISO shift register for an input string of 1010. [2]

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