

Magic VLSI - theory

part-1

```
$ magic -T scmos  
$ Ctrl + Z to kill  
$ magic -T scmos& (to run in the background)  
$ magic -T scmos filename.mag & ( to open a preexisting file)
```

- Magic has two windows - command window and canvas
- Enterring commands -

1. Magic command window -

% grid on

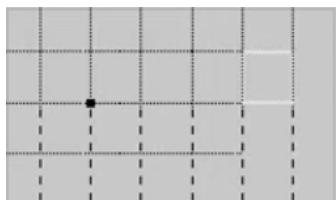
Alternate : Keep the four directional cursor on the layout + press G

Z - for zoom out

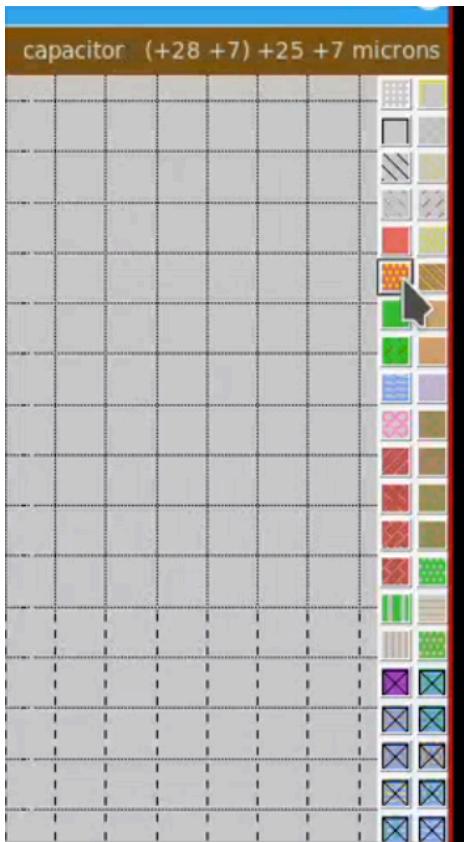
Shift + z - zoom in

2. Second way of entering commands is by keeping the canvas/layout window active and pressing colon (:) in the command window

- Options > Tech manager > scmos
- To close the command window -: exit
- General info -



Black dot at (0,0)

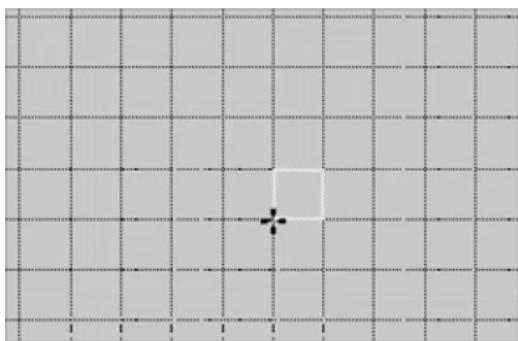


RHS : pallets (switch it ON/OFF in Options > Toolbar)



DRC - Design Rule Check (Green - OK + proceed)

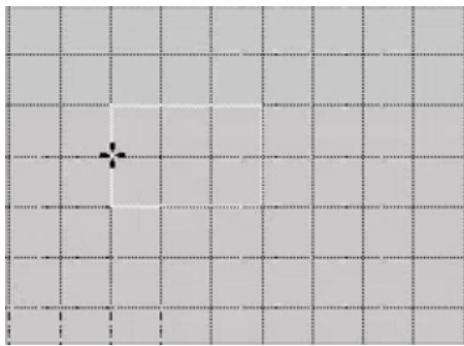
Check for minimum dimensions and spacing between geometrical objects



Cursor + left click-> anchors that particular spot

Cursor + right click after above step -> to select given area

Example - 3x2 dimension

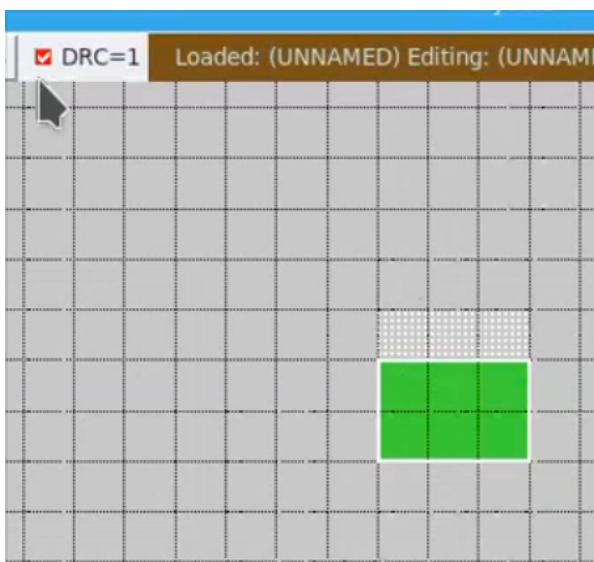


Paint the selected area by choosing from palette

Ex: green - for n diffusion

Alternate: place the cursor in the selected area, go to command window and press ' : '

: paint ndiff



Gray area corresponds to the substrate (P)

Top view is visible on the canvas

Dotted rectangular area = error (also notice red check next DRC - 1 DRC violation)

: drc find

```
texthelper updatedisplay uplevel upsidedown upvar  
Unknown macro or short command: 'XK_q'  
: paint ndiff  
: drc find  
Error area #1:  
N-type Diffusion width must be at least 3 (MOSIS rule #2.1a)
```

To remove any layer, pick that area (white outline) and click anywhere on the substrate.

To move a selected area:

Click on it -> gets white outline

: select area

Now the outline can be freely moved by using command window-

: move e 1

(move east by 1 unit)

Press ' .' to run the same command again

To get specific help with commands -

% help (general)

% help move (will give all move related commands)

% help select

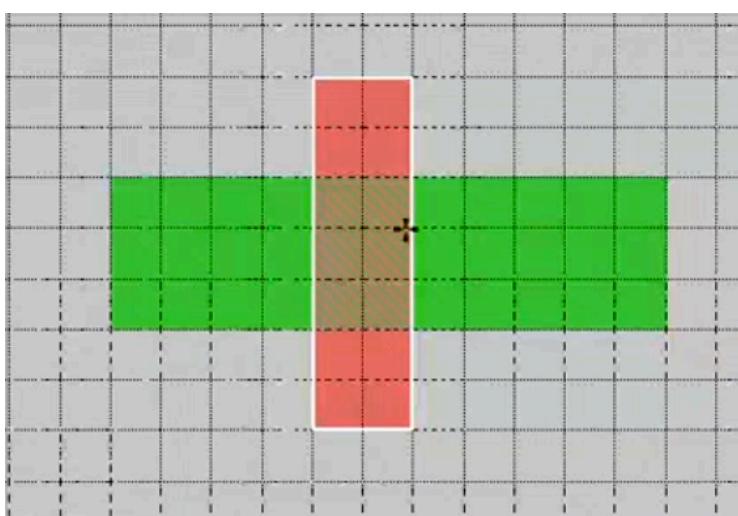
% select help

- Designing NMOS -

After paint ndiff

Poly -

: paint poly



Pure red - poly overhang

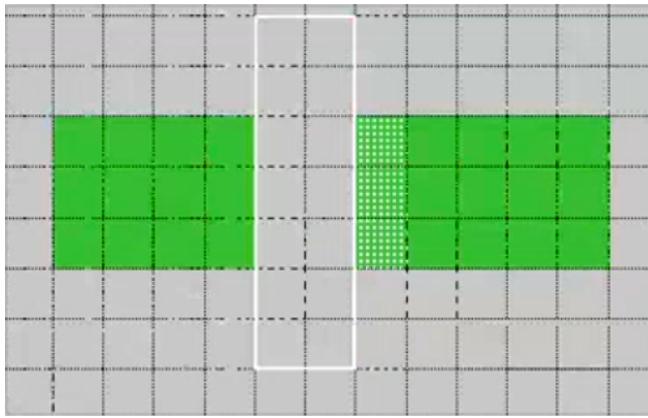
Green + red - gate

- To selectively only remove poly -

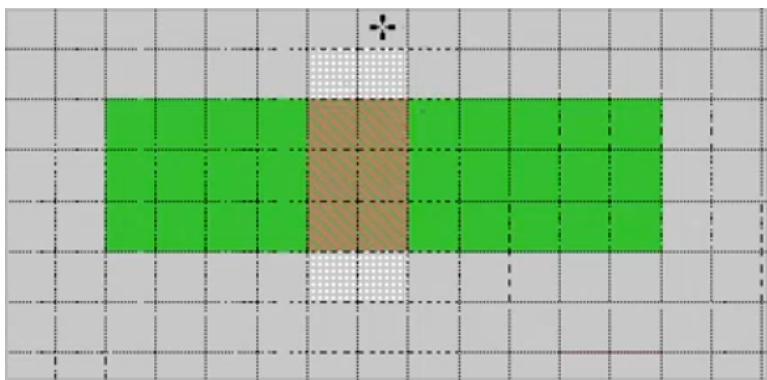
: select area poly

(syntax - select area layer)

: erase



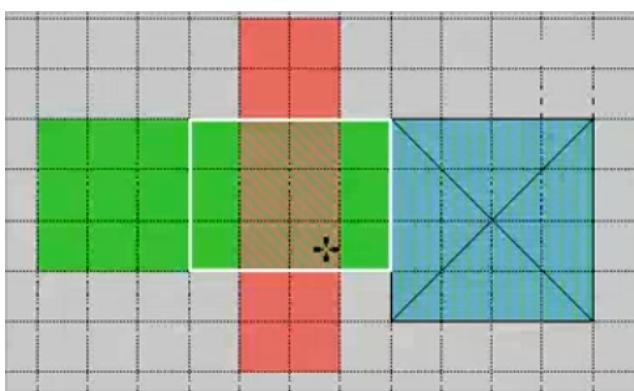
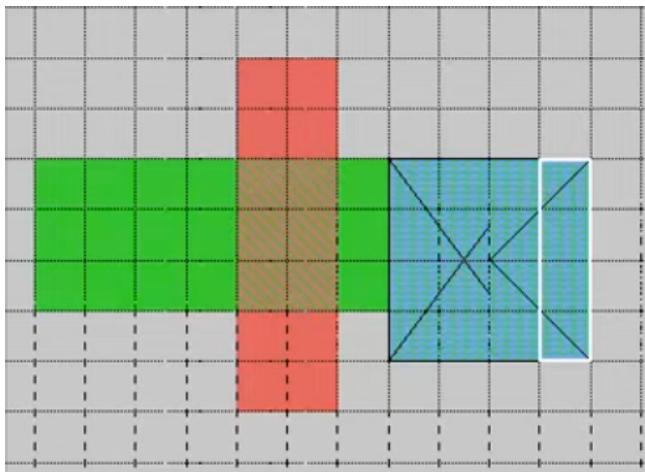
Method 2 : Instead of erase -
: delete (after selecting)



Gate area still remains
Now to remove this -
: select area nfet
: delete

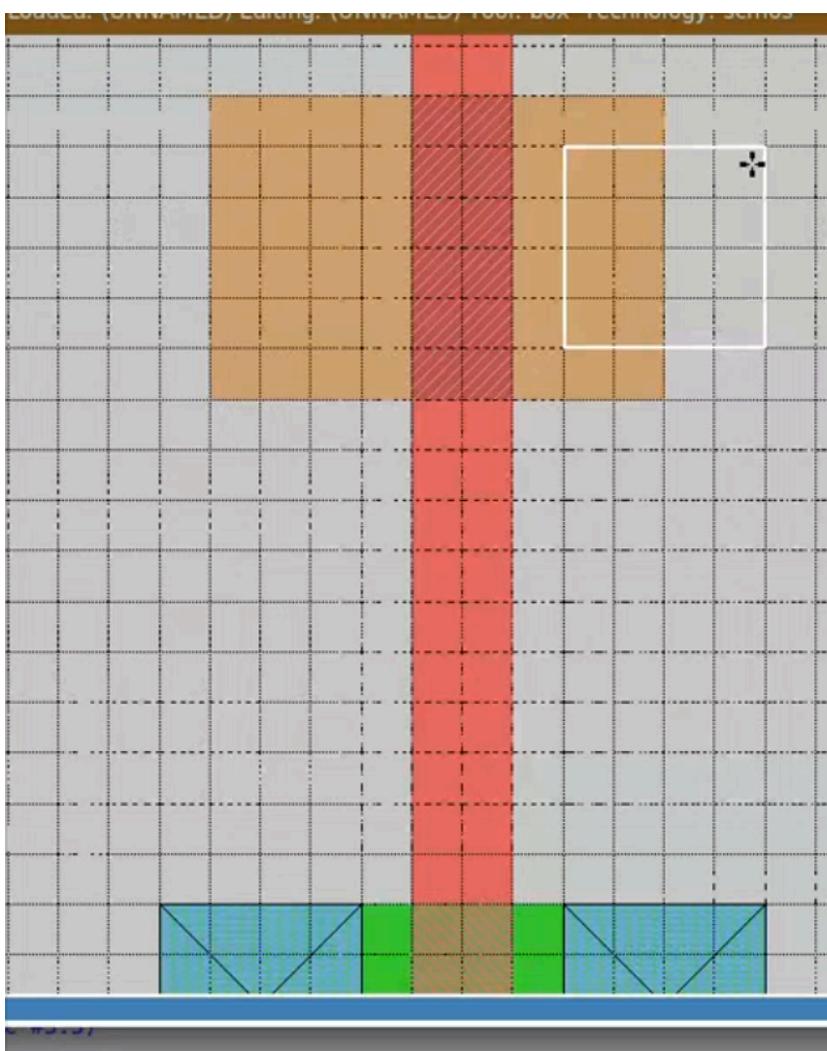
Note - width of nmosfet (green) = 3 grids = 3λ
Length = 2 grids = 2λ (p.s. the remaining green area is Source and drain)

Add contacts -
: paint ndc
(N diffusion contact)

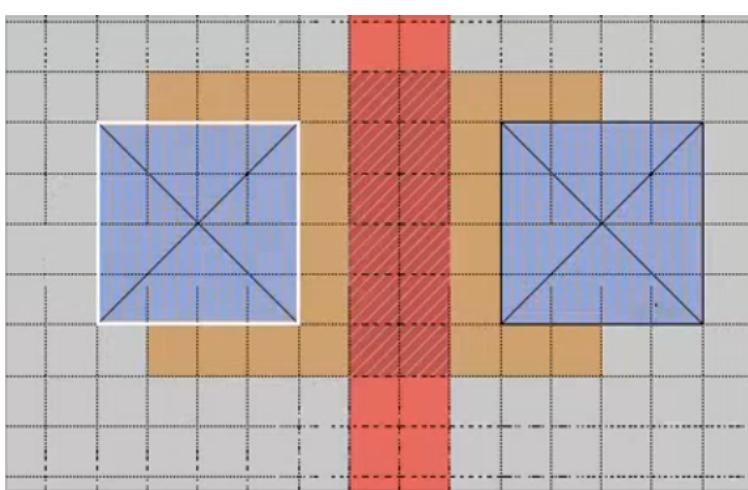


Replicate contact on lhs

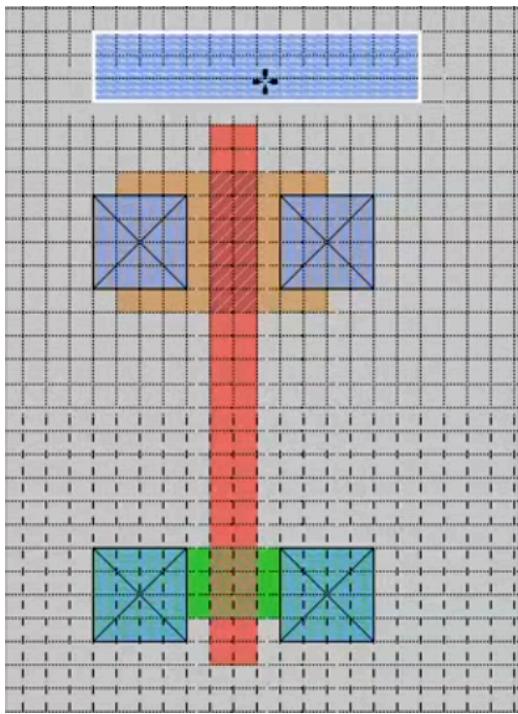
PMOS - diff has to be twice the size of ndiff



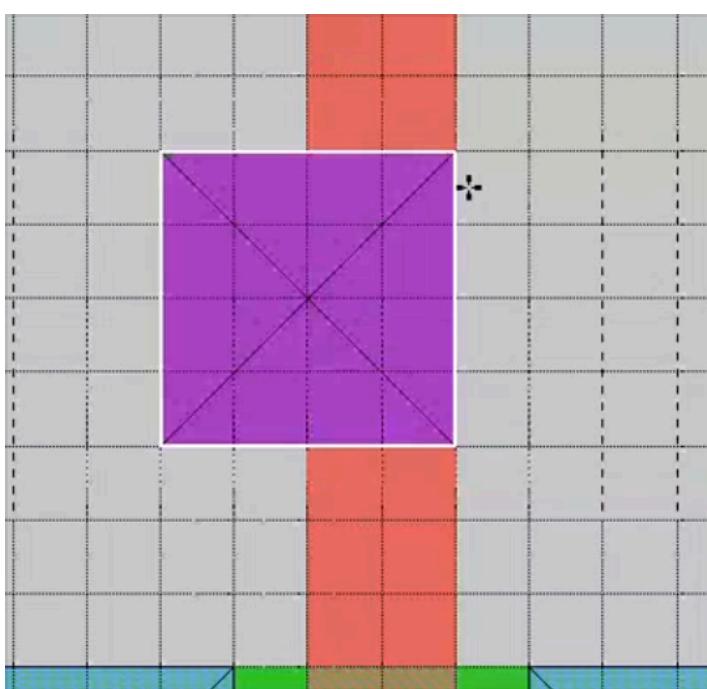
: paint pdc



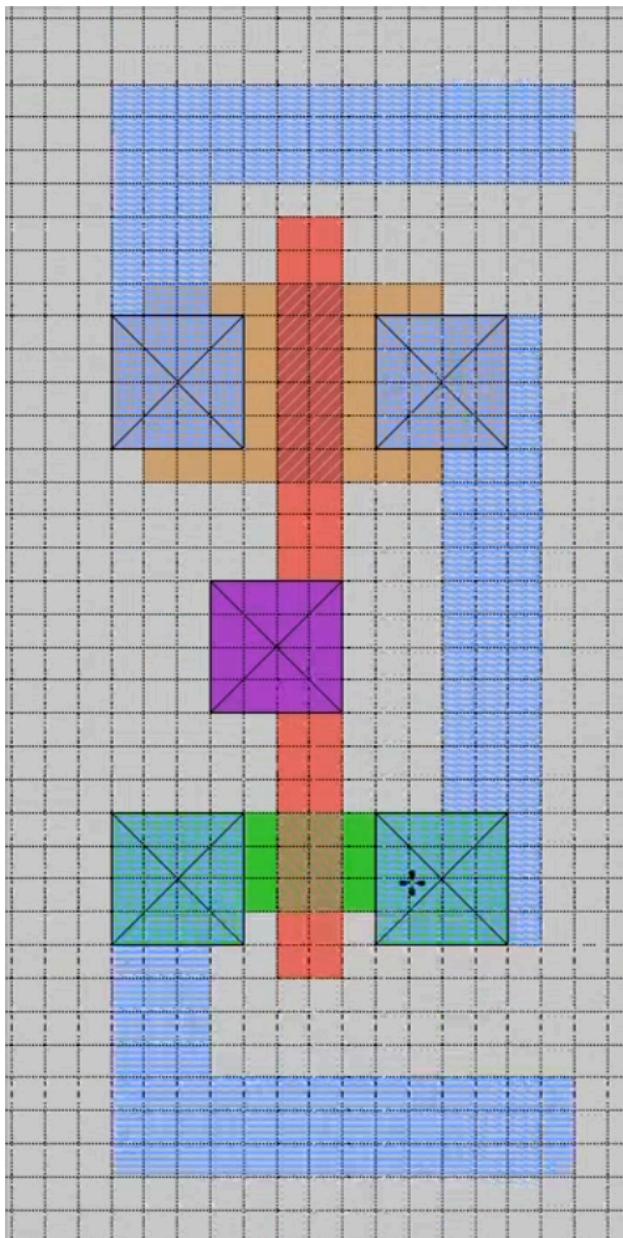
: paint m1
(Metal 1)



: paint pc
(Poly contact)

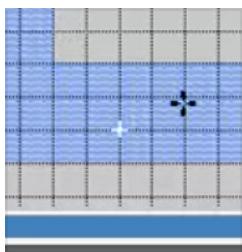


Inverter -



Labelling -

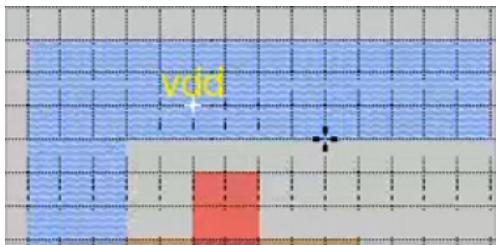
Click a point on the area, then in command line -



Syntax => :label str [pos [layer]]

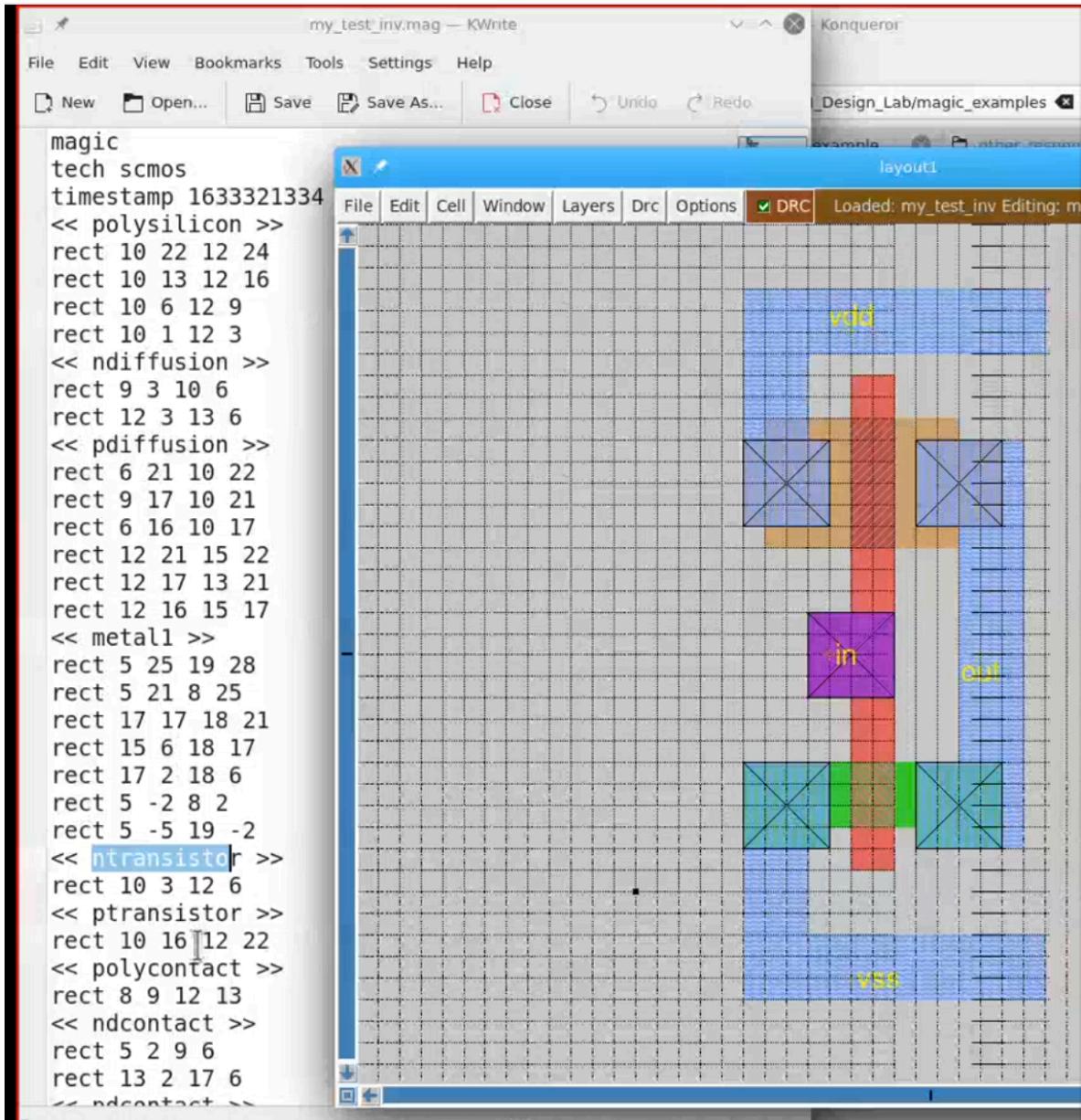
:label vdd n

(n - north of point selected)



- Saving the file -
: save filename.mag

part2



Converting these rect components to electrical components -
% extract

Ext file to spice netlist -

% ext2spice

my_test_inv.spice — KWrite

File Edit View Bookmarks Tools Settings Help

New Open... Save Save As... Close Undo Redo

```
* SPICE3 file created from my_test_inv.ext -
technology: scmos

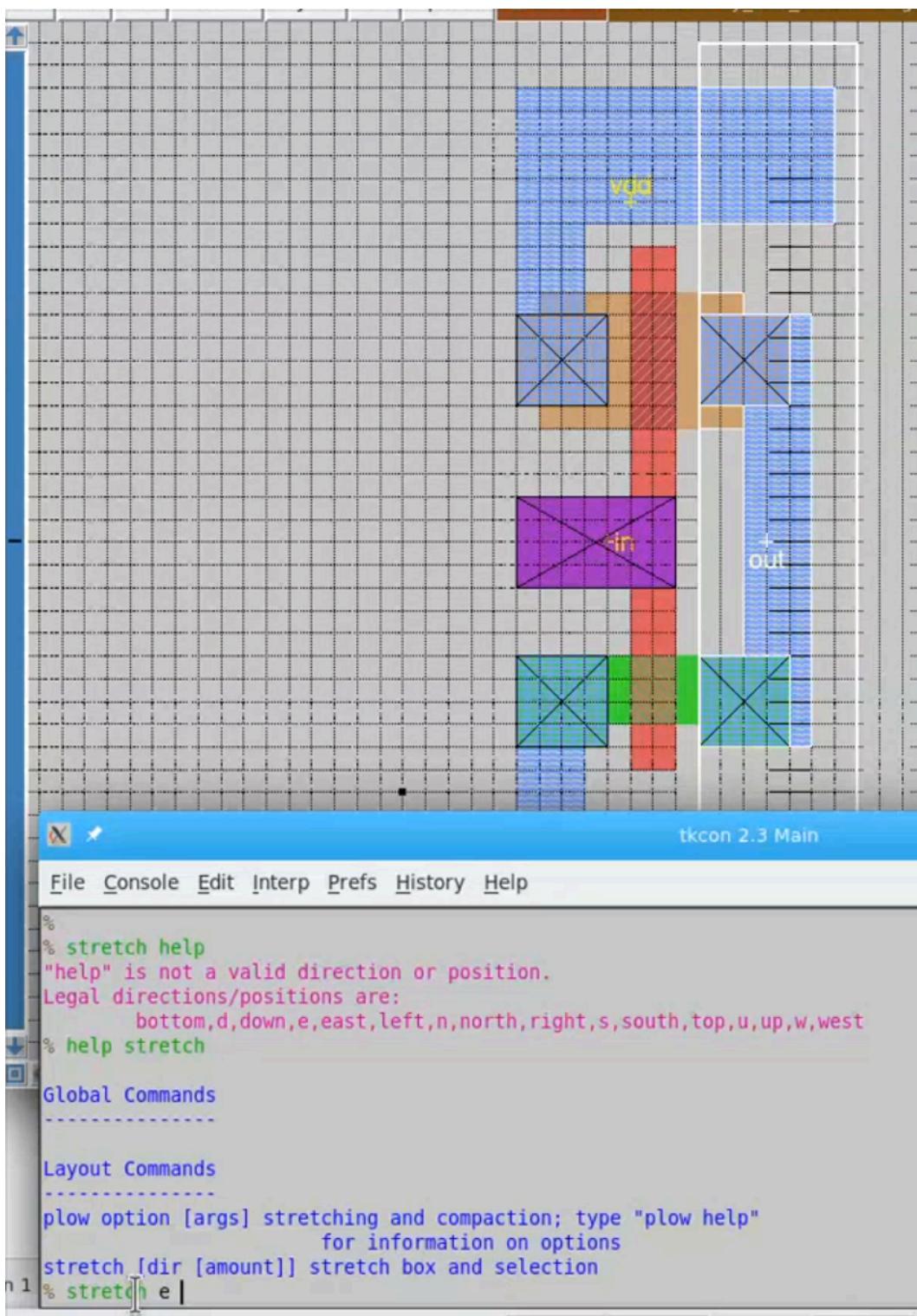
.option scale=1u

M1000 out in vss Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1001 out in vdd Vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
C0 vss Gnd 2.54fF
C1 vdd Gnd 2.44fF
C2 in Gnd 4.92fF
```

Changing M1 and M2 will affect the capacitances-



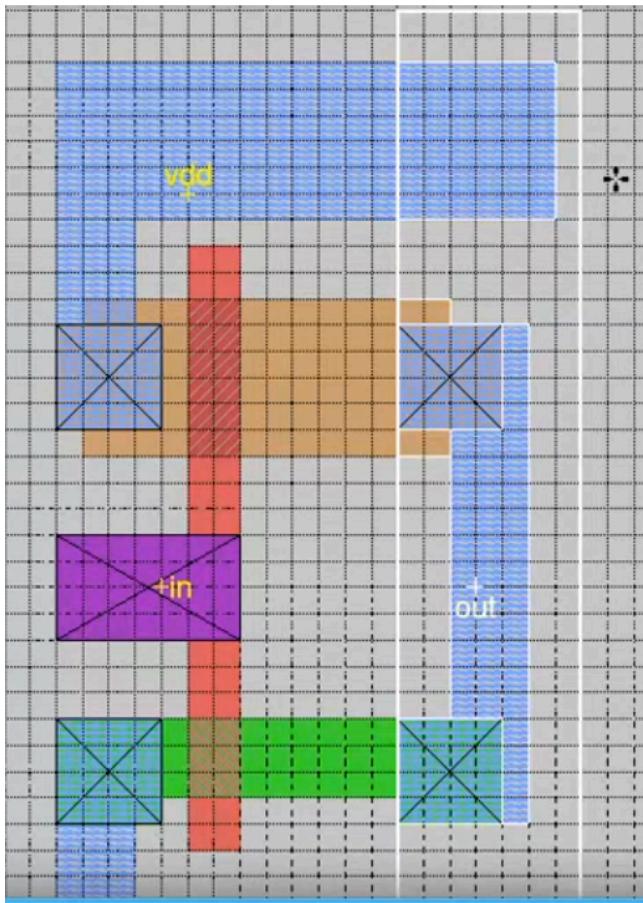
Stretching without disconnecting -



: select area

: stretch e 5

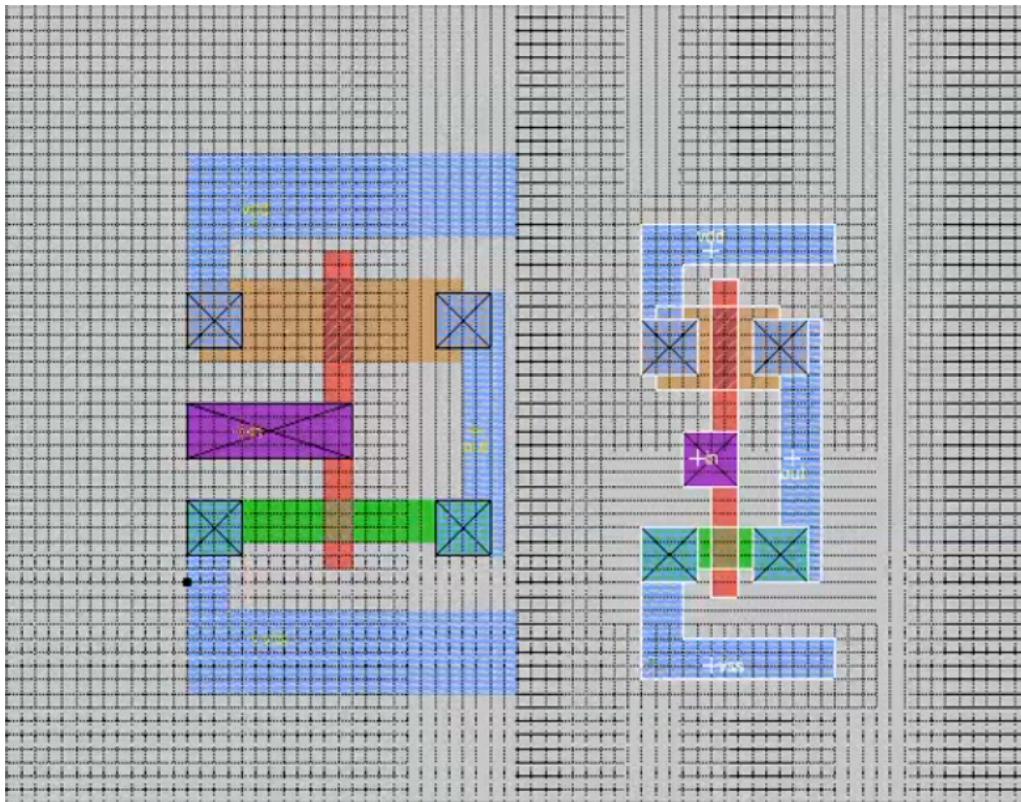
Result -



To get rid of that white outline -
: select clear

To select multiple objects -
: select more area

To copy-paste the cell (in row fashion) -
: dump filename.mag



Original spice netlist extracted from .mag file -

```
New Open... Save Save As... Close Undo
* SPICE3 file created from my_test_inv.ext - technology: scmos
.option scale=lu
M1000 out in vss Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1001 out in vdd Vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
C0 vss Gnd 2.54fF
C1 vdd Gnd 2.44fF
C2 in Gnd 4.92fF
```

Inorder to simulate this -

Make the following changes (note - .include <technology file>) -

```

* SPICE3 file created from my_test_inv.ext - technology: scmos
.option scale=1u
.include .....
M1000 out in vss Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1001 out in vdd Vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
C0 vss Gnd 2.54fF
C1 vdd Gnd 2.44fF
C2 in Gnd 4.92fF

V_DD vdd 0 5
V_SS vss 0 0
vin in 0 5

dc 0 5 0.1
|

```

And so on.. complete the netlist and plot accordingly.

Look into command extres (extract parasitic resistance?)

To compare layout Vs schematic - use **NETGEN** (LVS comparison)

For project use NETGEN and IRSIM

```

: extract
% ext2sim

```

Sim file (converts entire layout to switches and the corresponding parasitic RCs in that) -

```

| units: 100 tech: scmos format: MIT
n in vss out 2 3 10 3
p in vdd out 2 6 10 16
C vss GND 2.54
R vss 45
R out 176
C vdd GND 2.44
R vdd 105
C in GND 4.92
R in 272

```

Simulate this using IRSIM

For project, evaluation parameters include - area, speed, energy per transition

