PART 2: LAYOUT DESIGN USING MAGIC

**Lab 6: CMOS Inverter Layout**

**Objective:** To learn layout, extract, LVS and characterization processes in the design flow with CMOS inverter as an example.

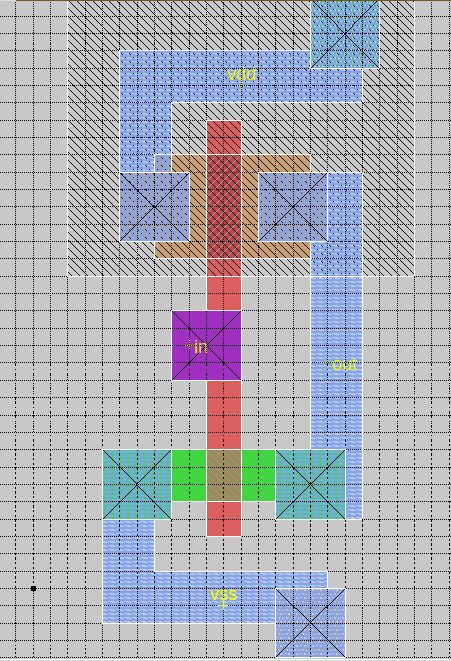


Fig: Layout design for CMOS Inverter

**Extracted spice netlist :**

\* SPICE3 file created from cmos.ext - technology: scmos

.option scale=1u

M1000 out in vss Gnd nfet w=3 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 out in vdd vdd pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 in Gnd 3.97fF

**(modified for NGSPICE simulation) :**

\* SPICE3 file created from cmos.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 out in vss Gnd cmosn w=3 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 out in vdd vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 in Gnd 3.97fF

Vdd vdd 0 5

Vin in 0 dc 2.5 pulse(0 5 0.01n 0.05n 0.05n 10n 20n)

Vss vss 0 0

.control

tran 0.1ns 40n

run

plot out, in

end

.endc

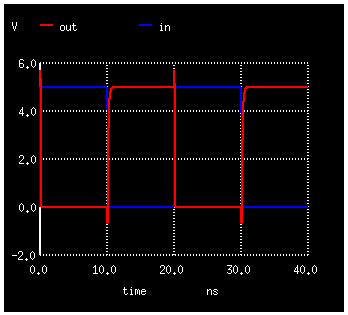


Fig: Transient response for CMOS Inverter

**Lab 7: Generation of standard cell library**

**Objective:** To create a standard cell library of CMOS gates – two and three input NAND, NOR, AND, OR gates, AOI for two products of two variables, D Latch and D-FlipFlop.

**(a) Two input NAND gate**

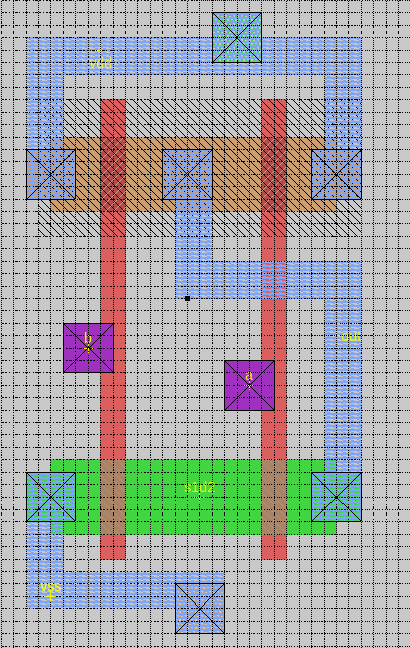


Fig: Layout design for NAND2

**Modified** **netlist for NGSPICE simulation:**

\* SPICE3 file created from cmos.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 out b vdd w\_n12\_5# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 s1d2 b vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 out a vdd w\_n12\_5# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 out a s1d2 Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 vss Gnd 2.40fF

C1 out Gnd 4.04fF

C2 a Gnd 6.35fF

C3 b Gnd 6.35fF

C4 vdd Gnd 4.18fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 a 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_2 b 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.A tran1.B tran1.out

.endc

.end

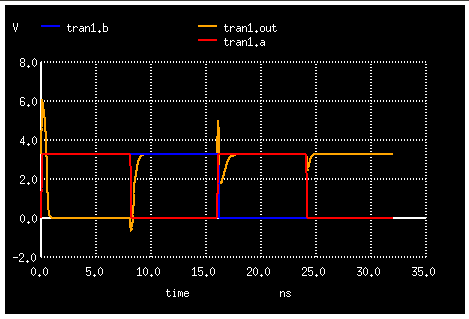


Fig: Transient response for NAND2

**3 input NAND gate**

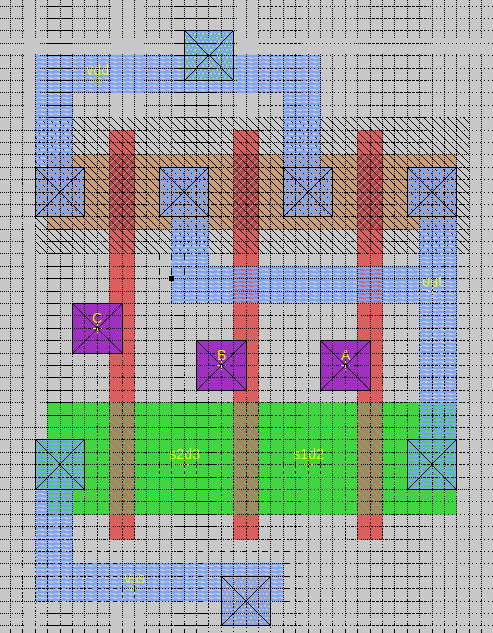


Fig: Layout design for NAND3

**Modified netlist for NGSPICE simulation:**

\* SPICE3 file created from cmos.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 out A vdd w\_n11\_2# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 out A s1d2 Gnd cmosn w=9 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 out C vdd w\_n11\_2# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 s1d2 B s2d3 Gnd cmosn w=9 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 out B vdd w\_n11\_2# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 s2d3 C vss Gnd cmosn w=9 l=2

+ ad=0 pd=0 as=0 ps=0

C0 vss Gnd 3.10fF

C1 out Gnd 4.09fF

C2 A Gnd 4.76fF

C3 B Gnd 4.76fF

C4 C Gnd 4.76fF

C5 vdd Gnd 3.43fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 A 0 PULSE(0 3.3 0 0 0 4ns 8ns)

v\_2 B 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_3 C 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.A tran1.B tran1.C tran1.out

.endc

.end

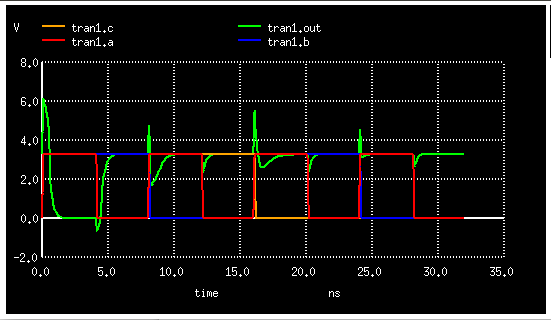


Fig: Transient response for NAND3

**(b) Two input NOR gate**

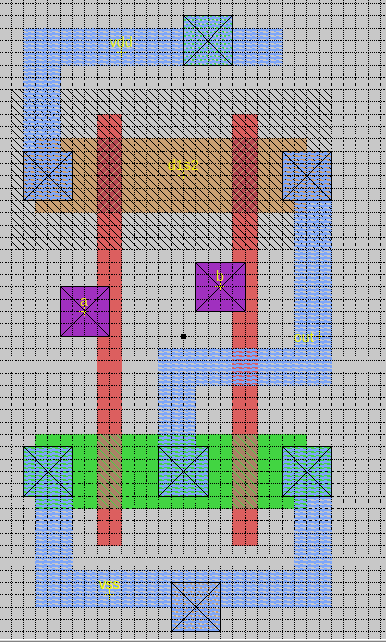
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Fig: Layout design for NOR2

**Modified netlist for NGSPICE simulation:**

\* SPICE3 file created from nor2.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 out a vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 d1s2 a vdd w\_n14\_7# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 out b d1s2 w\_n14\_7# cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 out b vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 vss Gnd 4.51fF

C1 out Gnd 3.38fF

C2 b Gnd 5.71fF

C3 a Gnd 5.71fF

C4 vdd Gnd 2.68fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 a 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_2 b 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.A tran1.B tran1.out

.endc

.end

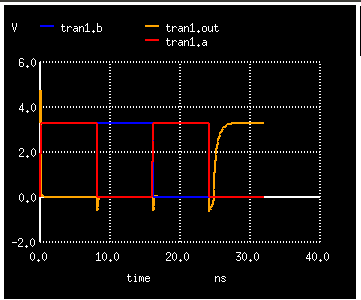


Fig: Transient response for NOR2

**3 input NOR gate**

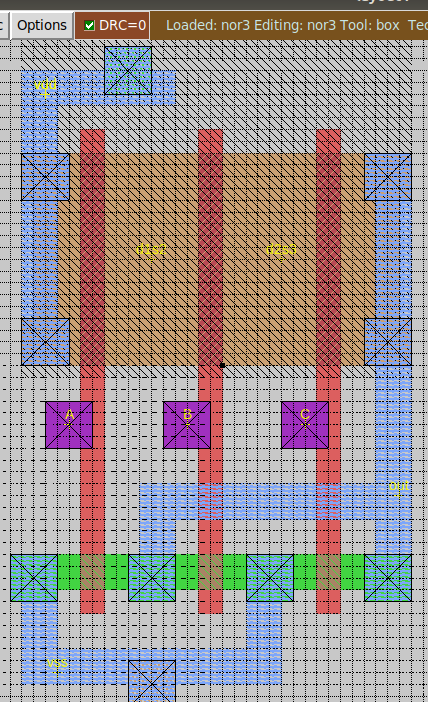


Fig: Layout design for NOR3

**Modified netlist for NGSPICE simulation:**

\* SPICE3 file created from cmos.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 d1s2 A vdd vdd cmosp w=18 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 d2s3 B d1s2 vdd cmosp w=18 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 out C vss Gnd cmosn w=3 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 out B vss Gnd cmosn w=3 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 out C d2s3 vdd cmosp w=18 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 out A vss Gnd cmosn w=3 l=2

+ ad=0 pd=0 as=0 ps=0

C0 vss Gnd 3.85fF

C1 out Gnd 4.79fF

C2 C Gnd 5.47fF

C3 B Gnd 5.47fF

C4 A Gnd 5.47fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 A 0 PULSE(0 3.3 0 0 0 4ns 8ns)

v\_2 B 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_3 C 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.A tran1.B tran1.C tran1.out

.endc

.end

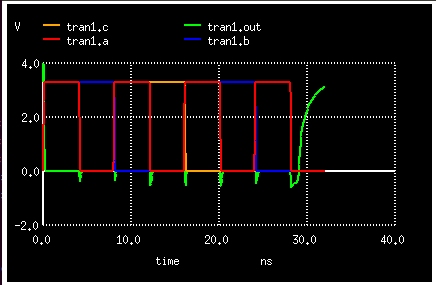


Fig: Transient response for NOR3

**(c) AND Gate**

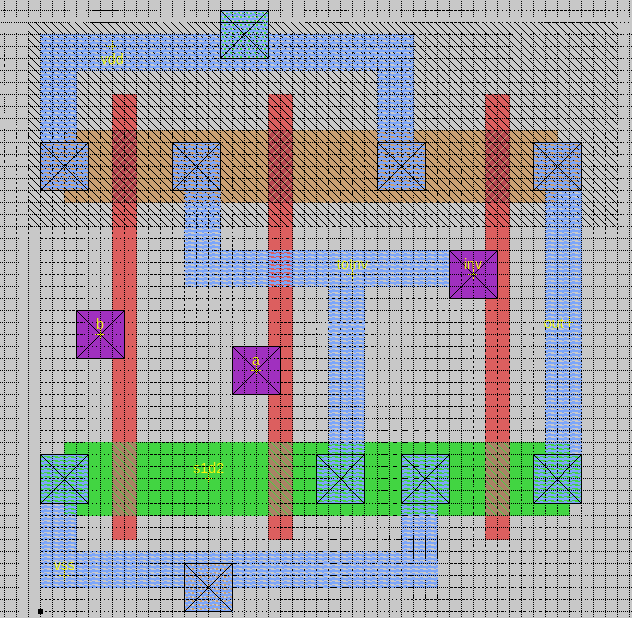


Fig: Layout design for 2 input AND gate

**Modified netlist for NGSPICE simulation:**

\* SPICE3 file created from nor2.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 inv a vdd vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 inv a s1d2 Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 inv b vdd vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 out inv vdd vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 out inv vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 s1d2 b vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 out Gnd 2.58fF

C1 inv Gnd 16.34fF

C2 a Gnd 6.19fF

C3 b Gnd 6.19fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 a 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_2 b 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.a tran1.b tran1.out

.endc

.end

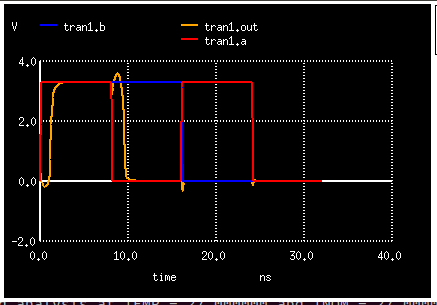


Fig: Transient response for AND2

**(d) OR gate**

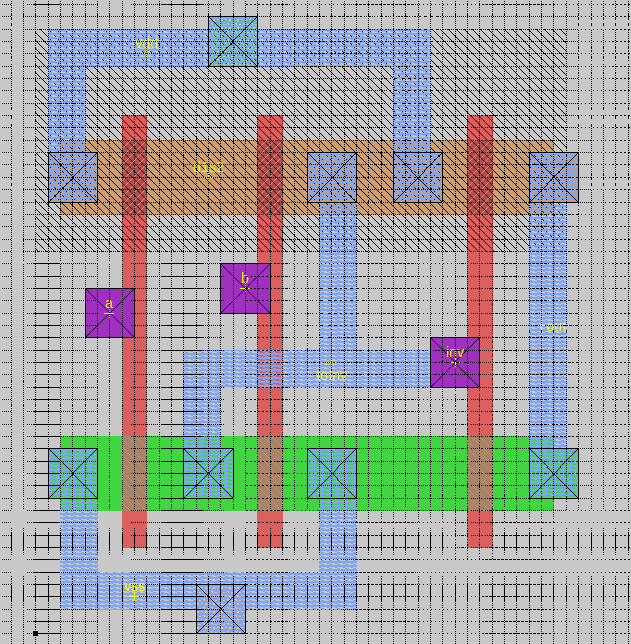


Fig: Layout design for 2 input OR gate

**Modified netlist for NGSPICE simulation:**

\* SPICE3 file created from nor2.ext - technology: scmos

.include ./t14y\_tsmc\_025\_level3.txt

.option scale=1u

M1000 inv b d1s2 vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 inv b vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 d1s2 a vss vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 out inv vdd vdd cmosp w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 inv a vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 out inv vss Gnd cmosn w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 vss Gnd 4.42fF

C1 out Gnd 2.16fF

C2 b Gnd 5.71fF

C3 a Gnd 5.71fF

C4 inv Gnd 9.94fF

v\_dd vdd 0 3.3

v\_ss vss 0 0

Gnd Gnd 0 0

v\_1 a 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_2 b 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.a tran1.b tran1.out

.endc

.end

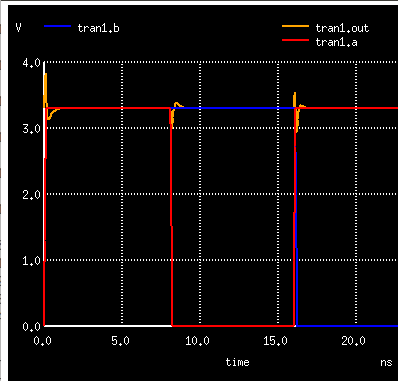


Fig: Transient response for AND2

**(e) AOI gate – (A.B + C.D)’**

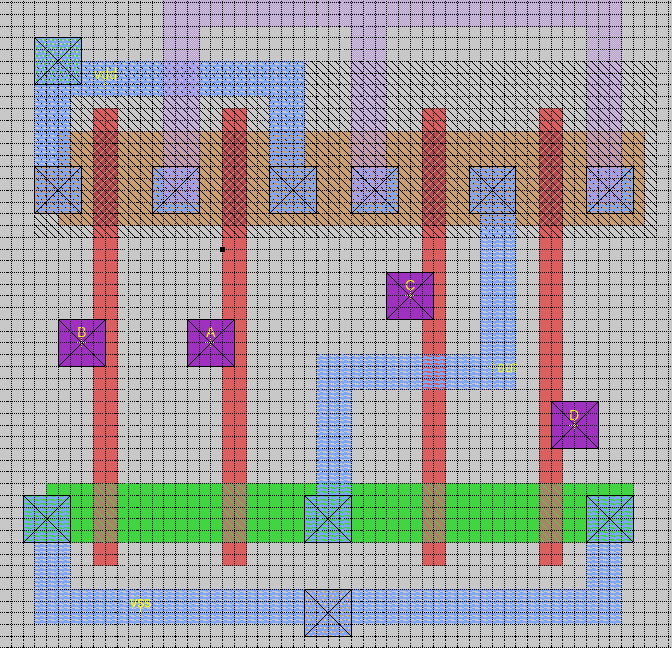


Fig: Layout design for AOI gate

**Extracted netlist (spice file) :**

\* SPICE3 file created from aoi.ext - technology: scmos

.option scale=1u

M1000 a\_n9\_2# B vdd vdd pfet w=8 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 a\_n9\_n25# B vss Gnd nfet w=5 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 out A a\_n9\_n25# Gnd nfet w=5 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 a\_19\_n25# D vss Gnd nfet w=5 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 a\_n9\_2# A vdd vdd pfet w=8 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 a\_29\_2# D out vdd pfet w=8 l=2

+ ad=0 pd=0 as=0 ps=0

M1006 out C a\_19\_n25# Gnd nfet w=5 l=2

+ ad=0 pd=0 as=0 ps=0

M1007 a\_29\_2# C out vdd pfet w=8 l=2

+ ad=0 pd=0 as=0 ps=0

C0 m2\_n5\_4# Gnd 2.74fF \*\*FLOATING

C1 vss Gnd 7.61fF

C2 out Gnd 4.65fF

C3 D Gnd 6.90fF

C4 C Gnd 6.90fF

C5 A Gnd 6.90fF

C6 B Gnd 6.90fF

**(f) D – Latch**

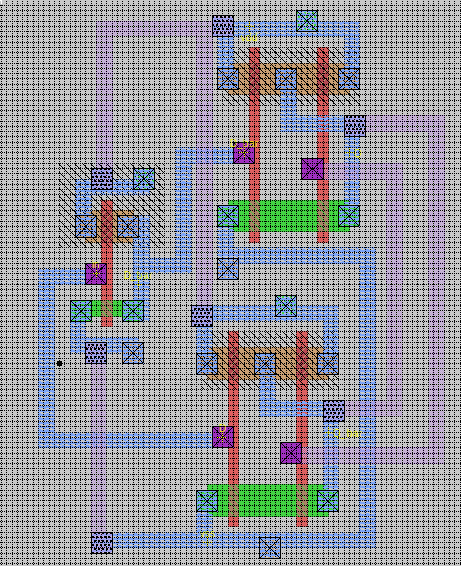


Fig: Layout design for D-Latch

**Extracted netlist (spice file) :**

\* SPICE3 file created from dlatch.ext - technology: scmos

.option scale=1u

M1000 vdd a\_46\_35# Q w\_31\_49# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 Q\_bar a\_42\_n19# a\_34\_n29# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 a\_38\_25# D\_bar vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 Q a\_46\_35# a\_38\_25# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 D\_bar in vdd vdd pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 D\_bar in vss Gnd nfet w=3 l=2

+ ad=0 pd=0 as=0 ps=0

M1006 a\_34\_n29# in vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1007 Q\_bar in vdd w\_27\_n5# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1008 Q D\_bar vdd w\_31\_49# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1009 vdd a\_42\_n19# Q\_bar w\_27\_n5# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

C0 Q\_bar Gnd 7.71fF

C1 a\_42\_n19# Gnd 6.35fF

C2 vss Gnd 23.70fF

C3 in Gnd 20.50fF

C4 Q Gnd 9.64fF

C5 a\_46\_35# Gnd 6.35fF

C6 D\_bar Gnd 13.16fF

C7 vdd Gnd 14.24fF

**(g) D – FlipFlop**

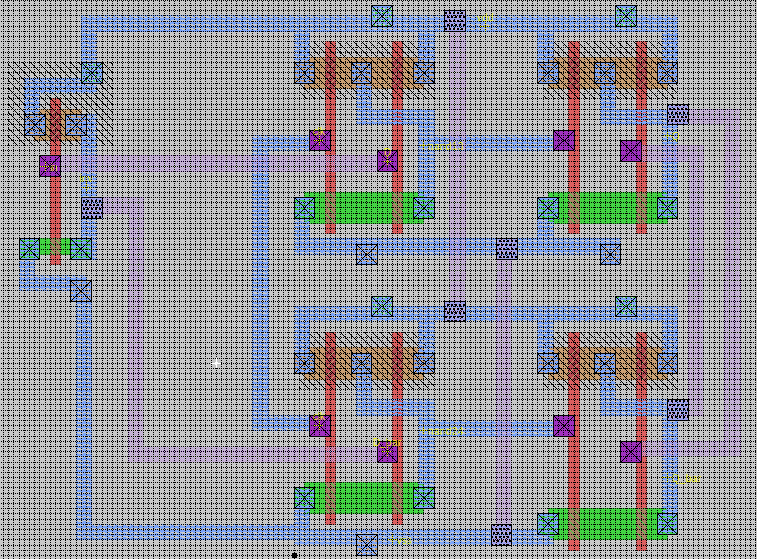
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Fig: Layout design for D-Flip Flop

**Extracted netlist (spice file) :**

\* SPICE3 file created from dff.ext - technology: scmos

.option scale=1u

M1000 Q\_bar nand24 vdd w\_48\_32# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1001 a\_55\_64# nand13 vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1002 vdd D\_bar nand24 w\_1\_32# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1003 vdd a\_63\_18# Q\_bar w\_48\_32# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1004 nand13 a\_16\_74# a\_8\_64# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1005 Q a\_63\_76# a\_55\_64# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1006 nand24 D\_bar a\_8\_8# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1007 nand13 clk vdd w\_1\_88# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1008 a\_55\_3# nand24 vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1009 Q\_bar a\_63\_18# a\_55\_3# Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1010 inv in vdd vdd pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1011 nand24 clk vdd w\_1\_32# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1012 a\_8\_64# clk vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1013 Q nand13 vdd w\_48\_88# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1014 vdd a\_16\_74# nand13 w\_1\_88# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1015 vdd a\_63\_76# Q w\_48\_88# pfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1016 a\_8\_8# clk vss Gnd nfet w=6 l=2

+ ad=0 pd=0 as=0 ps=0

M1017 inv in vss Gnd nfet w=3 l=2

+ ad=0 pd=0 as=0 ps=0

C0 D Gnd 3.02fF \*\*FLOATING

C1 Q\_bar Gnd 8.37fF

C2 a\_63\_18# Gnd 7.54fF

C3 nand24 Gnd 14.82fF

C4 D\_bar Gnd 6.35fF

C5 vss Gnd 33.07fF

C6 inv Gnd 8.56fF

C7 in Gnd 5.87fF

C8 Q Gnd 9.41fF

C9 a\_63\_76# Gnd 6.35fF

C10 nand13 Gnd 13.63fF

C11 a\_16\_74# Gnd 6.35fF

C12 clk Gnd 22.99fF

C13 vdd Gnd 32.00fF