VLSI DESIGN LAB

Report submitted in fullfilment of course

on VLSI Design Lab (EC302)

Under the guidance of

Dr. Ramesh Kini



Submitted by:

Adithi Sadananda Upadhya

191EC101

Department of Electronics & Communication Engineering

National Institute of Technology Karnataka, Surathkal

Srinivasnagar 575025 Karnataka, India

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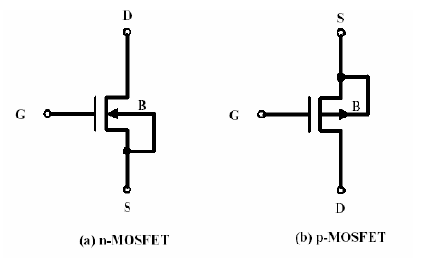
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PART 1: CIRCUIT SIMULATION WITH NGSPICE

**Lab 1: Study of VI characteristics of NMOS Transistor**

**Objective:** To study the input and output characteristics of NMOS Transistor, effects of L, W, VTO, LAMBDA, VSB, and temperature on the behavior of the transistor



**(a) Input-Output Characteristics**

.include ./t14y\_tsmc\_025\_level3.txt

\*netlist

m1 vdd in 0 0 cmosn l=1u w=0.55u

\*power sources

v\_dd vdd 0 3.3

v\_in in 0 3.3

.control

dc v\_in 0 3.3 0.1 v\_dd 0 3.3 1

run

setplot dc1

plot -v\_dd#branch

dc v\_dd 0 3.3 0.1 v\_in 0 3.3 1

run

setplot dc2

plot -v\_dd#branch

.endc

.end

3

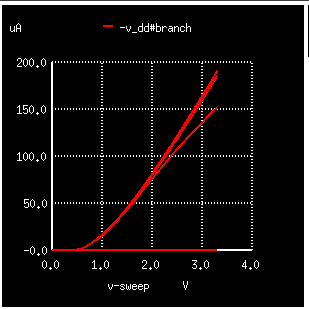


Figure 1: IDS vs VGS for varying VDS

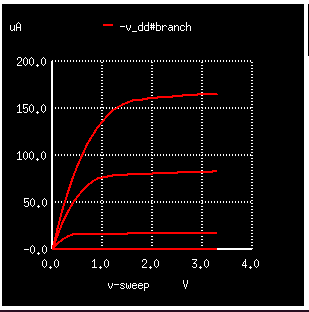


Figure 2: IDS vs VDS for varying VGS

**(b) Varying Width**

.include ./t14y\_tsmc\_025\_level3.txt

\*netlist

m1 vdd in 0 0 cmosn l=1u w=0.5u

\*power sources

4

v\_dd vdd 0 3.3

v\_in in 0 3.3

.dc v\_dd 0 3.3 0.1 v\_in 0 3.3 1

\*computing the response for various widths

.control

foreach wid 125e-9 500e-9 2500e-9

alter m1 w=$wid

run

end

.endc

\*plotting the output for various widths

.control

foreach iter 1 2 3

setplot dc$iter

plot -vdd#branch

end

.endc

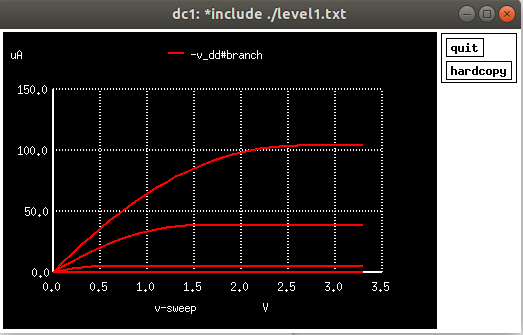


Figure 3: For width = 125n

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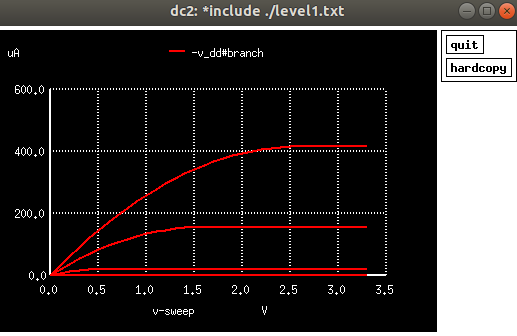


Figure 4: For width = 500n

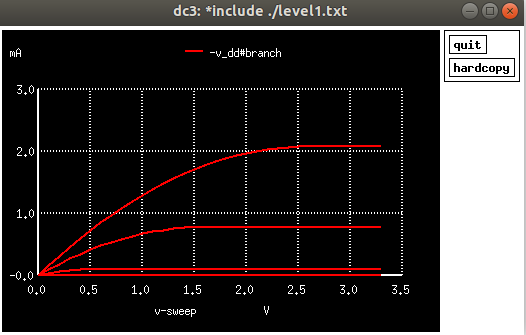


Figure 5: For width = 2500n

As seen in the VI characteristics above, with the increase in the value of width (W), the drain current (Id) increases.

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**(c) Varying Length**

.include ./t14y\_tsmc\_025\_level3.txt

\*netlist

m1 vdd in 0 0 cmosn l=3u w=0.5u

\*power sources

v\_dd vdd 0 3.3

v\_in in 0 3.3

.dc v\_dd 0 3.3 0.1 v\_in 0 3.3 1

\*computing the response for various lengths

.control

foreach len 125e-9 500e-9 2500e-9

alter m1 l=$len

run

end

.endc

\*plotting the output for various lengths

.control

foreach iter 1 2 3

setplot dc$iter

plot -v\_dd#branch

end

.endc

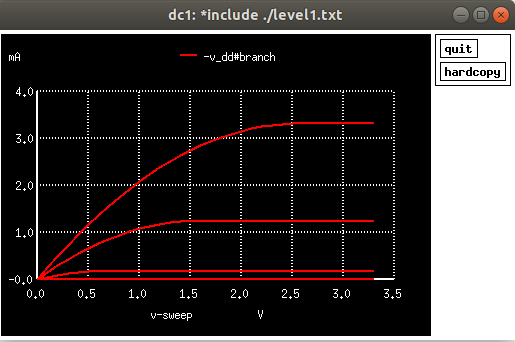


Figure 6: For length=125n

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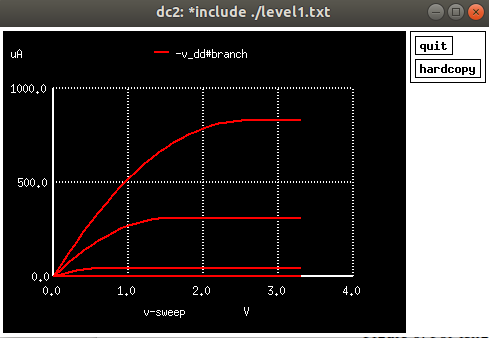


Figure 7: For length = 500n

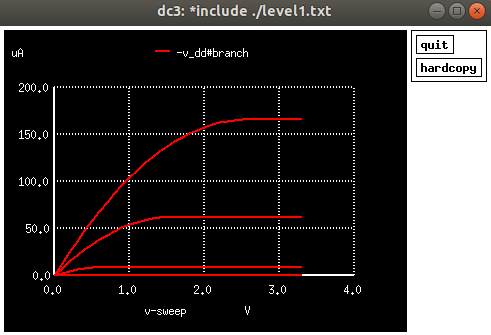


Figure 8: For length = 2500n

From the VI characteristics as seen above, with the increase in the value of length (L), the drain current (Id) decreases.

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**(d) Varying VTO**

.include /home/adithi/vlsi\_lab/Part1/level1.txt

.model cmosn nmos LEVEL=1 VTO=.03

m0 out in Vss 0 cmosn

\*sources

Vgnd Vss 0 dc 0

vdd out 0 dc 5

\*input\_source

Vin in 0 dc 5

.dc Vin 0 5 .1

.control

foreach val 0.5 1 2

altermod m0 VTO = $val

run

end

.endc

.control

foreach iter 1 2 3

setplot dc$iter

end

plot dc1.vdd#branch\*-1 dc2.vdd#branch\*-1 dc3.vdd#branch\*-1

.endc

.end

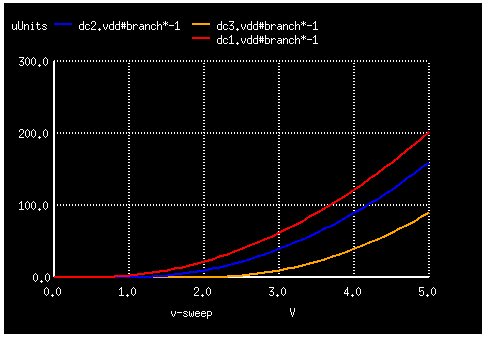


Figure 9: For Varying VTO

In the above figure for VI characteristics, as the value of VTO increases, the drain current decreases.

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**(e) Varying LAMBDA**

.include /home/adithi/vlsi\_lab/Part1/level1.txt

.model cmosn nmos LEVEL=1 VTO=.03

m1 vdd in 0 0 cmosn

\*sources

v\_dd vdd 0 3.3

v\_in in 0 3.3

.dc v\_dd 0 3.3 0.1 v\_in 0 3.3 1

.control

foreach ld .01 .05 .09

altermod m1 LAMBDA = $ld

run

end

.endc

.control

foreach iter 1 2 3

setplot dc$iter

plot -v\_dd#branch

end

.endc

.end

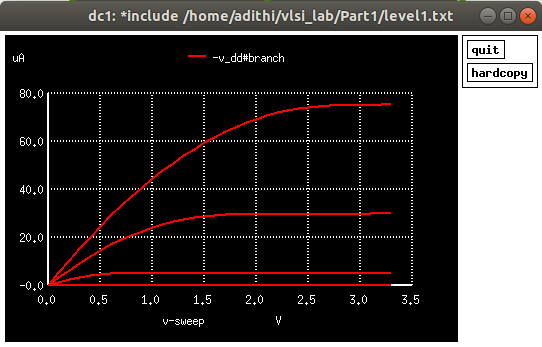


Figure 10: Id Vs Vdd for LAMBDA = 0.01

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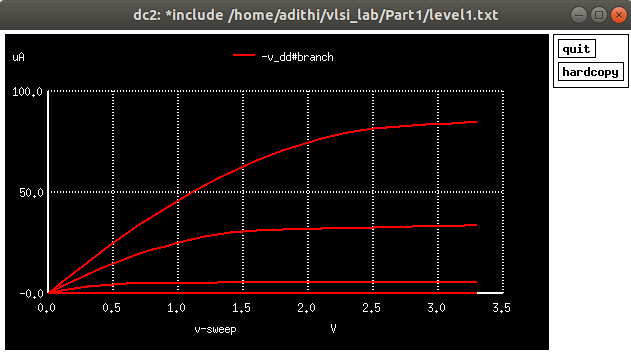


Figure 11: Id Vs Vdd for LAMBDA = 0.05

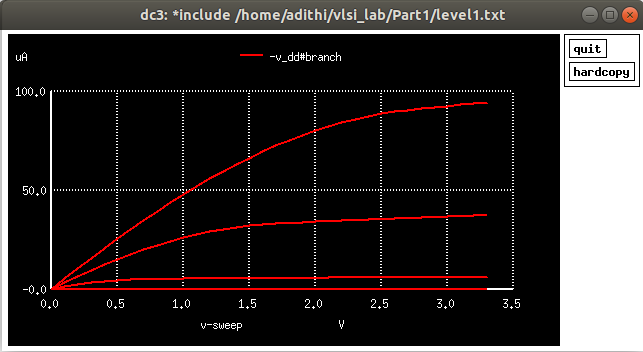


Figure 12: Id Vs Vdd for LAMBDA = 0.09

The Id vd Vdd curve is linear at first, then slowly varies in the saturation region due to channel length modulation which should otherwise be constant. As lambda is increased, the saturation region drain current also increases slightly as the drain-to-source voltage increases.

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**(f) Varying VSB**

.include ./t14y\_tsmc\_025\_level3.txt

\*netlist

m1 vdd in s 0 cmosn l=1u w=0.55u

\*power sources

v\_dd vdd 0 5

v\_in in 0 5

v\_ss s 0 0

.dc v\_in 0 5 0.1 v\_ss 0 3 1

.control

run

setplot dc1

plot -v\_dd#branch

.endc

.end

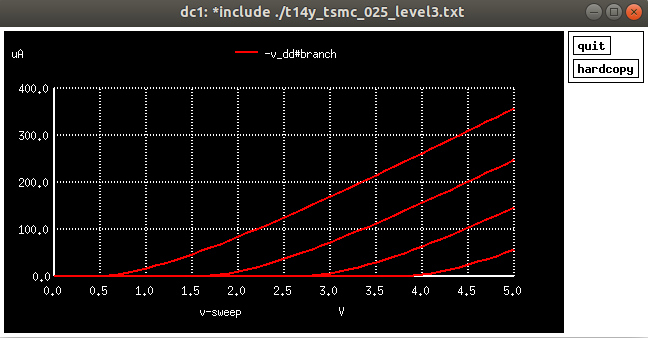


Figure 13: For varying VSB

As VSB is increased, the threshold voltage also increases due to body-effect.

**(g) Varying temperature**

.include ./t14y\_tsmc\_025\_level3.txt

m0 out in Vss 0 cmosn TEMP=27

12

\*sources

Vgnd Vss 0 dc 0

vdd out 0 dc 5

\*input\_source

Vin in 0 dc 5

.dc Vin 0 5 .1

.control

foreach t1 27 50 100

alter m0 TEMP=$t1

run

end

.endc

.control

foreach iter 1 2 3

setplot dc$iter

end

plot dc1.vdd#branch\*-1 dc2.vdd#branch\*-1 dc3.vdd#branch\*-1

.endc

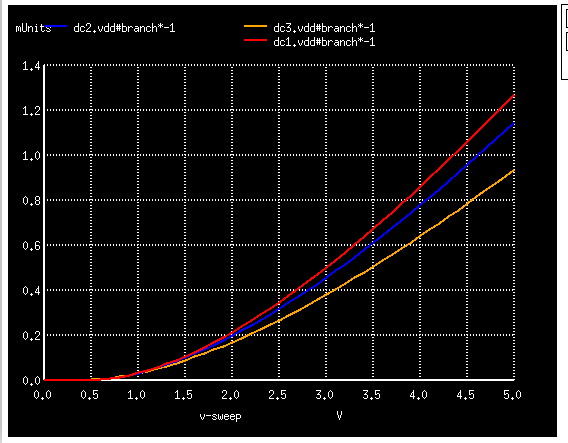
.end

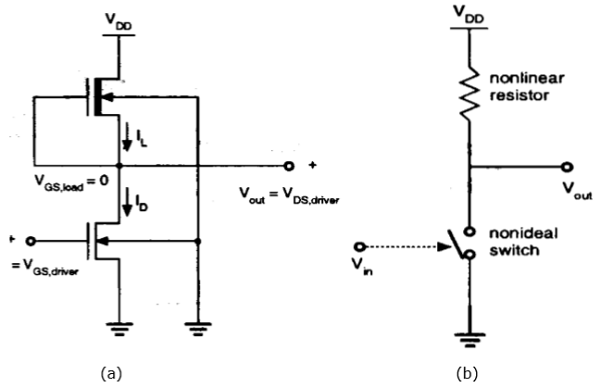
Figure 14: For varying temperature

From the VI characteristics as seen above, as temperature increases, it is observed that current (Id) decreases.

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**Lab 2: Study of MOS Inverter with passive resistive load**

**Objective:** To study the transfer function, noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a MOS Inverter for various L, W of the transistor, load capacitance and rise/fall time of input.



**(a) Varying load resistance and width**

.include ./t14y\_tsmc\_025\_level3.txt

\*netlist

m0 out in 0 0 cmosn l=1.8u w=6.4u

r0 vdd out 100

\*power sources

Vdd vdd 0 5

Vin in 0 dc 2.5 pulse(0 5 0.01n 0.05n 0.05n 10n 20n)

\* computing the response for various load resistance values

.control

foreach res 100 1k 100k

alter r0=$res

tran 0.1ns 2n

dc Vin 0 5 0.1

end

.endc

.control

foreach iter 1 2 3

setplot dc$iter

setplot tran$iter

end

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plot tran1.in tran1.out tran2.out tran3.out

plot dc1.out dc2.out dc3.out vs in

.endc

.end

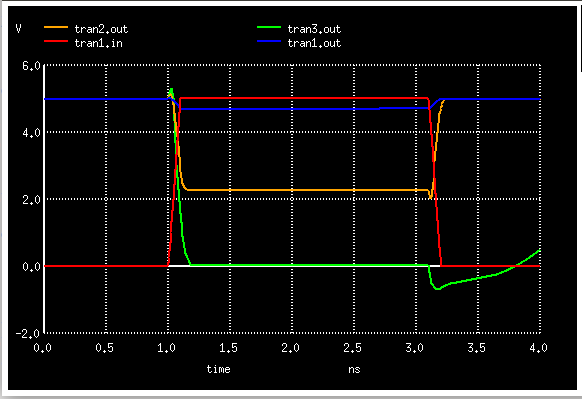


Figure 15: Transient analysis - due to varying Resistance

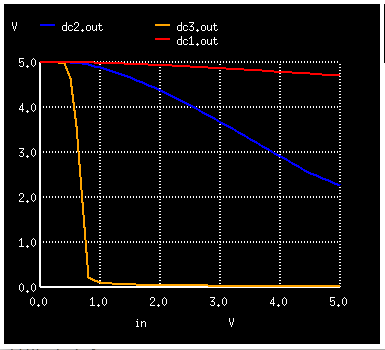


Figure 16: DC Analysis – VTC due to varying resistance ( Vout vs Vin)

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For a given W/L ratio of driver NMOS, as load resistance (RL) increases -

* Inverter gain increases ; VTC slope increases
* VTC curve shifts left

**Varying width:**

.include ./t14y\_tsmc\_025\_level3.txt

m0 out in 0 0 cmosn w=6.4u l=1.8u ad=6.84p pd=10.8u as=6.84p ps=10.8u

r0 vdd out 1k

Vdd Vdd 0 dc 5

Vin in 0 dc 2.5 pulse(0 5 0.01n 0.05n 0.05n 10n 20n)

.dc Vin 0 5 0.1

\* computing the response for various widths

.control

foreach wid 125e-9 500e-9 2500e-9

alter m0 w=$wid

run

end

.endc

\* plotting the output for various widths

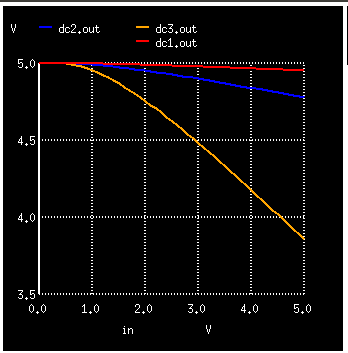
.control

foreach iter 1 2 3

setplot dc$iter

end

plot dc1.out dc2.out dc3.out vs in

.endc

.end

Figure 17: DC Analysis – VTC due to varying aspect ratio ( Vout vs Vin)

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**Lab 3: Study of MOS Inverter with active load - NMOS and PMOS (pseudo NMOS load)**

**Objective:** For a MOS Inverter with active load – NMOS and PMOS (pseudo NMOS load), study the transfer function, noise margin, effect on risetime, falltime, propagation delay, power and energy consumed with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

**Lab 4: Study of CMOS Inverter**

**Objective:** To study the transfer function, noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a CMOS Inverter with variation in L and W of pull up and pull down transistors. Also power and energy consumed with non ideal step input.

**(a) Transfer function**

.include ./t14y\_tsmc\_025\_level3.txt

m1 out in 0 0 cmosn l=1u w=1u

m2 out in vdd vdd cmosp l=1u w=2u

v\_dd vdd 0 dc 5

v\_in in 0 dc 5

.dc v\_in 0 5 0.1

.control

run

plot out,in

.endc

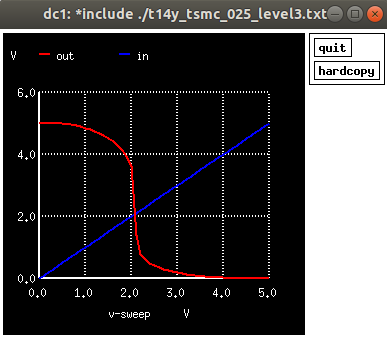
.end

Figure : Transfer Function

**Tranfer function, effect on rise time, power consumed due to variation in the width of NMOS:**

.include ./t14y\_tsmc\_025\_level3.txt

\* NMOS - Driver, PMOS - Load

m0 out in vdd vdd cmosp l=1u w=.6u

m1 out in 0 0 cmosn l=1u w=.2u

v\_dd vdd 0 dc 5

v\_in in 0 dc 5 pulse(5 0 .01m .2m .2m .5m 1m)

.dc v\_in 0 5 .01

\*varying W of nmos

.control

foreach wdt .6u 2u 10u

alter m1 w=$wdt

tran .001m 1m

run

end

.endc

\* plot for various w of load

.control

foreach iter 1 2 3

setplot dc$iter

setplot tran$iter

end

.endc

\* case-1 dc analysis for transfer function varying with W of nmos

\* case-2 tran analysis to observe the effect on rise time

\* case-3 for power variation

.control

plot tran1.out tran2.out tran3.out

plot dc1.out dc2.out dc3.out

plot tran1.v\_dd#branch\*vdd\*-1 tran2.v\_dd#branch\*vdd\*-1 tran3.v\_dd#branch\*vdd\*-1

.endc

.end

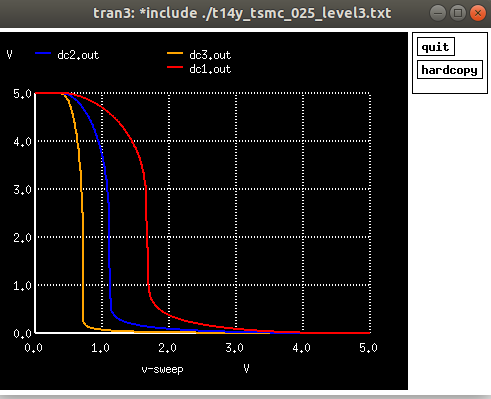


Figure :Transfer function due to varying width of NMOS

As width of NMOS (driver) increases, the VTC curve shifts towards the left.

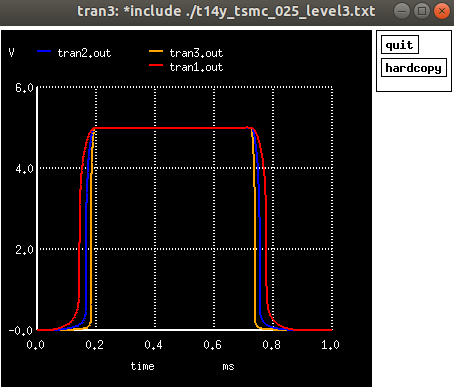
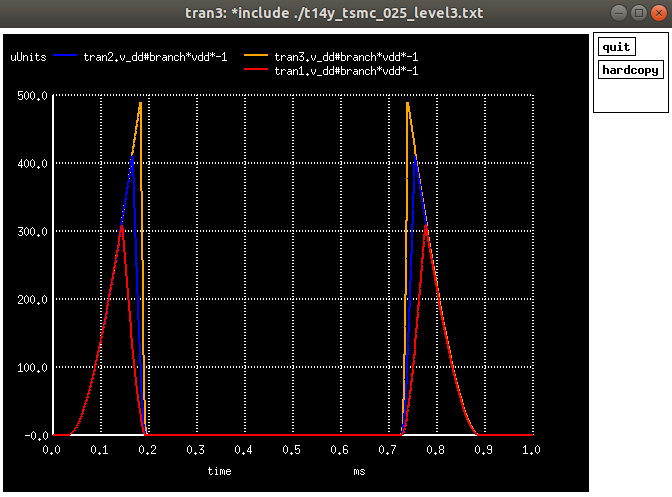


Figure : Effect on rise time due to variation in W of NMOS

Figure : Effect of varying W of NMOS on power consumed

**Tranfer function, effect on rise and fall time, power consumed due to variation in the length of NMOS:**

.include ./t14y\_tsmc\_025\_level3.txt

\* NMOS - Driver, PMOS - Load

m0 out in vdd vdd cmosp l=1u w=.6u

m1 out in 0 0 cmosn l=1u w=.2u

v\_dd vdd 0 dc 5

v\_in in 0 dc 5 pulse(5 0 .01m .2m .2m .5m 1m)

.dc v\_in 0 5 .01

\*varying W of nmos

.control

foreach len 0.5u 2u 10u

alter m1 l=$len

tran .001m 1m

run

end

.endc

\* plot for various L of load

.control

foreach iter 1 2 3

setplot dc$iter

setplot tran$iter

end

.endc

\* case-1 dc analysis for transfer function varying with L of nmos

\* case-2 tran analysis to observe the effect on rise time

\* case-3 for power variation

.control

plot tran1.out tran2.out tran3.out

plot dc1.out dc2.out dc3.out

plot tran1.v\_dd#branch\*vdd\*-1 tran2.v\_dd#branch\*vdd\*-1 tran3.v\_dd#branch\*vdd\*-1

.endc

.end

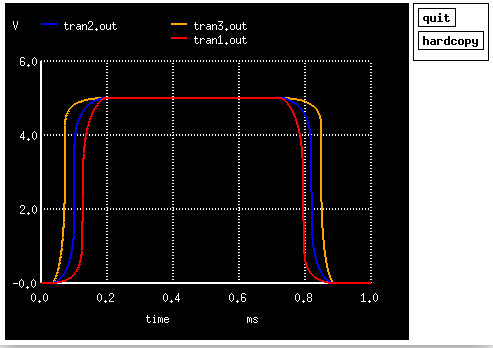


Figure : Effect on rise and fall time due to variation in L of NMOS

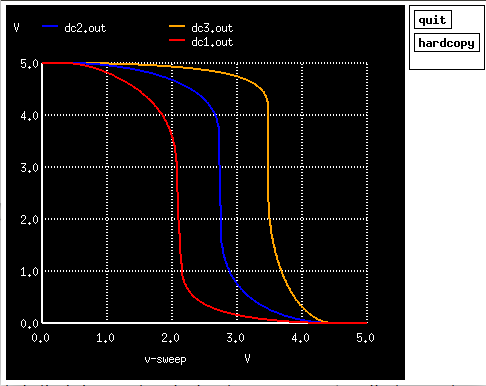
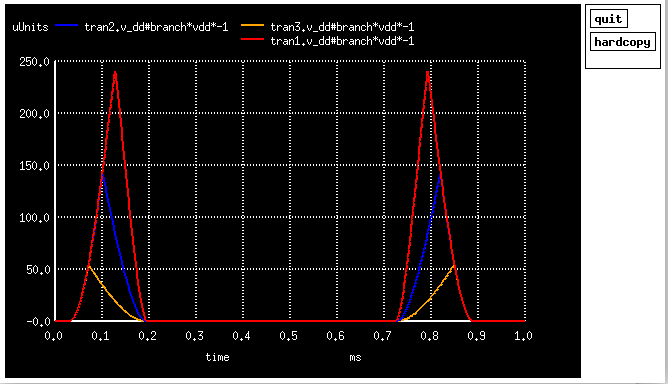


Figure :Transfer function due to varying length of NMOS

Figure : Effect of varying L of NMOS on power consumed

**Variation in the length of PMOS (Load) :**

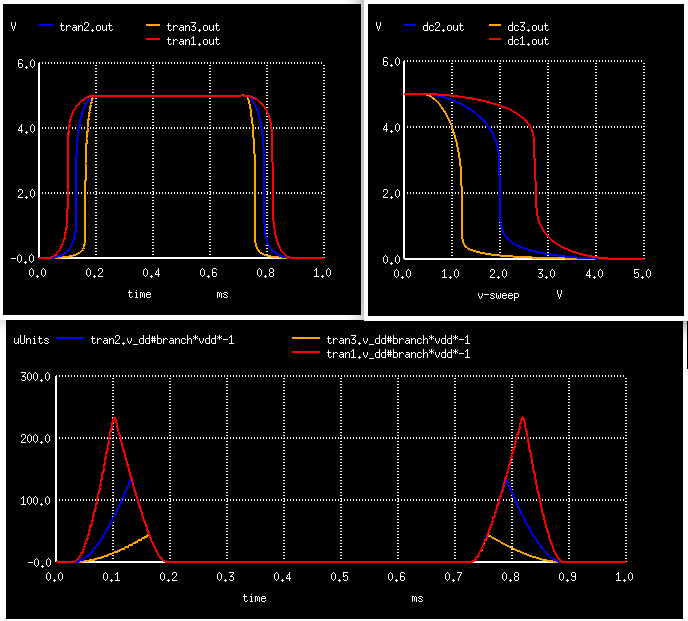


Figure : Effect on rise and fall time, transfer characteristics, and power consumed due to variation in length of load PMOS

**Variation in the width of PMOS (Load) :**

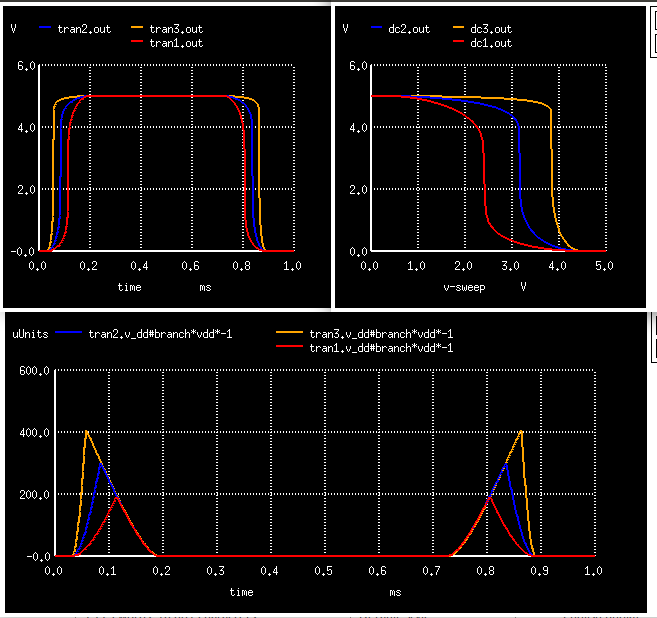


Figure : Effect on rise and fall time, transfer characteristics, and power consumed due to variation in width of load PMOS

**(b) Varying rise and fall time of input**

**(c) Varying capacitive load at the load ( by estimating the input capacitance of inverter and experimenting with different fan out loads)**

**Lab 5: Study of CMOS gates**

**Objective:** To study the behaviour transfer function, noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of CMOS gates like NAND, NOR, functions like AOI ( 2 input AND gate, 2 input OR gate), and 2 input XOR gate with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input. Study the effect of VSB due to series connected transistors.

**(a) NAND GATE**

.include ./t14y\_tsmc\_025\_level3.txt

\* F = (A.B)' NAND

m1 F A int 0 cmosn L=1u W=10u

m2 int B 0 0 cmosn L=1u W=10u

m3 F A vdd vdd cmosp L=1u W=10u

m4 F B vdd vdd cmosp L=1u W=10u

v\_dd vdd 0 3.3

v\_1 A 0 PULSE(0 3.3 0 0 0 8ns 16ns)

v\_2 B 0 PULSE(0 3.3 0 0 0 16ns 32ns)

.control

tran 0.1ns 32ns

run

end

plot tran1.A tran1.B tran1.F

.endc

.end

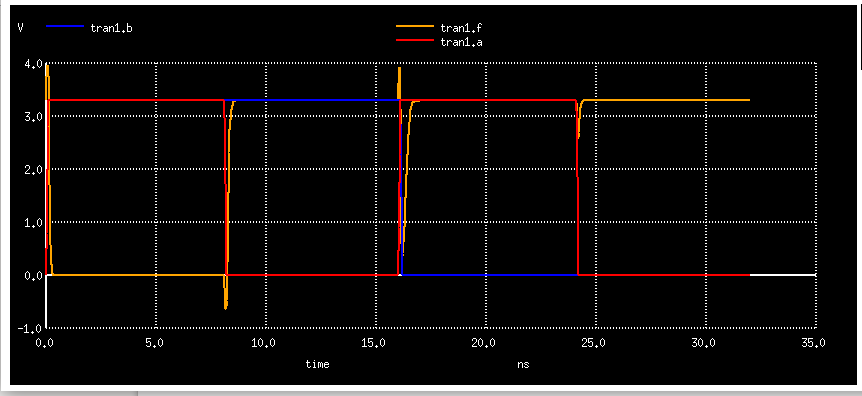


Figure : Transient response for NAND gate

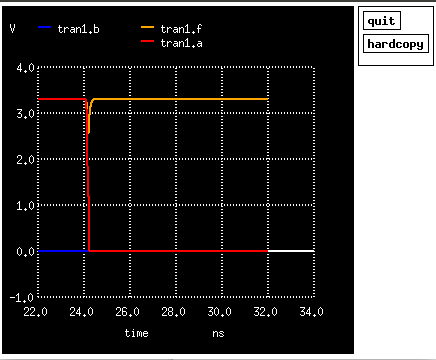


Figure : Transient response for NAND gate with inputs A=0, B=0

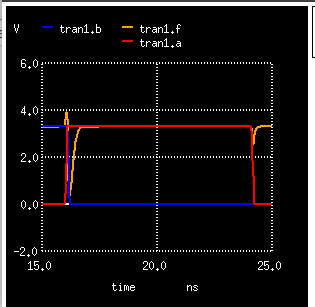


Figure : Transient response for NAND gate with inputs A=1, B=0

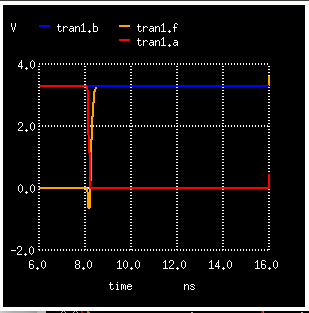


Figure : Transient response for NAND gate with inputs A=0, B=1

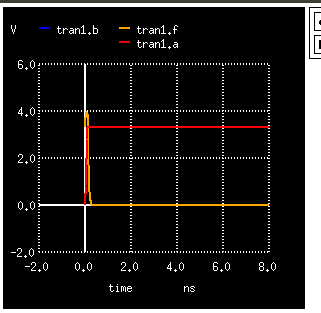


Figure : Transient response for NAND gate with inputs A=1, B=1

**(b) NOR GATE**